Assignments and Delays (1A)

- Intra-Assignment Delays

Please send corrections (or suggestions) to youngwlim@hotmail.com.

This document was produced by using OpenOffice and Octave.

Intra Assignment Delays

```
module M1;
integer a, b;

 always
    b = #2 a;

 initial
   begin
            a=0; b=0;
      #2  a=1;
      #2  a=2;
      #2  a=3;
      #2  a=4;
      #2  a=5;
      #2  a=6;
      #2  a=7;
   end
endmodule
```

Blocking and NonBlocking Assignments

a = b;

- b is evaluated and used immediately to update a.
- The next statement will use this updated new value
- If a is an output of a process, elements on a's fanout list are scheduled in the current time as a regular evaluation events.

a <= b;

- b is evaluated and nonblocking update event is scheduled for a.
- execution of the process continues.
- only after the nonblocking update events are executed, this new value will be seen

```
a = 1;
b = 0;

#10
a = b;  // a = 0
b = a;  // b = 0
```

```
a = 1;
b = 0;

#10
a <= b;
b <= a;
// a = 0, b = 1
```

Blocking and NonBlocking Assignments

```
a = 1;
b = 0;

#10
a = b;  // a = 0
b = a;  // b = 0
```

```
a = 1;
b = 0;

#10
a = b;  // a = 0
b <= a;
// b = 0
```

```
a = 1;
b = 0;

#10
a <= b;
b <= a;
// a = 0, b = 1
```

```
a = 1;
b = 0;

#10
a <= b;
b = a;   // b = 1
// a= 0
```

Intra Assignment Delays

a = #0 b;

- b is evaluated and an update event for a is scheduled as a regular event in the current time.
- The current process will be blocked until the next simulation cycle when the update of a will occur and the process will continue executing.

a <= #0 b;

- b is evaluated and nonblocking update event is scheduled for the current time.
- The current process will continue executing.
- The update event will be executed after all regular events for the current time are executed

Intra Assignment Delays

a = #4 b;

- like a = #0 b;
- the update event and the continuation of the process is scheduled 4 time units into the future

a <= #4 b;

- like a <= #0 b;
- a will not be updated (using a non-blocking update event) until 4 time units into the future.

Delay

#3 a = b;

- Wait 3 time units before doing the action for a=b.
- The value assigned to a will be the value of b 3 time units hence.

a <= #4 b;

- Wait 3 time units before doing the action for a=b.
- The value assigned to a will be the value of b 3 time units hence.

Delay

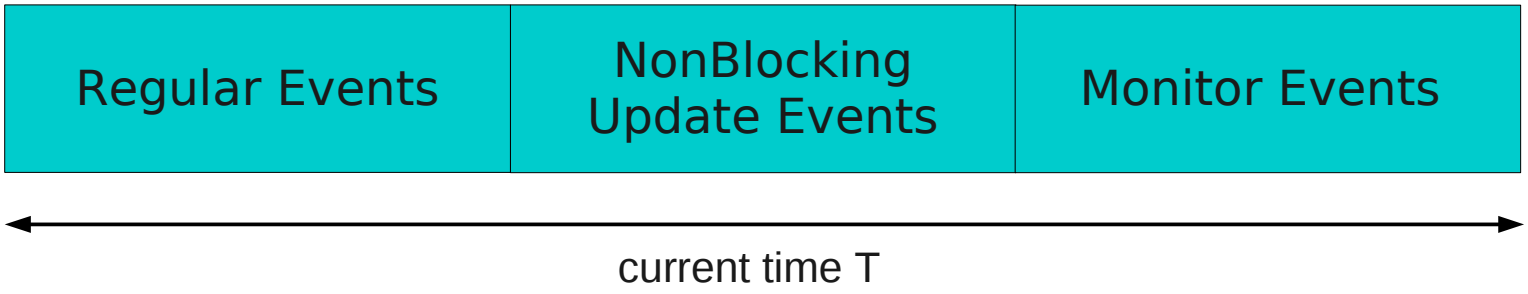
Note that in the above situations the value assigned to a is the same.
the value of b in the last two examples could change in the next three time units.
But for those two cases, the value assigned toa would be the same.
The differences lie in what part of the event list the update is scheduled in, whether the value is available in the next behavioral statement, and whether the current process is blocked because of the #

a <= #4 b;

- Wait 3 time units before doing the action for a=b.
-

All regular events for time T scheduled form previous times or current time T are scheduled here

All nonblocking update events for current time T scheduled form previous times or current time T are scheduled here



Sequential Assignment (2)

References

[1] http://en.wikipedia.org/
[2] T.R. Padmanabhan, B.T. Sundari, “Design Through Verilog HDL
[3] Thomas & Moorby, The Verilog Hardware Description Language”, 3rd ed.