FPGA Carry Chain Adder (1A)

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Please send corrections (or suggestions) to youngwlim@hotmail.com.

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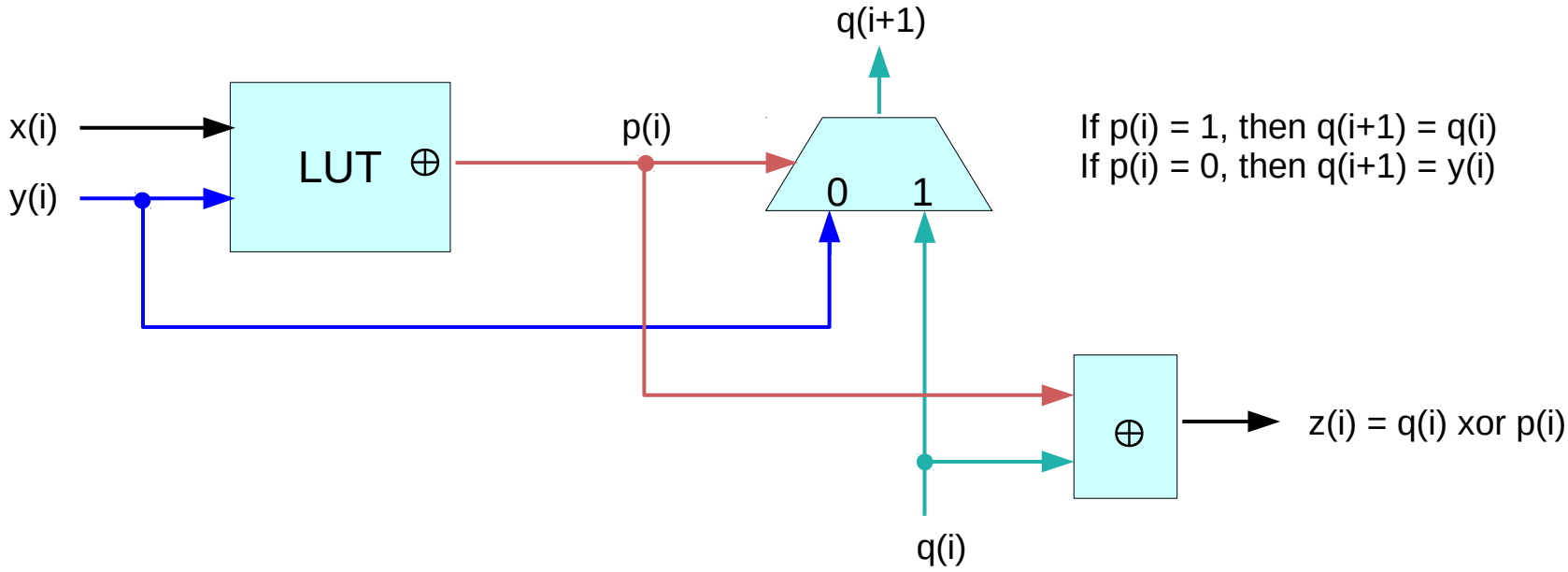
FPGA Carry Chain Cell



$$s_i = (a_i \oplus b_i) \oplus c_i = p_i \oplus c_i$$

$$c_{i+1} = (a_i \cdot b_i) + (a_i \oplus b_i) c_i = \overline{p_i} \cdot g_i + p_i \cdot c_i = \overline{p_i} \cdot a_i + p_i \cdot c_i = \overline{p_i} \cdot b_i + p_i \cdot c_i$$

when $\overline{p_i} = 1$, *then* $a_i = b_i$

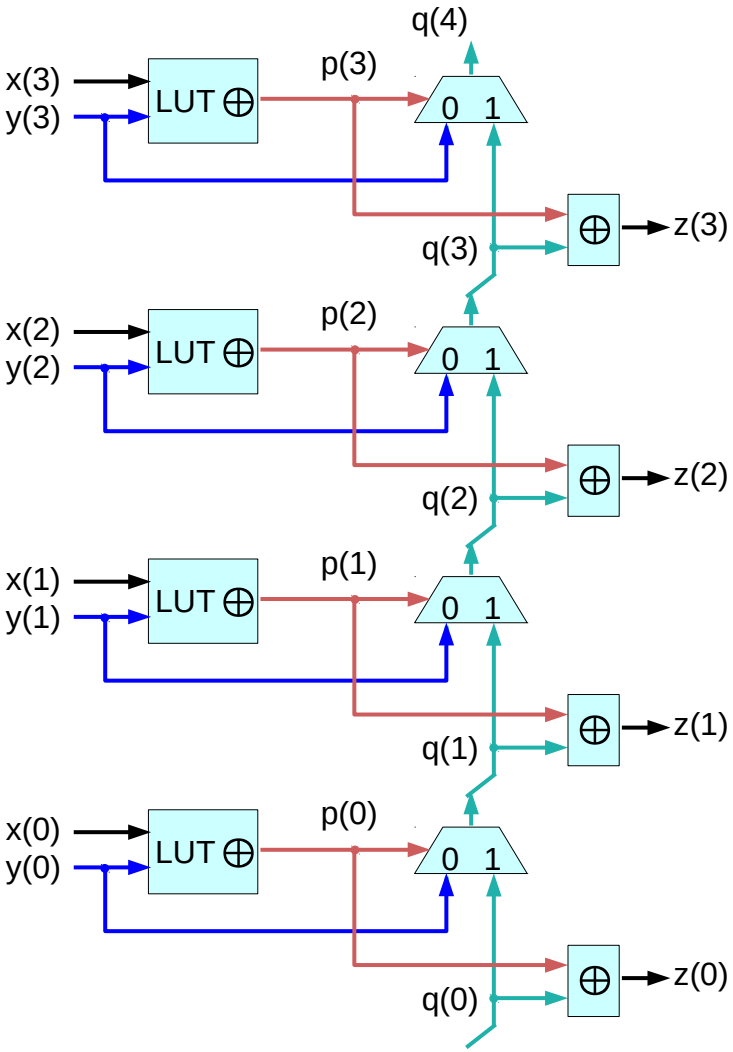
when $g_i = 1$, *then* $a_i = b_i = 1$

p(i)	0	1
0	0	1
1	1	0

g(i)	0	1
0	0	0
1	0	1

Synthesis of Arithmetic Circuits: FPGA, ASIC and Ebedded Systems, J-P Deschamps et al

FPGA Carry Chain Cell



Synthesis of Arithmetic Circuits: FPGA, ASIC and Ebedded Systems, J-P Deschamps et al

FPGA Carry Chain

FPGAs generally contain dedicated computation resources
for generating fast adders

The Virtex family programmable arrays include
logic gates (**XOR**) and **multiplexers** that along with the
general purpose **lookup tables** allow one to build effective carry-chain adders

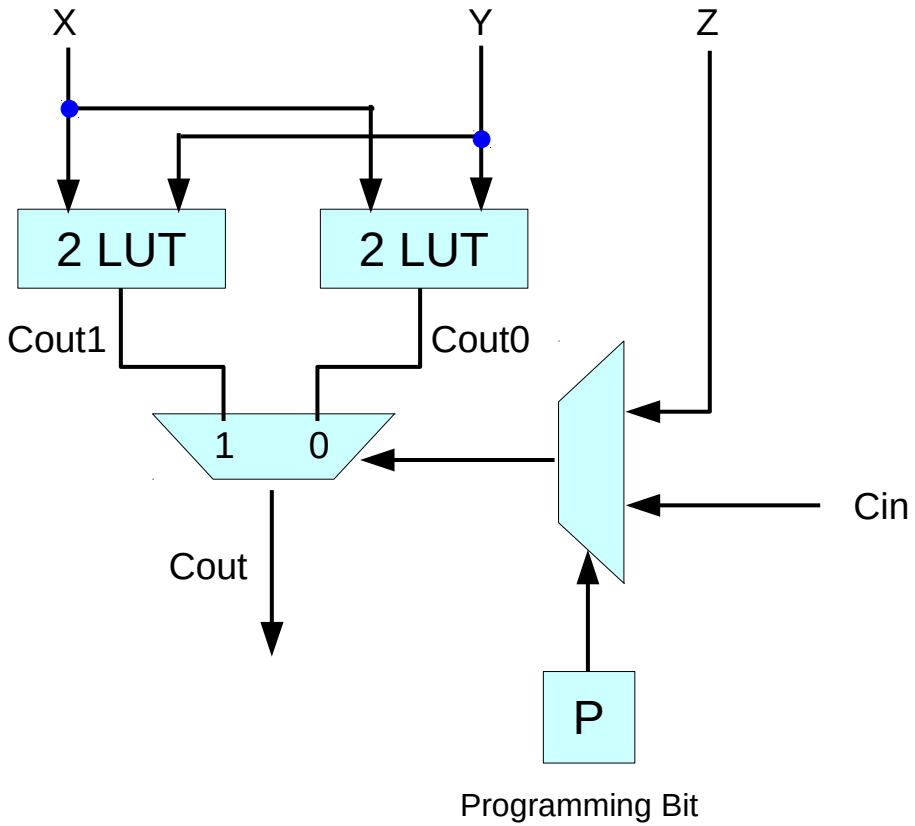
The carry chain is made up of multiplexers
belonging to adjacent configurable blocks

the lookup table is used for implementing the exclusive or function

p(i) = x(i) xor y(i)

https://en.wikipedia.org/wiki/Carry-lookahead_adder

FPGA Carry Chain Cell



Cout1, Cout2 : functions of X, Y, Cin

Cout1 = X+Y when Cin=1
Cout0 = X Y when Cin=0

Cout = (X + Y) Cin + X Y $\overline{Cin}$

Cout = P' Cin + G $\overline{Cin}$ … P' = relaxed P

Cout1	Cout0	Cout	Name
0	0	0	Kill
0	1	$\overline{Cin}$	Inverse Propagate
1	0	Cin	Propagate
1	1	1	Generate

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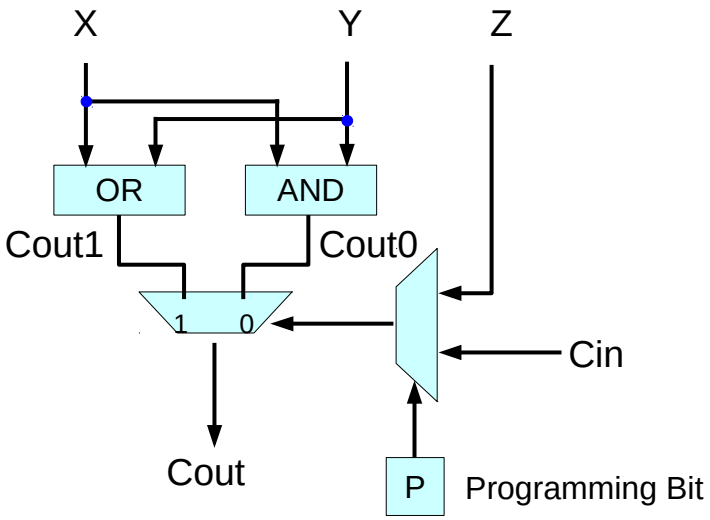
FPGA Carry Chain Cell



X	Y	Cin Cout1	$\overline{Cin}$ Cout0	
0	0	0	0	$\overline{X}\ \overline{Y}$
0	1	1	0	$\overline{X}\ Y$
1	0	1	0	$X\ \overline{Y}$
1	1	1	1	$X\ Y$

Cout : functions of X, Y, Cin

Cout(X, Y, 1) = Cout1 = X + Y
Cout(X, Y, 0) = Cout0 = X Y

Cout1 = X + Y when Cin=1
Cout0 = XY when Cin=0

Cout1 = P' Cin … P' = relaxed P
Cout0 = G $\overline{Cin}$

If Cin, then Cout = ($\overline{X}$ Y + X $\overline{Y}$ + X Y)
If $\overline{Cin}$, then Cout = X Y

Cin (X + Y) + $\overline{Cin}$ X Y
Cin ($\overline{X}$ Y + X $\overline{Y}$ + X Y) + $\overline{Cin}$ X Y
Cin ($\overline{X}$ Y + X $\overline{Y}$) + (Cin + $\overline{Cin}$) X Y
P Cin + G

Cin (X + Y) + $\overline{Cin}$ X Y
Cin P' + $\overline{Cin}$ G … P' : relaxed P

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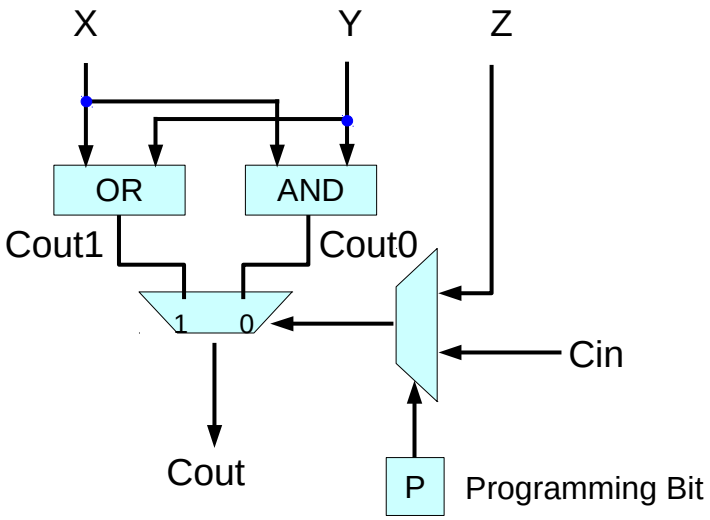
FPGA Carry Chain Cell



X	Y	Cin Cout1	$\overline{Cin}$ Cout0	
0	0	0	0	$\overline{X}\ \overline{Y}$
0	1	1	0	$\overline{X}\ Y$
1	0	1	0	$X\ \overline{Y}$
1	1	1	1	$X\ Y$

X	Y	Cin	Cout	
0	0	0	0	Cout0
0	1	0	0	Cout0
1	0	0	0	Cout0
1	1	0	1	Cout0
0	0	1	0	Cout1
0	1	1	1	Cout1
1	0	1	1	Cout1
1	1	1	1	Cout1

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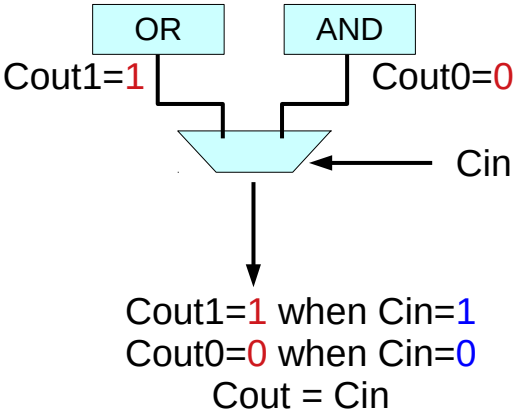
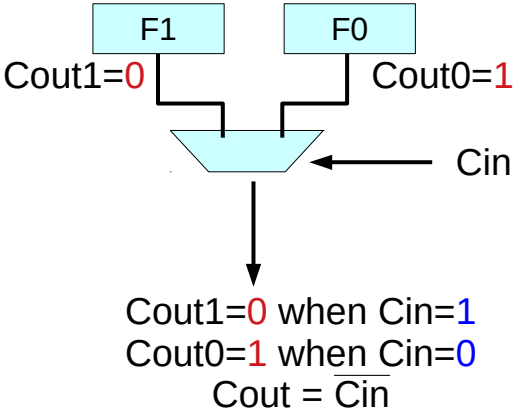
FPGA Carry Chain Cell



Cout0	Cout1	Cout	Name
0	0	0	Kill
0	1	Cin	Propagate
1	0	$\overline{Cin}$	Inverse Propagate
1	1	1	Generate



Cout1	Cout0	Cout	Name
0	0	0	Kill
0	1	$\overline{Cin}$	Inverse Propagate
1	0	Cin	Propagate
1	1	1	Generate

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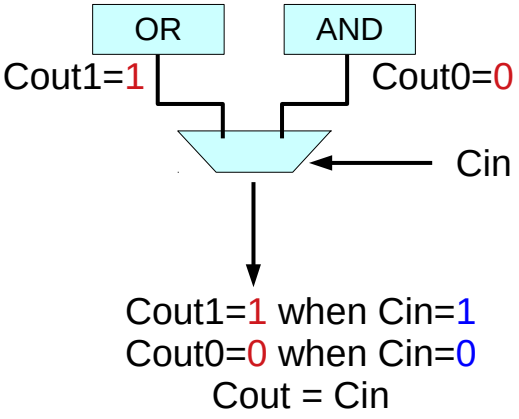

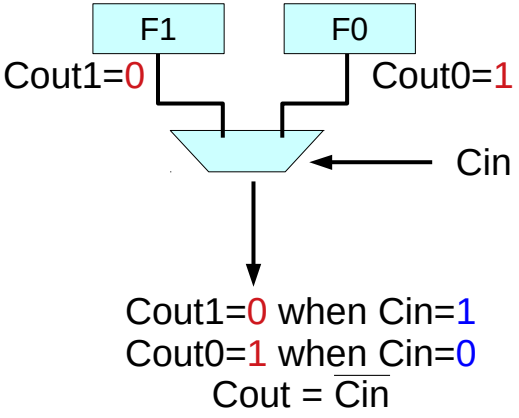

Cout0	Cout1	Cout	Name
0	0	0	Kill
0	1	Cin	Propagate
1	0	$\overline{Cin}$	Inverse Propagate
1	1	1	Generate

X	Y	Cin	Cout		Cout1	Cout0
0	0	0	0	Cout0	0	0
0	1	0	0	Cout0	1	0
1	0	0	0	Cout0	1	0
1	1	0	1	Cout0	1	1
0	0	1	0	Cout1	0	0
0	1	1	1	Cout1	1	0
1	0	1	1	Cout1	1	0
1	1	1	1	Cout1	1	1

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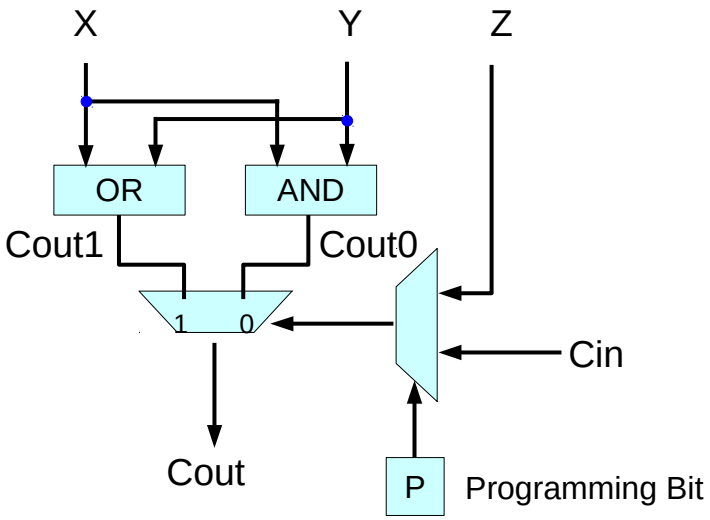
Carry Chain



		Cin	$\overline{Cin}$	
X	Y	Cout1	Cout0	
0	0	0	0	$\overline{X}\ \overline{Y}$
0	1	1	0	$\overline{X}\ Y$
1	0	1	0	$X\ \overline{Y}$
1	1	1	1	$X\ Y$

Cout1	Cout0	Cout	Name
0	0	0	Kill
0	1	$\overline{Cin}$	Inverse Propagate
1	0	Cin	Propagate
1	1	1	Generate

Carry Out

X	Y	Cin	
0	0	Cin	Cin
0	1	Cin	$\overline{Cin}$
1	0	Cin	$\overline{Cin}$
1	1	Cin	Cin

Cout1=1 when Cin=1
Cout0=0 when Cin=0
Cout = Cin propagate

Cout1=0 when Cin=1
Cout0=1 when Cin=0
Cout = $\overline{Cin}$ inverse propagate

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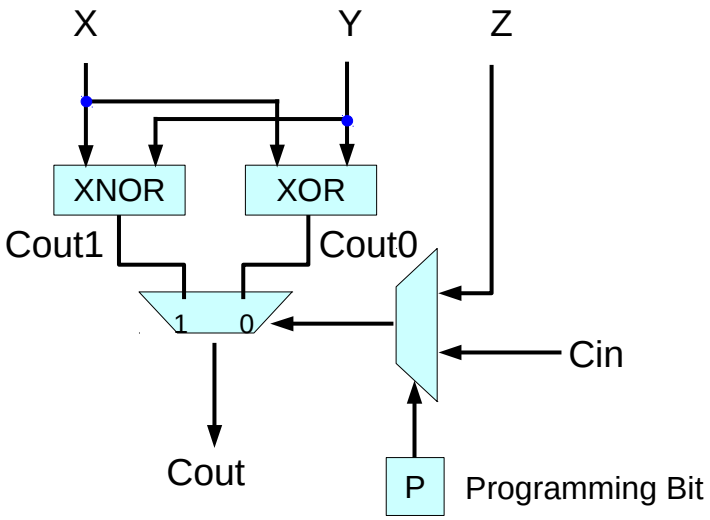
Parity Checker



		Cin	$\overline{Cin}$	
X	Y	Cout1	Cout0	
0	0	1	0	$\overline{X}\ \overline{Y}$
0	1	0	1	$\overline{X}\ Y$
1	0	0	1	$X\ \overline{Y}$
1	1	1	0	$X\ Y$

Cout1	Cout0	Cout	Name
0	0	0	Kill
0	1	$\overline{Cin}$	Inverse Propagate
1	0	Cin	Propagate
1	1	1	Generate

Computing Parity	
X ⊕ Y ⊕ Cin	
0 ⊕ 0 ⊕ Cin	Cin
0 ⊕ 1 ⊕ Cin	$\overline{Cin}$
1 ⊕ 0 ⊕ Cin	$\overline{Cin}$
1 ⊕ 1 ⊕ Cin	Cin

Cout1=1 when Cin=1
Cout0=0 when Cin=0
Cout = Cin propagate

Cout1=0 when Cin=1
Cout0=1 when Cin=0
Cout = $\overline{Cin}$ inverse propagate

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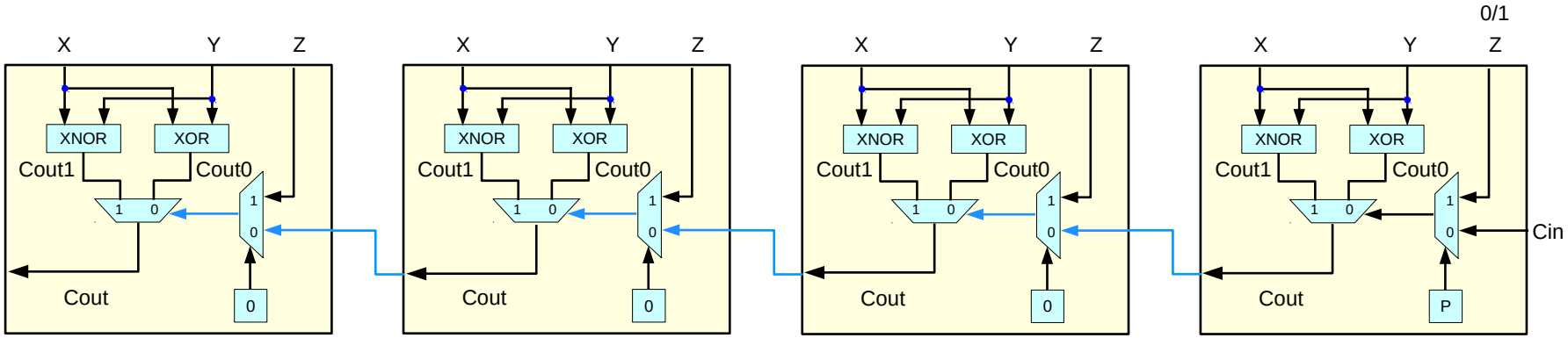
Ripple Carry Chain



the **first cell** in the chain

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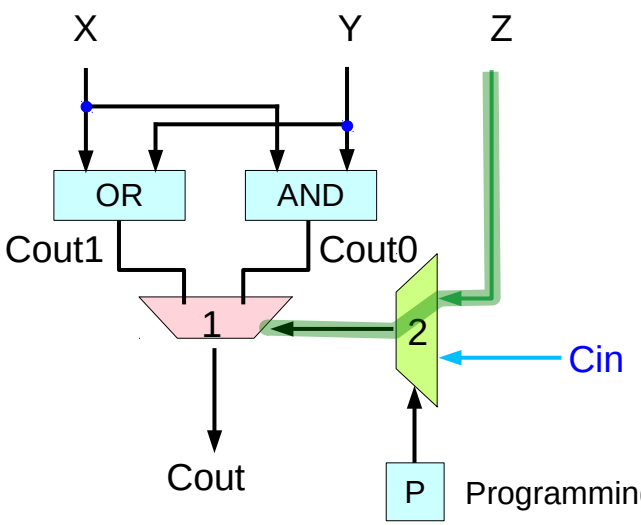
FPGA Carry Chain Cell



when Cin is ignored,
Z is routed to mux1

- used in combined adder/subtractors
- must be ignored, otherwise

the logic cells - resources to compute a function
the exact location of logic cells depends on the user.
a user can start or end a carry computation
at any place in an fpga.

But in many carry computations,
the first cell has only 2 inputs,
and forcing the carry chain
to wait for the arrival of an additional,
unnecessary input Z will only needlessly
slow down the circuit's computation.

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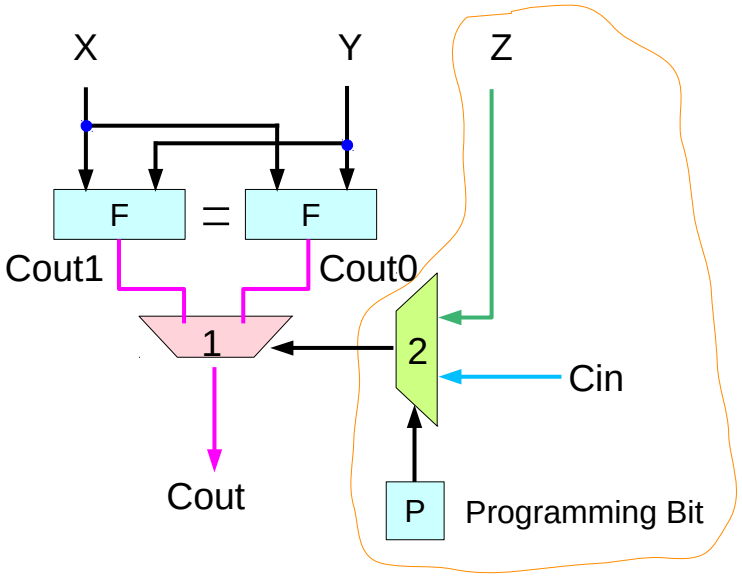
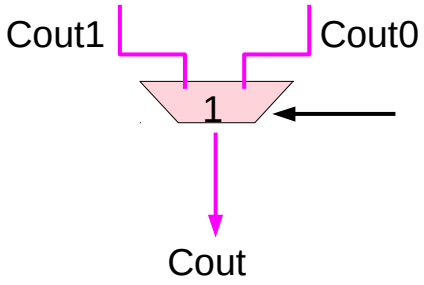
FPGA Carry Chain Cell



when Cin is ignored,
Z can also be ignored
by having the same LUTs



the **first cell** in the chain

the same LUTs

the same output
regardless of Z and Cin

Cout1 = Cout0 = Cout
regardless of the select

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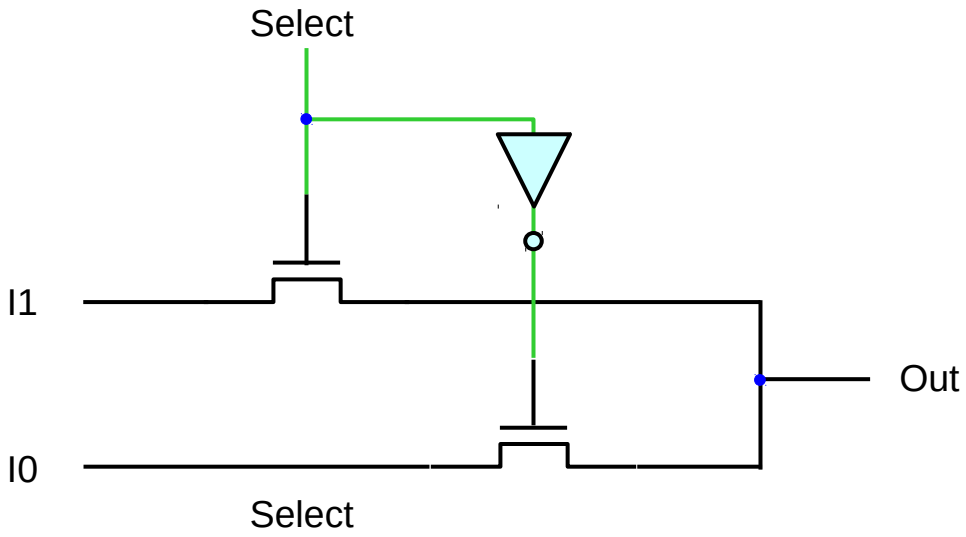
Ripple Carry Chain



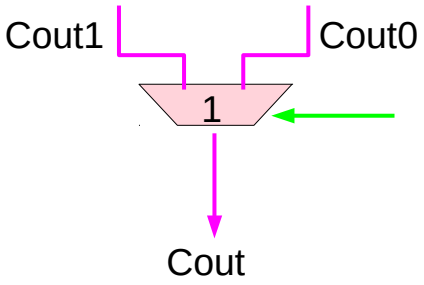


fig1b shows an implementation of a mux that does not obey this requirement

since the carry chain is part of an fpga,
the input to this mux could be connected to some unused logic in another row which is generating unknown values.

if that unused logic had multiple transitions which caused the signal to change quicker than the gate could react,
then it is possible that **the select signal** to this mux could be stuck midway between true and false (2.5V for 5V CMOS)

in this case, it will not be able to pass a true value from the input to the output
and thus will not function properly for this application.

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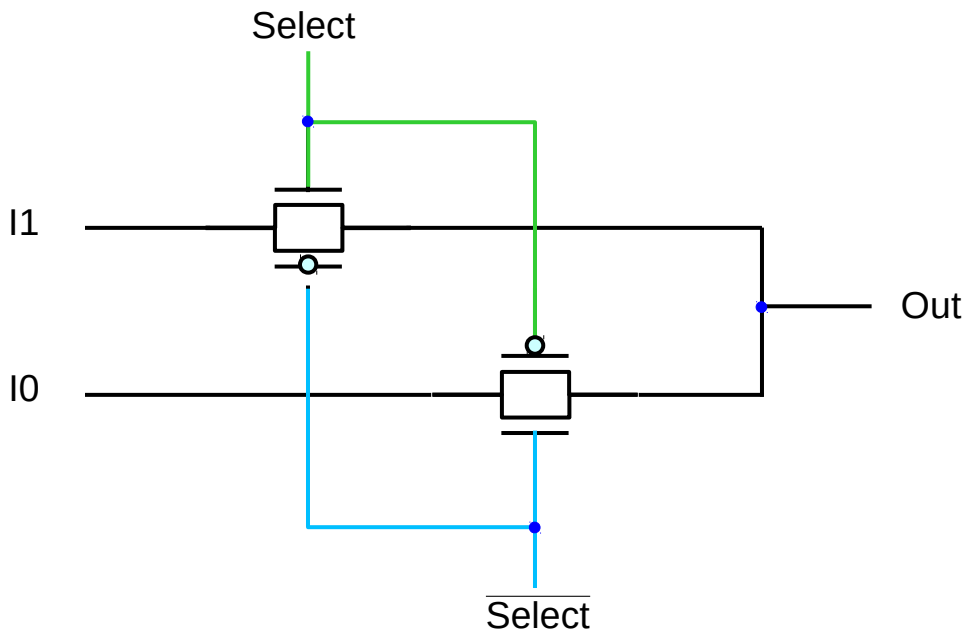
Ripple Carry Chain



however a mux built with
both n-transistor and p-transistor pass gates
will operate properly for this case

assume this mux implementation will be used

tristate driver based muxes could be used,
which restore signal drive and cut series RC chains

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Unit Gate Delay Model

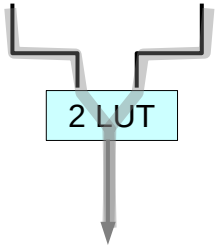
All simple gate of two or three inputs
that are directly implementable
in one logic level in CMOS
are considered to have a delay of one.

All other gate must be implemented by such gates,
and have the delay of the underlying circuit.

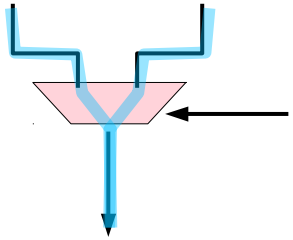
Delay of one
- inverters and
- 2 to 3 input NAND
- 2 to 3 input NOR gates

A 2:1 mux has a delay of one
from the I0 or I1 inputs to the output,
But has a delay of two
from the select input to the output
due to the Inverter delay

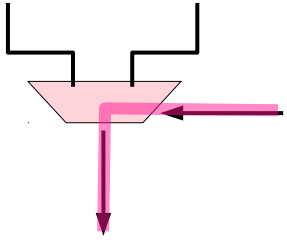
Delay of zero (constant delay)
- the delay of the 2-LUTs,
- any routing leading to them,



Delay of **0**



Delay of **1**



Delay of **2**

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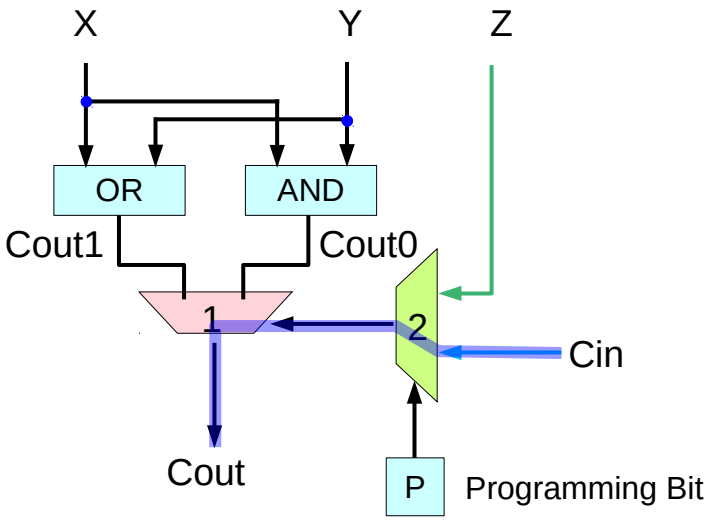
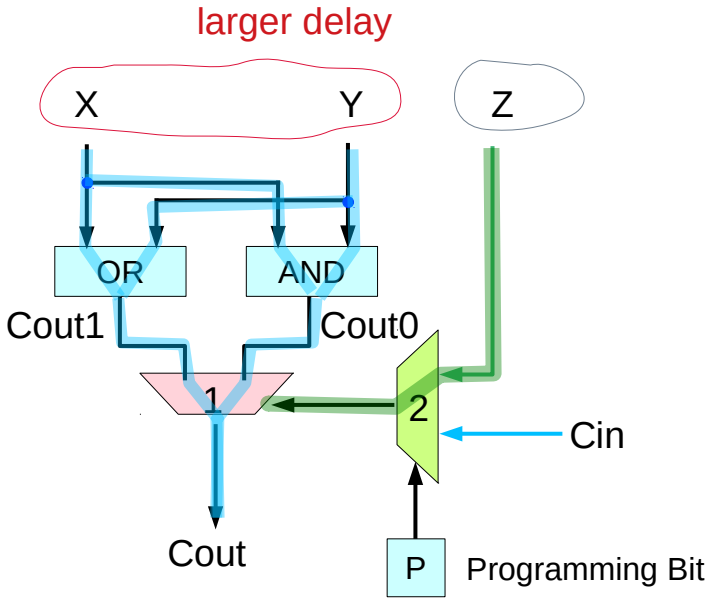
FPGA Carry Chain Cell



Delay 3



Delay 1

Significantly slower
two muxes on the carry chain in each cell

Delay 1 for first cell
Delay 3 for each additional cell in the carry chain
delay 1 for mux2
delays 2 for mux1

Overall 3n-2 for an n-cell carry chain

The critical path comes from the 2-LUTs
and not from the input Z
since the delay through the 2-LUTs
will be larger than through mux 2 in the first cell

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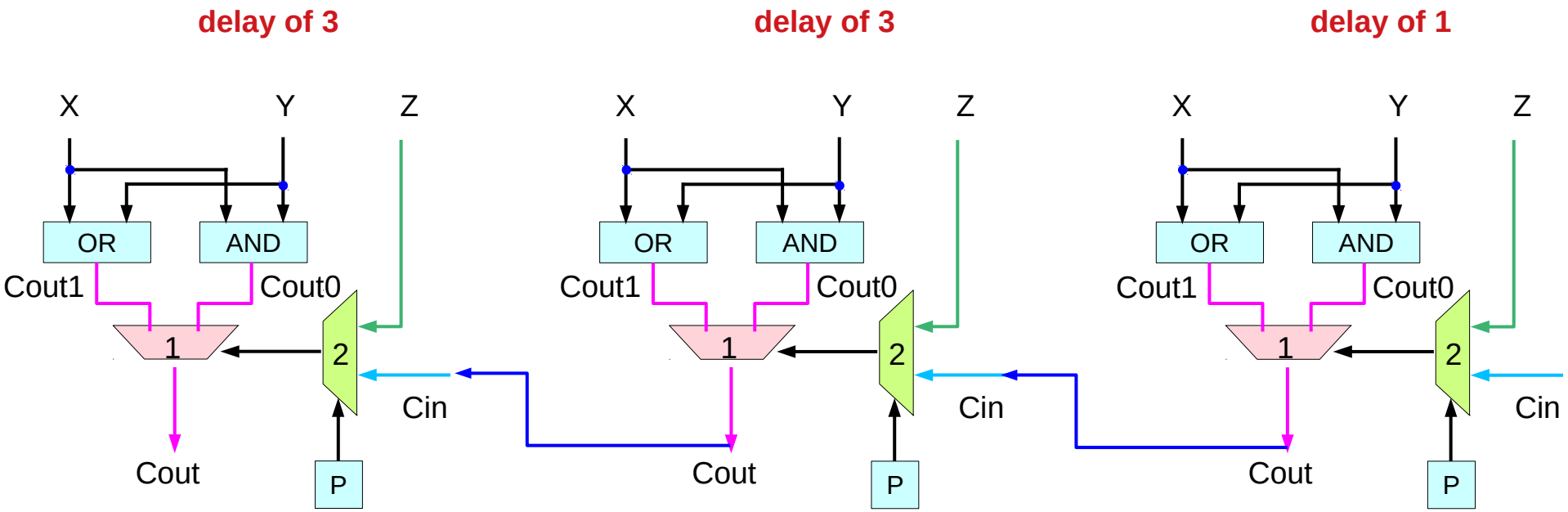
FPGA Carry Chain Cell



delay of 3n-2 for an n-bit ripple carry chain

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FPGA Carry Chain Cell

the linear delay growth of ripple carry adders

optimize a ripple carry chain structure for use in FPGAs

while this provides some performance gain
over the basis ripple carry scheme
found in many current FPGAs,

still much slower than what is done in custom logic

advanced adder techniques in custom logic
can be integrated into reconfigurable logic

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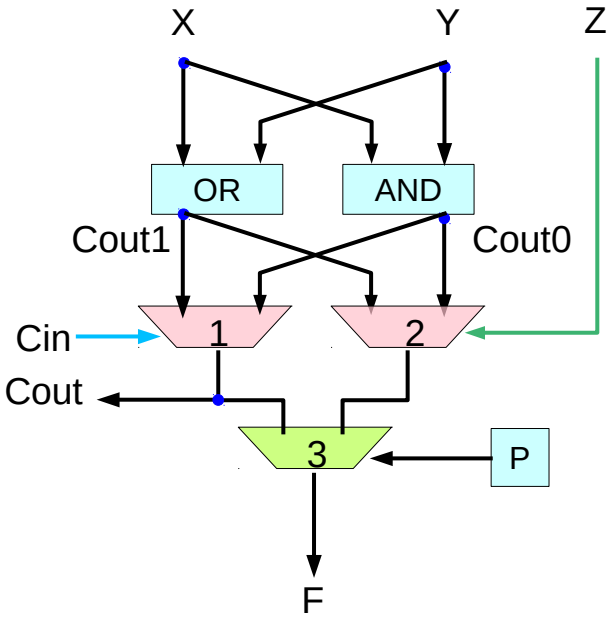
FPGA Carry Chain Cell

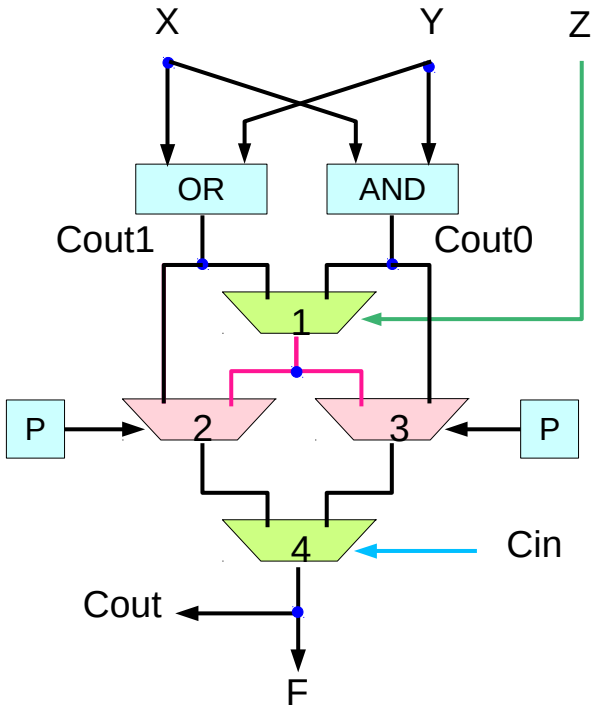
Design A

2n / 2n+2



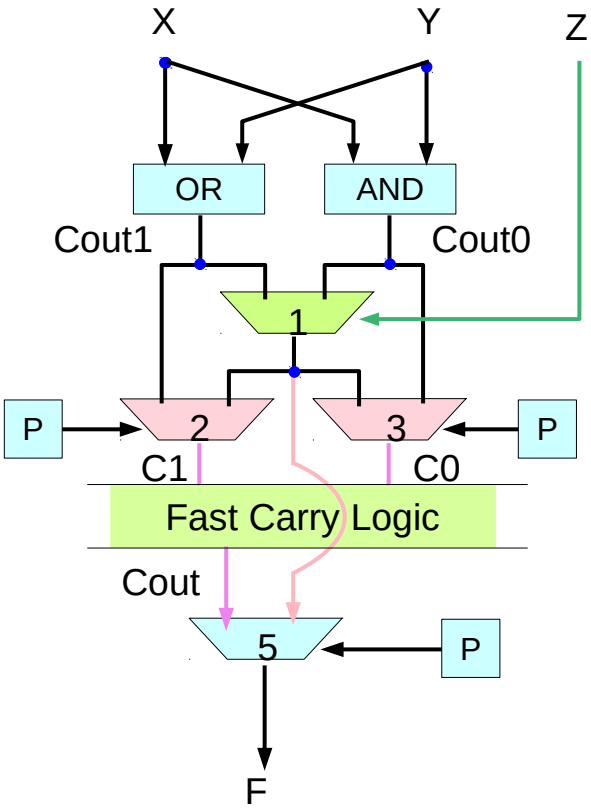
Design B

2n / 2n+1



Design C

2n+2



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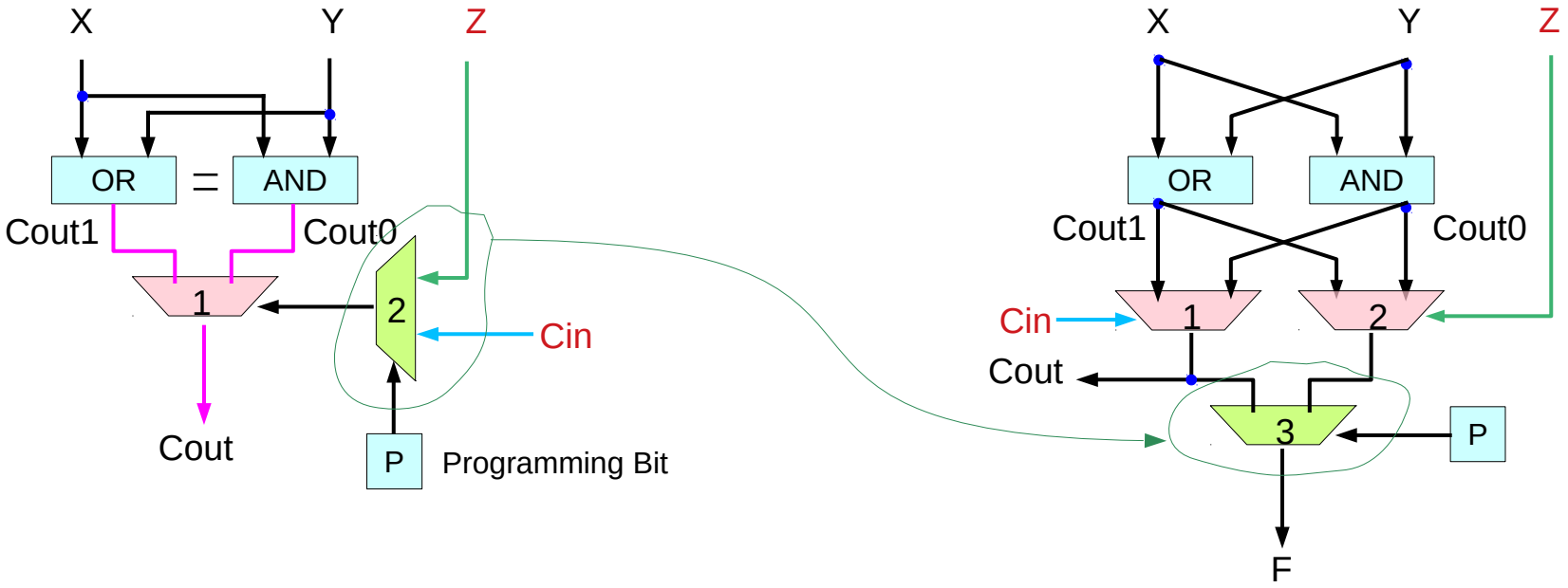
Design A (1)

to reduce the delay of the ripple carry chain
- remove mux2 from the carry path.
- no need to choose between Cin and Z for the select line to the output mux1

- two separate muxes, mux1 and mux2, controlled by Cin and Z, respectively.
- the circuit chooses between these outputs with mux3.



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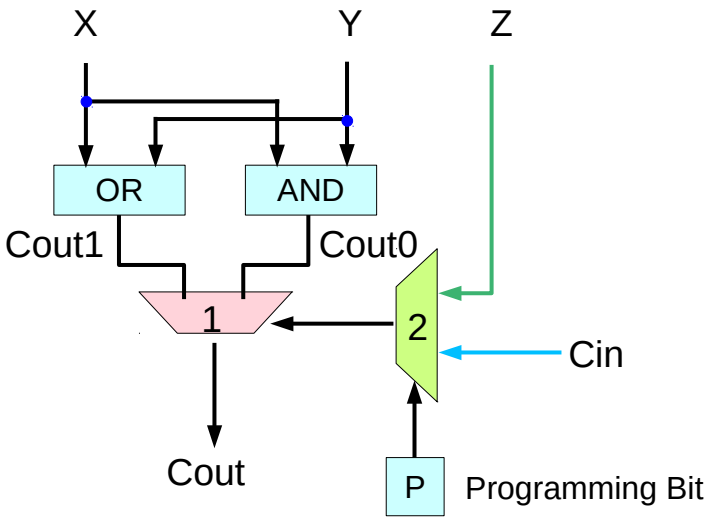
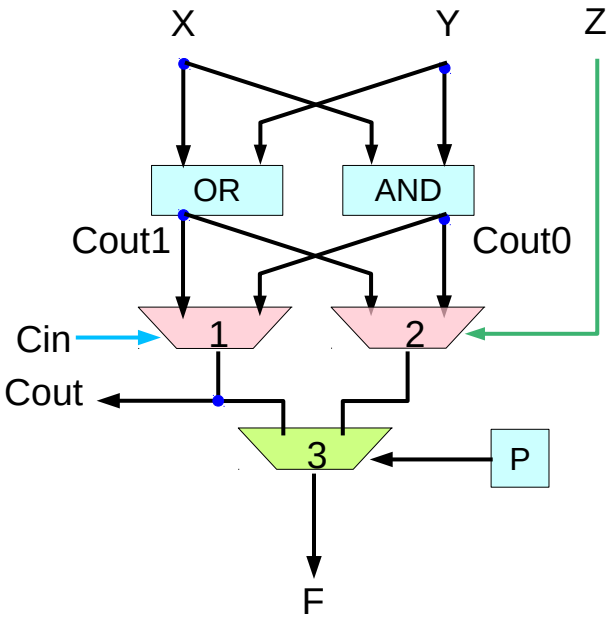
Design A (2)





- not logically equivalent
- the Z input in the first cell cannot be used
  - Z is only attached to mux2
  - mux2 does not lead to the carry cells
  - not connected to Cout

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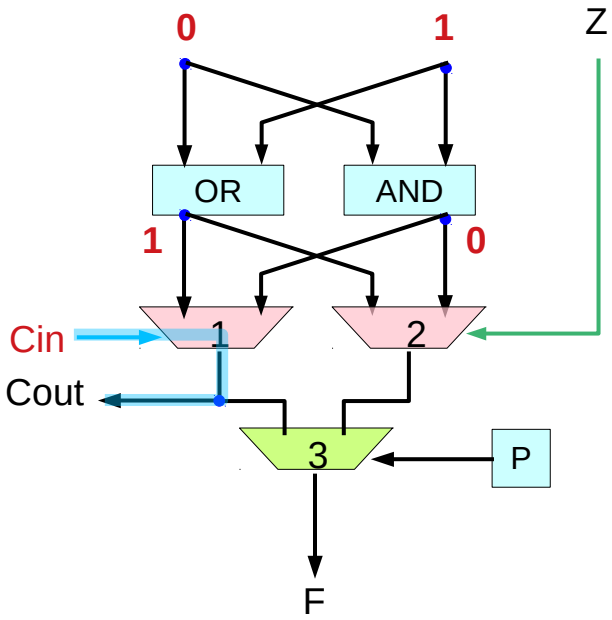
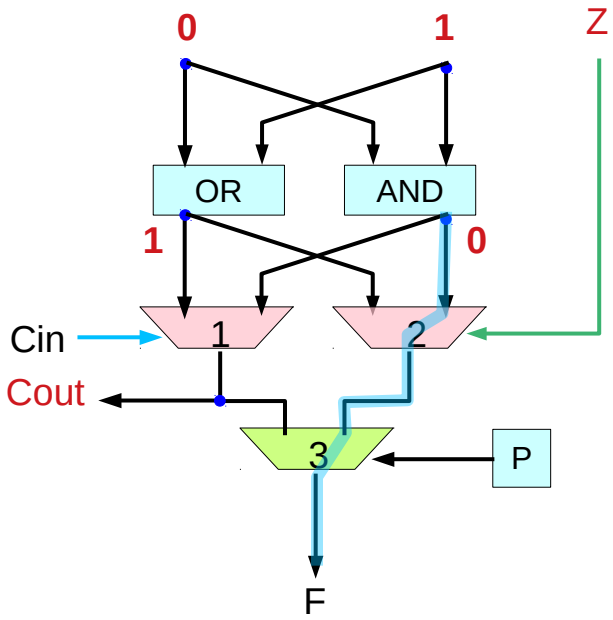
Design A (3)

delay of 2



an additional cell
for generating Cin

delay of 2



- need an additional cell to use Z as a carry input

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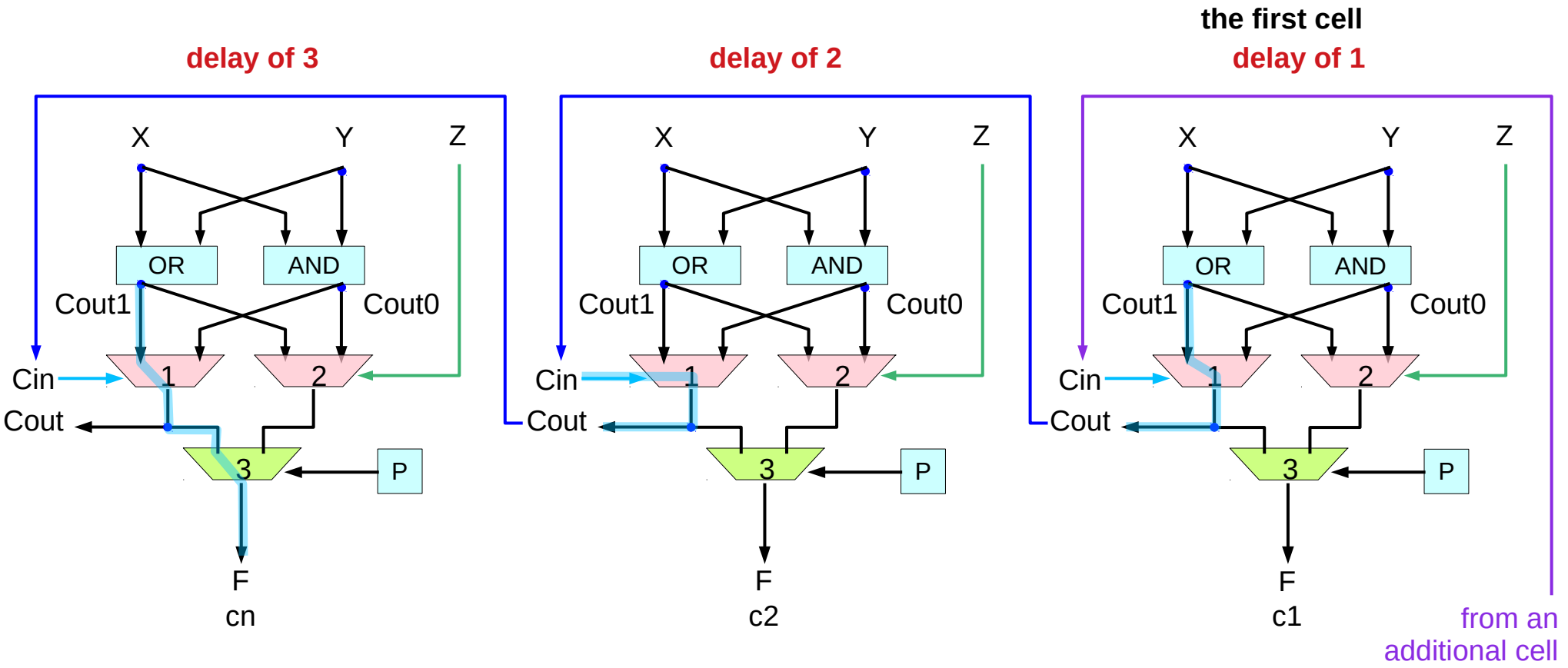
Design A (4)



(2 for mux1, 1 for mux3)

50% faster circuit that the original design

delay of 2n for an n-bit ripple carry chain

delay of 2(n+1)

without a carry input Z

with a carry input Z

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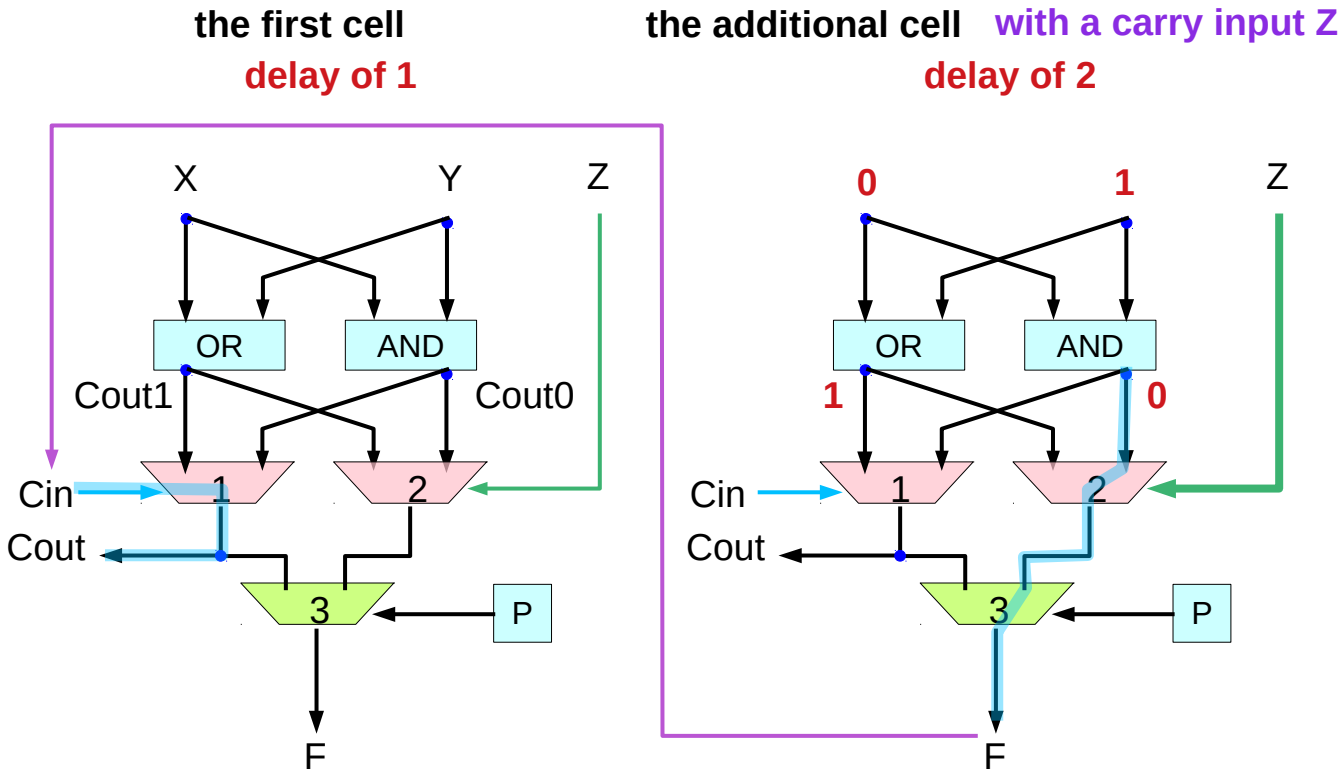
Design A (5)



delay of 2(n+1) for an n-bit ripple carry chain with a carry input

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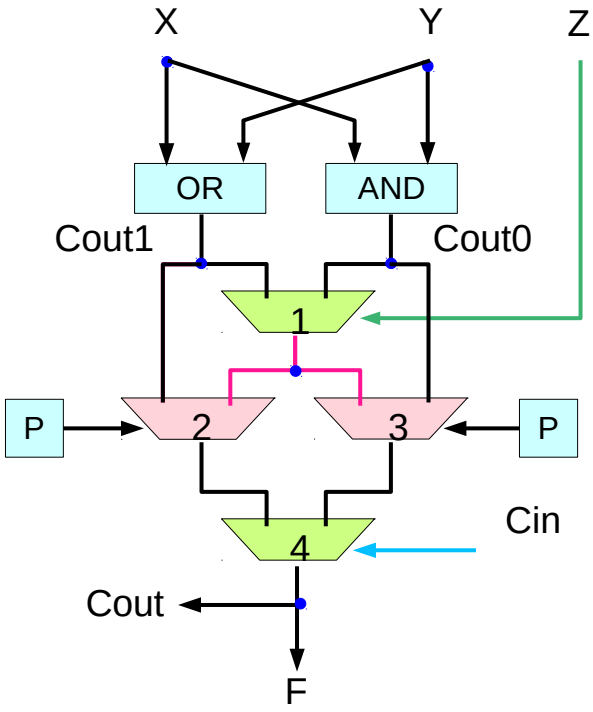
Design B (1)

although this design is 1 gate delay slower than that of fig 2a,
it provides the ability to have a carry input
to the first cell in a carry chain,
something that is important in many computations.

Also, for carry computations that do not need this feature,
without a carry input
the first cell in a carry chain built from fig 2b
can be configured to bypass mux1,
reducing the overall delay to 2n,
which is identical to that of fig2a.



(2 for mux1, 1 for mux3)

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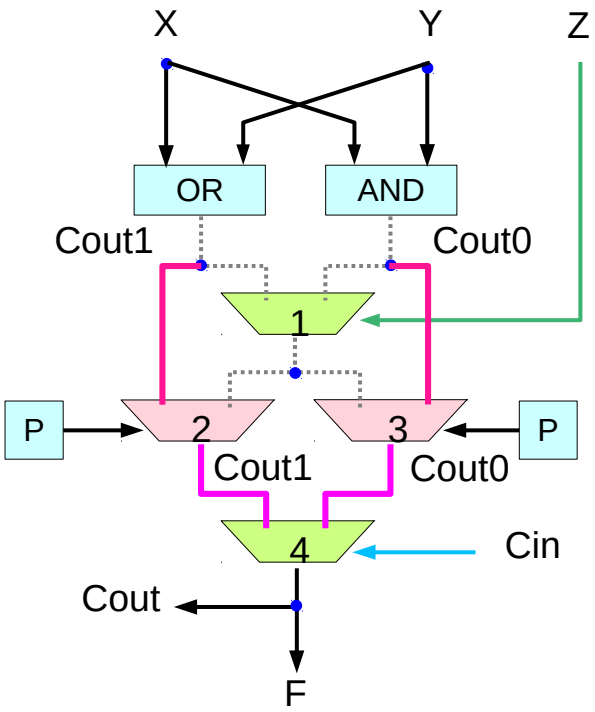
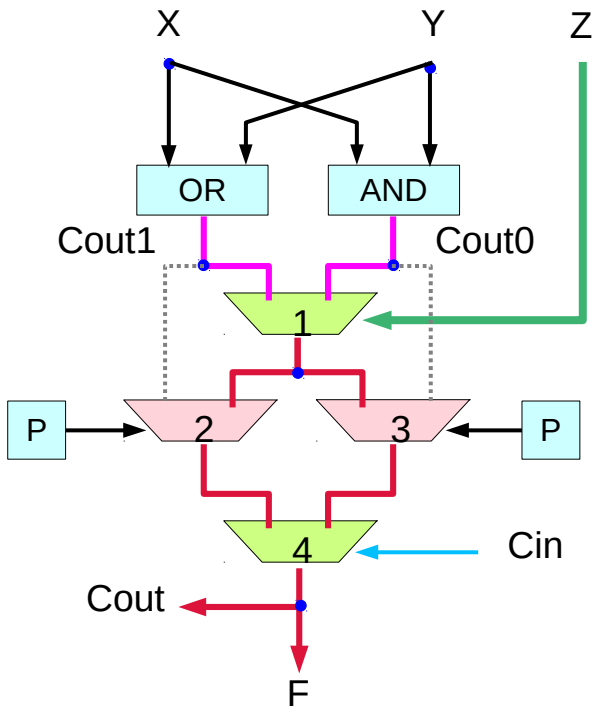
Design B (2)

the other cells



for cells in the middle of a carry chain
mux2 passes Cout1
mux3 passes Cout0
mux4 receives Cout1 and Cout0
provides a standard ripple carry path.

the first cell carry input



For the first cell in a carry chain
with a carry input (provided by input Z),
mux2 and mux3 both pass the value from mux1

the two main inputs to mux4 are identical
the output of mux4 (Cout) will be the same
as the output of mux1 (ignoring Cin)

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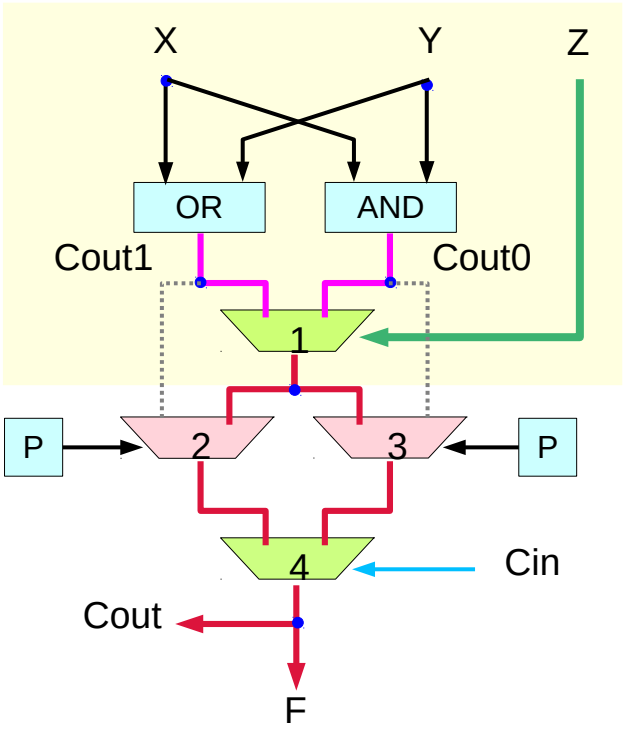
Design B (3)

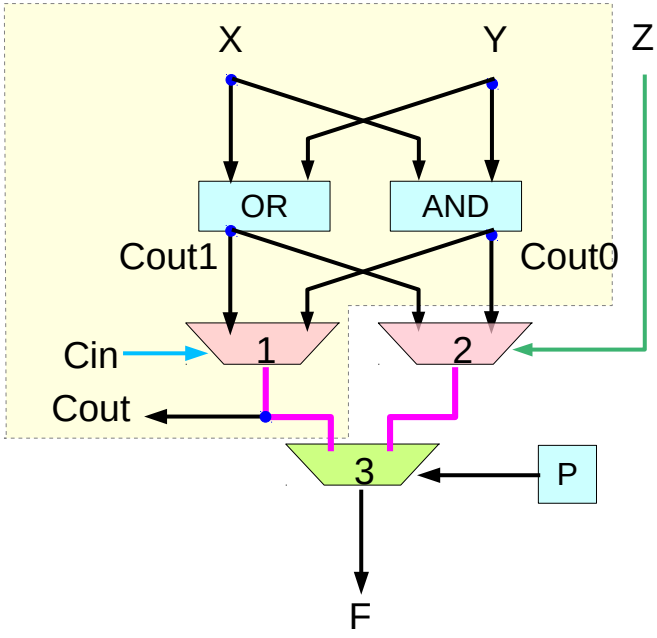
the first cell carry input



mux1's main inputs are driven
by two 2-LUTs (OR, AND) controlled by X and Y
mux1 forms a **3-LUT** with the other 2-LUTs

When mux2 and mux3 pass the value from mux1
(Cout1 and Cout2 respectively)
the circuit is configured to continue the carry chain

Functionally equivalent



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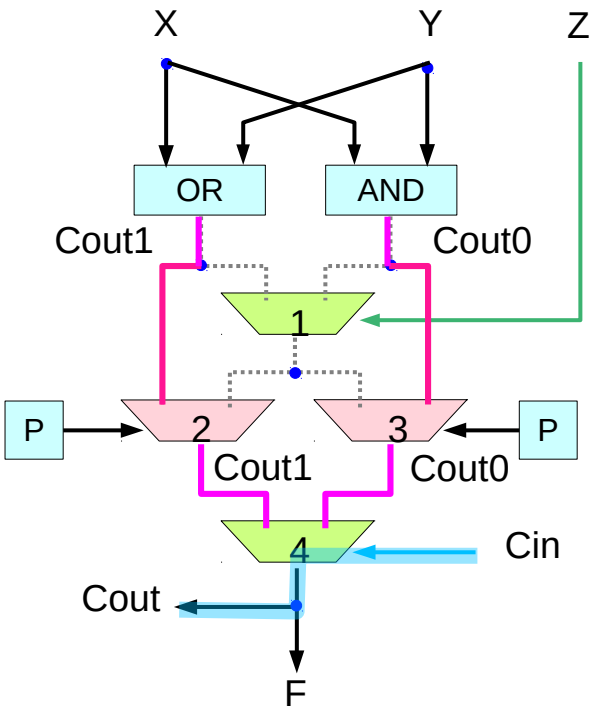
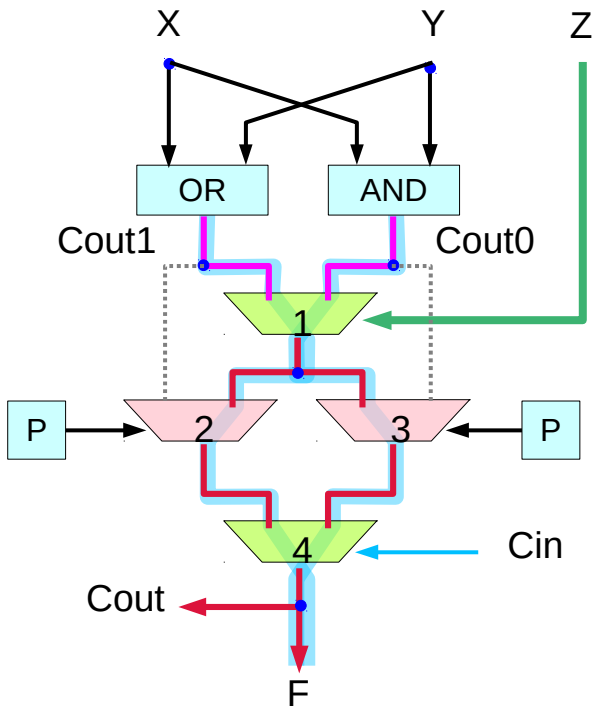
Design B (4)

delay of 2 **the other cells**



delay of 3 **the first cell** **with a carry input**



A delay of 2 in all other cells
except the first cell in the carry chain

an total delay of **2n+1** for an n-bit carry chain
when a carry input to the first cell is enabled

1 gate delay slower than that of fig 2a,

a delay of 3 in the first cell
1 in mux1, 1 in mux2, 1 in mux4

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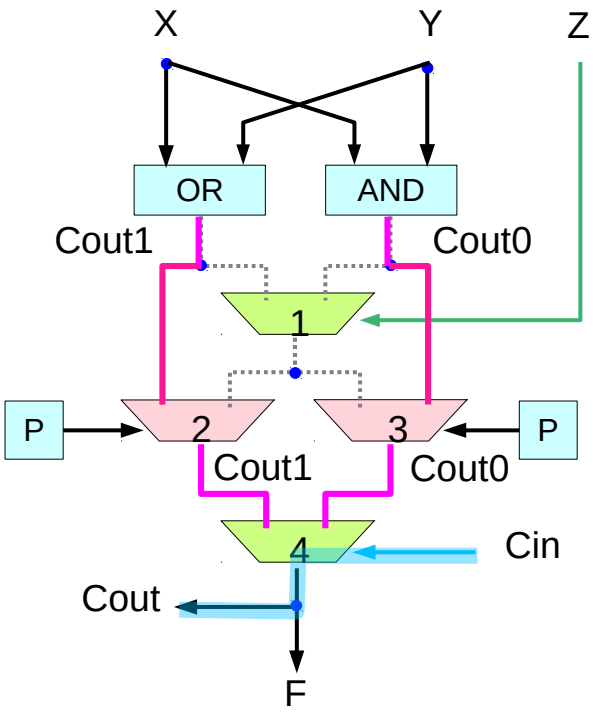
Design B (5)

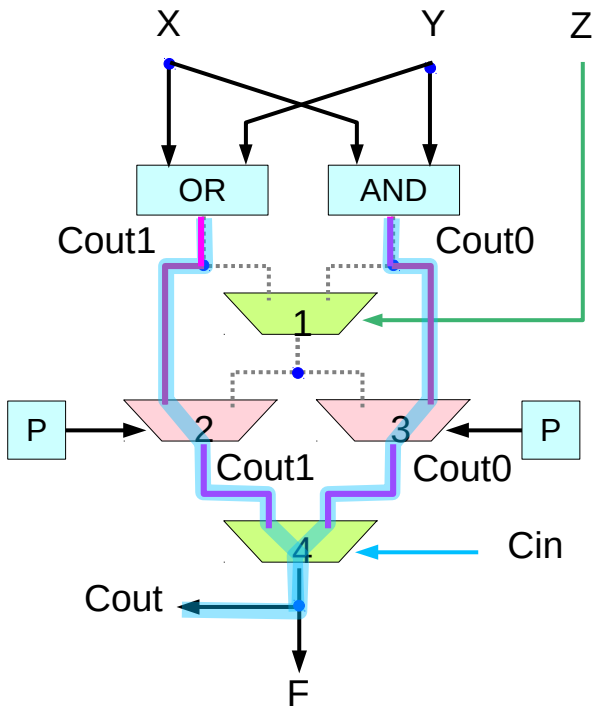
delay of 2 **the other cells**



A delay of 2 in all other cells
except the first cell in the carry chain

an total delay of **2n** for an n-bit carry chain
when a carry input to the first cell is disabled

delay of 2 **the first cell without a carry input**



a delay of 2 in the first cell
when a carry input is not used

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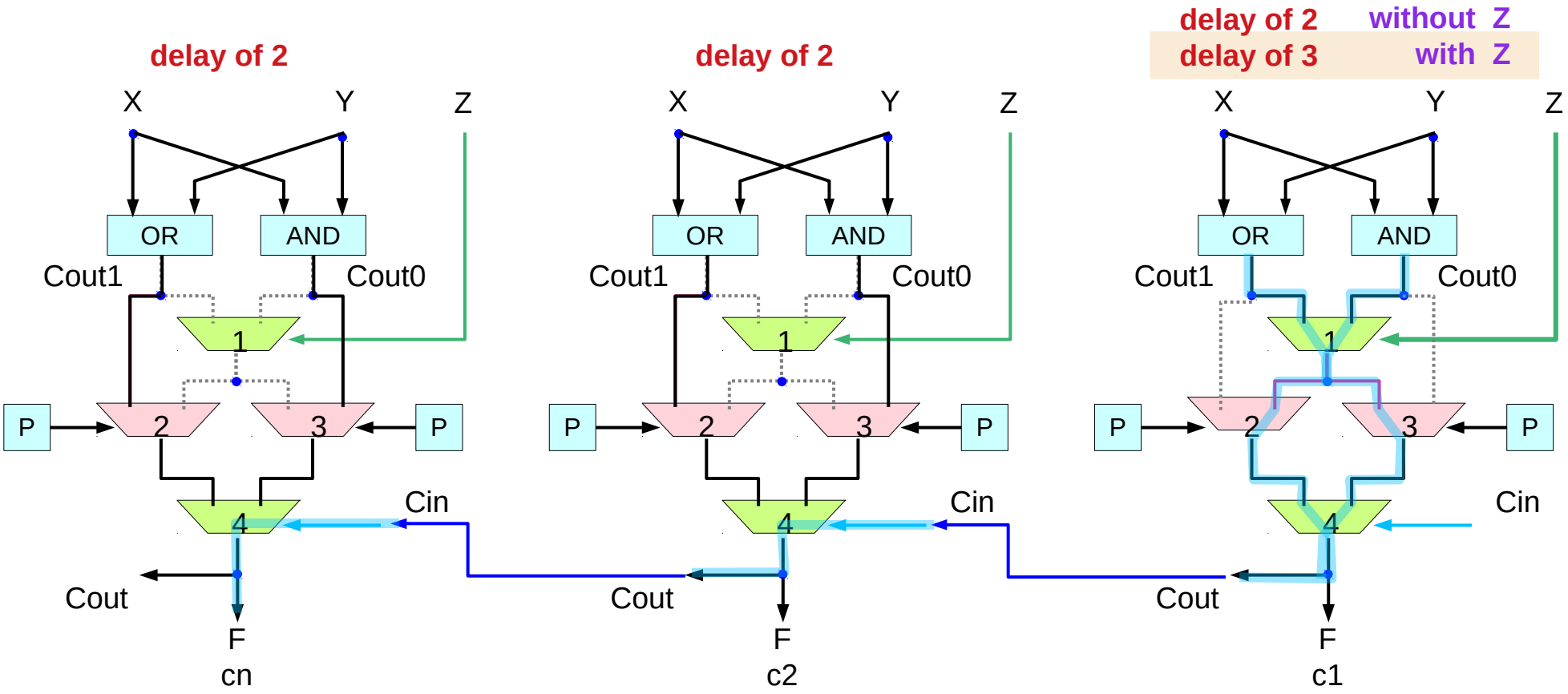
Design B (6)



delay of 2n for an n-bit ripple carry chain **without a carry input Z**

delay of 2n+1 **with a carry input Z**

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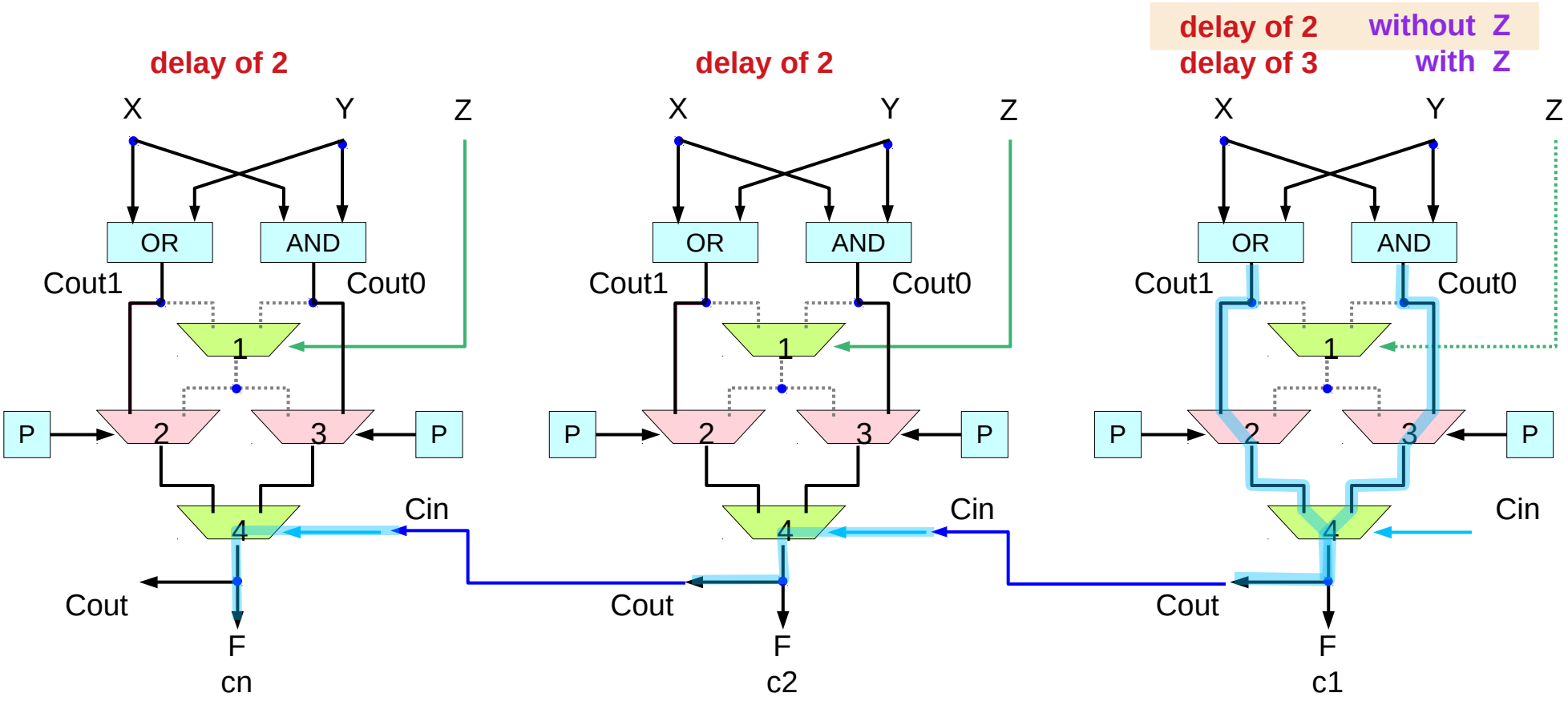
Design B (7)



delay of 2n for an n-bit ripple carry chain **without a carry input Z**

delay of 2n+1 **with a carry input Z**

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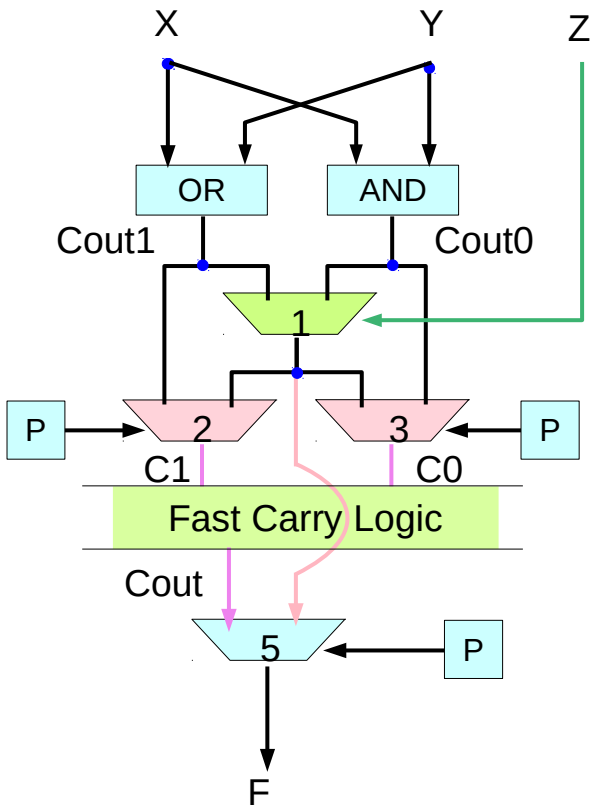
Design C (1)

the actual carry chain (mux4) in Design B has been replaced by
- an abstract fast carry logic unit
- mux5 has been added

to the abstract fast carry logic units, various high performance carry chains can be applied

mux5 is present because
- significant delay for non-carry computations
- much faster carry propagation for long carry chains

when used as a simple normal **3 LUT**, using inputs X, Y, and Z
mux5 allows us to bypass the carry chain by selecting the output of mux1



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Design C (2)

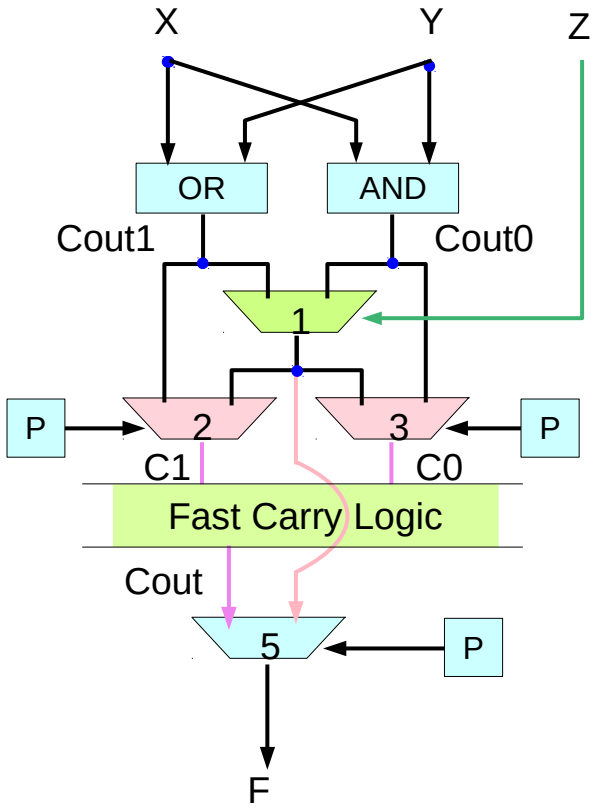
All the developed fast carry logic units in Design C
that can compute the following value,
can provide the functionality necessary
to support the needs of FPGA carry chain computations

$$Cout_i = (Cout_{i-1} \cdot C1_i) + (\overline{Cout_{i-1}} \cdot C0_i)$$

where *i* is the position of the cell within the carry chain,

thus, the fast carry logic unit can contain
any logic structure implementing this equation
(including Brent-Kung), Variable Bit, and Ripple Carry.

Note that because of the needs and requirements of
carry chains for FPGAs, new circuits are developed,
by utilizing the standard adder structures,
but which are more appropriate for FPGAs



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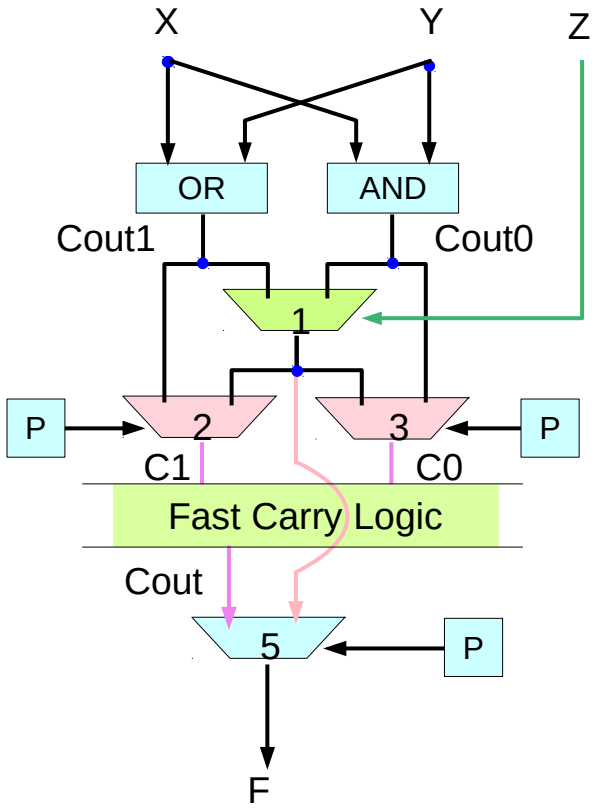
Design C (3)

the main difference is to support all states
- Generate
- Propagate
- Kill
- Inverse Propagate

These 4 states are encoded
on signals C1 and C0

Also, while standard adders are concerened
only with the maximum delay
through an entire n-bit adder structure,
the delay concerns for FPGAs
are more complicated

Specifically, when an n-bit carry chain is built into
the architecture of an FPGA
it does not represent an actual computation,
but only the potential for a computation.



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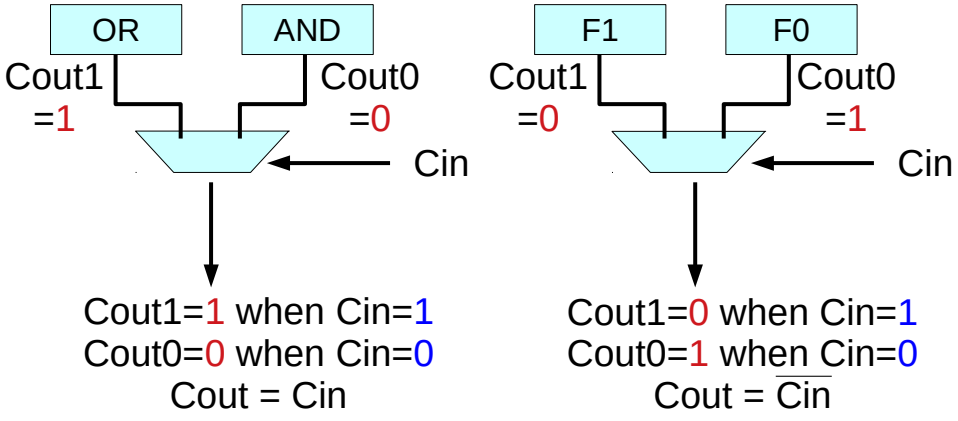
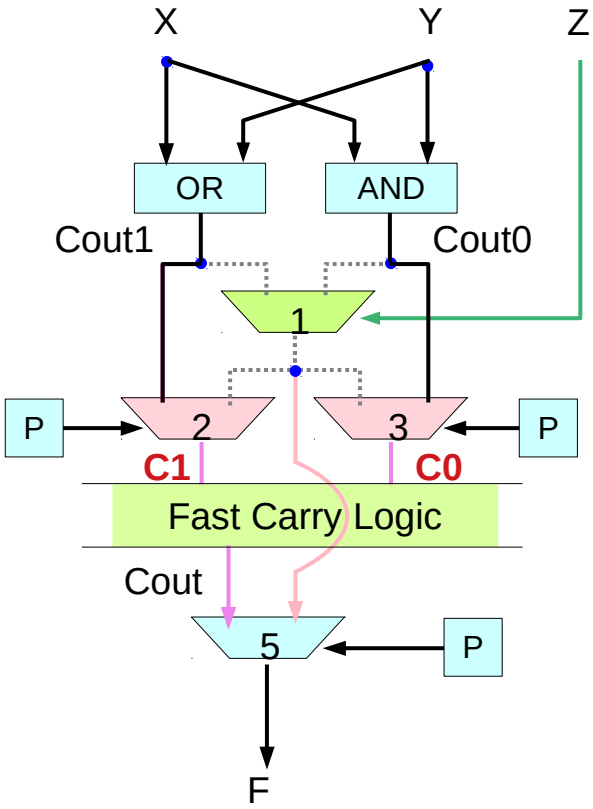
Design C (4)

		Cin	$\overline{Cin}$	
X	Y	Cout1	Cout0	
0	0	0	0	$\overline{X}\ \overline{Y}$
0	1	1	0	$\overline{X}\ Y$
1	0	1	0	$X\ \overline{Y}$
1	1	1	1	$X\ Y$

Cout1	Cout0	Cout	Name
0	0	0	Kill
0	1	$\overline{Cin}$	Inverse Propagate
1	0	Cin	Propagate
1	1	1	Generate



C1	C0		Name
0	0	0	Kill
0	1	$\overline{Cin}$	Inverse Propagate
1	0	Cin	Propagate
1	1	1	Generate



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Design C (5)

X	Y	C1	C0	
0	0	0	0	$\overline{X}\ \overline{Y}$
0	1	1	0	$\overline{X}\ Y$
1	0	1	0	$X\ \overline{Y}$
1	1	1	1	$X\ Y$

$$C1_i = X_i + Y_i$$
$$C0_i = X_i \cdot Y_i$$

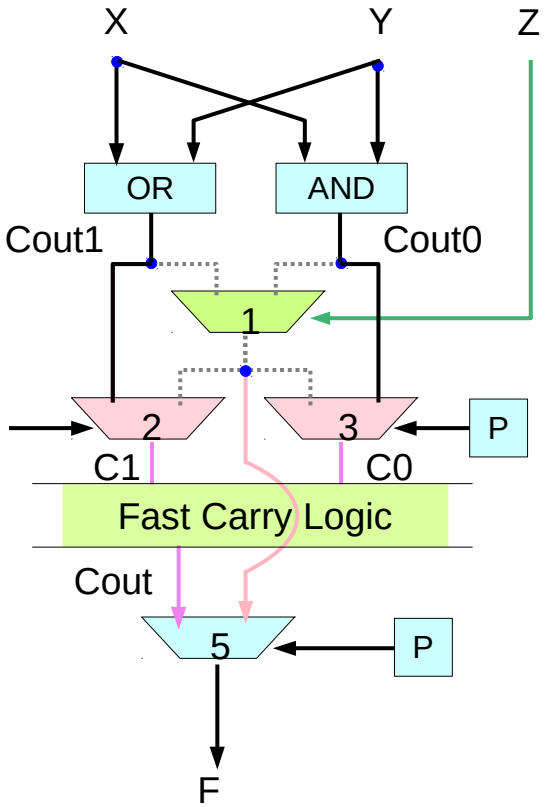
C1	C0		Name
0	0	0	Kill
0	1	Cin	Inverse Propagate
1	0	Cin	Propagate
1	1	1	Generate

$$Cout_i = (Cout_{i-1} \cdot C1_i) + (\overline{Cout_{i-1}} \cdot C0_i)$$

$$(Cout_{i-1} \cdot C1_i) = Cout_{i-1} \cdot (\overline{X}\,Y + X\,\overline{Y} + X\,Y)$$

$$(\overline{Cout_{i-1}} \cdot C0_i) = \overline{Cout_{i-1}} \cdot X\,Y$$

X	Y	$Cout_i$	$Cout_{i+1}$
0	0	0	0
0	1	0	0
1	0	0	0
1	1	0	1
0	0	1	0
0	1	1	1
1	0	1	1
1	1	1	1



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Design C (6) – Complements of C0 and C1

$C1 = \bar{X}Y + X\bar{Y} + XY$

X	Y	C1
0	0	0
0	1	1
1	0	1
1	1	1

$C0 = XY$

X	Y	C0
0	0	0
0	1	0
1	0	0
1	1	1

$C1 = \bar{X}Y + X\bar{Y} + XY$

$C0 = XY$

$\overline{C1} = \bar{X}\bar{Y}$

X	Y	$\overline{C1}$
0	0	0
0	1	1
1	0	1
1	1	1

$\overline{C0} = \bar{X}Y + X\bar{Y} + \bar{X}\bar{Y}$

X	Y	$\overline{C0}$
0	0	0
0	1	1
1	0	1
1	1	1

$\bar{C}1 = \overline{(\bar{X}Y) + (X\bar{Y}) + (XY)} = \bar{X}\bar{Y}$

$\bar{C}0 = \bar{X} + \bar{Y} = \bar{X}Y + X\bar{Y} + \bar{X}\bar{Y}$

$$Cout_3 = (Cout_1 \cdot (C1_3 \cdot C1_2 + C0_3 \cdot \overline{C1_2})) + (\overline{Cout_1} \cdot (C1_3 \cdot C0_2 + C0_3 \cdot \overline{C0_2}))$$

$$= (Cout_1 \cdot (C1_3 \cdot (\bar{X}_2Y_2 + X_2\bar{Y}_2 + X_2Y_2) + C0_3 \cdot \bar{X}_2\bar{Y}_2)) + (\overline{Cout_1} \cdot (C1_3 \cdot X_2Y_2 + C0_3 \cdot (\bar{X}_2Y_2 + X_2\bar{Y}_2 + \bar{X}_2\bar{Y}_2)))$$

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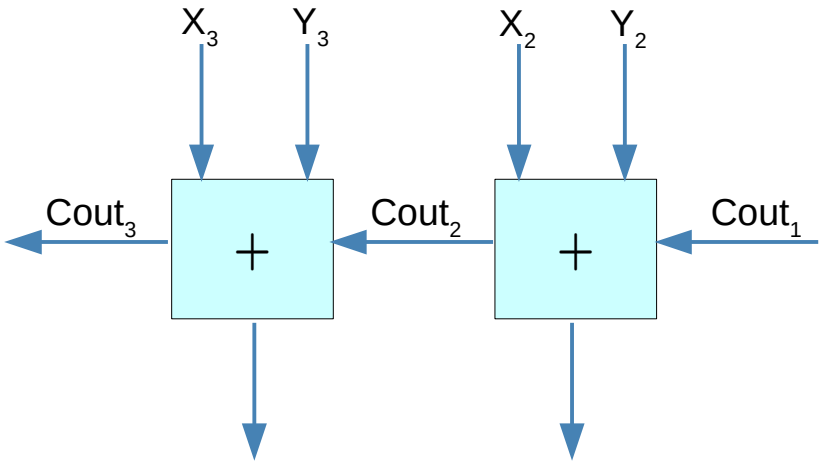
Design C (7) – $Cout_3$ in terms of $Cout_1$

X_3	Y_3	X_2	Y_2	$Cout_2$	$Cout_3$	Cout3
0	0	0	0	0	0	0
0	0	0	1	$Cout_1$	0	0
0	0	1	0	$Cout_1$	0	0
0	0	1	1	1	0	0
0	1	0	0	0	$Cout_3$	0
0	1	0	1	$Cout_1$	$Cout_3$	$Cout_1$
0	1	1	0	$Cout_1$	$Cout_3$	$Cout_1$
0	1	1	1	1	$Cout_3$	1
1	0	0	0	0	$Cout_3$	0
1	0	0	1	$Cout_1$	$Cout_3$	$Cout_1$
1	0	1	0	$Cout_1$	$Cout_3$	$Cout_1$
1	0	1	1	1	$Cout_3$	1
1	1	0	0	0	1	1
1	1	0	1	$Cout_1$	1	1
1	1	1	0	$Cout_1$	1	1
1	1	1	1	1	1	1

$$Cout_3 = (Cout_1 \cdot (C1_3 \cdot C1_2 + C0_3 \cdot \overline{C1_2})) + (\overline{Cout_1} \cdot (C1_3 \cdot C0_2 + C0_3 \cdot \overline{C0_2}))$$



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Design C (8) – $Cout_3$ in terms of $Cout_1$

X_3 Y_3	X_2 Y_2	$C1_3$	$C0_3$	$C1_2$	$C0_2$	$Cout_1$ $C1_3C1_2$	$Cout_1$ $C0_3\overline{C1}_2$	$\overline{Cout}_1$ $C1_3C0_2$	$\overline{Cout}_1$ $C0_3\overline{C0}_2$	$Cout^3$
0 0	0 0	0	0	0	0	0	0	0	0	0
0 0	0 1	0	0	1	0	0	0	0	0	0
0 0	1 0	0	0	1	0	0	0	0	0	0
0 0	1 1	0	0	1	1	0	0	0	0	0
0 1	0 0	1	0	0	0	0	0	0	0	0
0 1	0 1	1	0	1	0	1	0	0	0	$Cout_1$
0 1	1 0	1	0	1	0	1	0	0	0	$Cout_1$
0 1	1 1	1	0	1	1	1	0	1	0	1
1 0	0 0	1	0	0	0	0	0	0	0	0
1 0	0 1	1	0	1	0	1	0	0	0	$Cout_1$
1 0	1 0	1	0	1	0	1	0	0	0	$Cout_1$
1 0	1 1	1	0	1	1	1	0	1	0	1
1 1	0 0	1	1	0	0	0	1	0	1	1
1 1	0 1	1	1	1	0	1	0	0	1	1
1 1	1 0	1	1	1	0	1	0	0	1	1
1 1	1 1	1	1	1	1	1	0	1	0	1

$$Cout_3 = (Cout_1 \cdot (C1_3 \cdot C1_2 + C0_3 \cdot \overline{C1_2})) + (\overline{Cout_1} \cdot (C1_3 \cdot C0_2 + C0_3 \cdot \overline{C0_2}))$$

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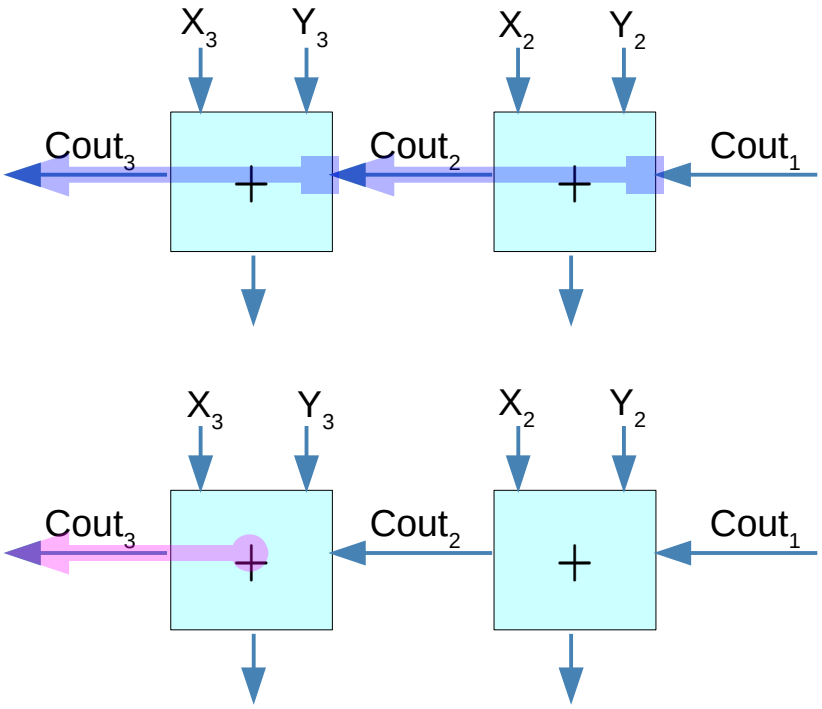
Design C (9) – When Cout1 = 1



$$C1_3 \cdot C1_2 \cdot Cout_1$$

prop prop

$\overline{X_3}Y_3$ $\overline{X_2}Y_2$
$X_3\overline{Y_3}$ $X_2\overline{Y_2}$
X_3Y_3 X_2Y_2

$$C0_3 \cdot \overline{C1_2} \cdot Cout_1$$

gen $\overline{\text{prop}}$

X_3Y_3 $\overline{X_2}\,\overline{Y_2}$

$$Cout_3 = (Cout_1 \cdot (C1_3 \cdot C1_2 + C0_3 \cdot \overline{C1_2})) + (\overline{Cout_1} \cdot (C1_3 \cdot C0_2 + C0_3 \cdot \overline{C0_2}))$$

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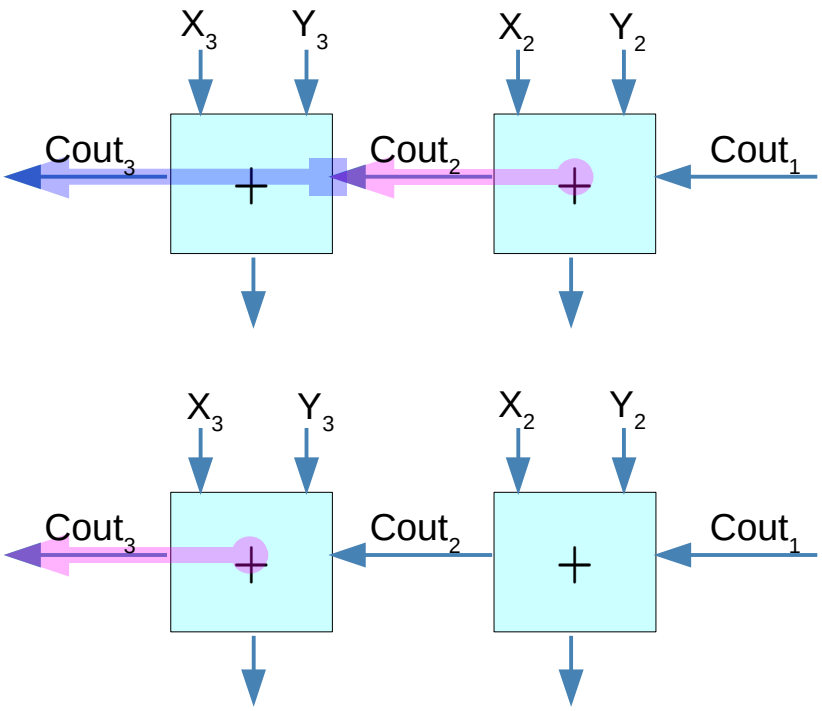
Design C (10) – When Cout1 = 0



$$C1_3 \cdot C0_2 \cdot \overline{Cout}_1$$

prop

$\overline{X}_3 Y_3$

$X_3 \overline{Y}_3$

$X_3 Y_3$

gen

$X_2 Y_2$

$$C0_3 \cdot \overline{C0}_2 \cdot \overline{Cout}_1$$

gen

$X_3 Y_3$

$\overline{\text{gen}}$

$\overline{X}_2 Y_2$

$X_2 \overline{Y}_2$

$\overline{X}_2 \overline{Y}_2$

$$Cout_3 = (Cout_1 \cdot (C1_3 \cdot C1_2 + C0_3 \cdot \overline{C1}_2)) + (\overline{Cout}_1 \cdot (C1_3 \cdot C0_2 + C0_3 \cdot \overline{C0}_2))$$

$(C1_3\, C1_2 + C0_3 \overline{C1}_2) Cout_1 + (C1_3\, C0_2 + C0_3 \overline{C0}_2) \overline{Cout}_1$

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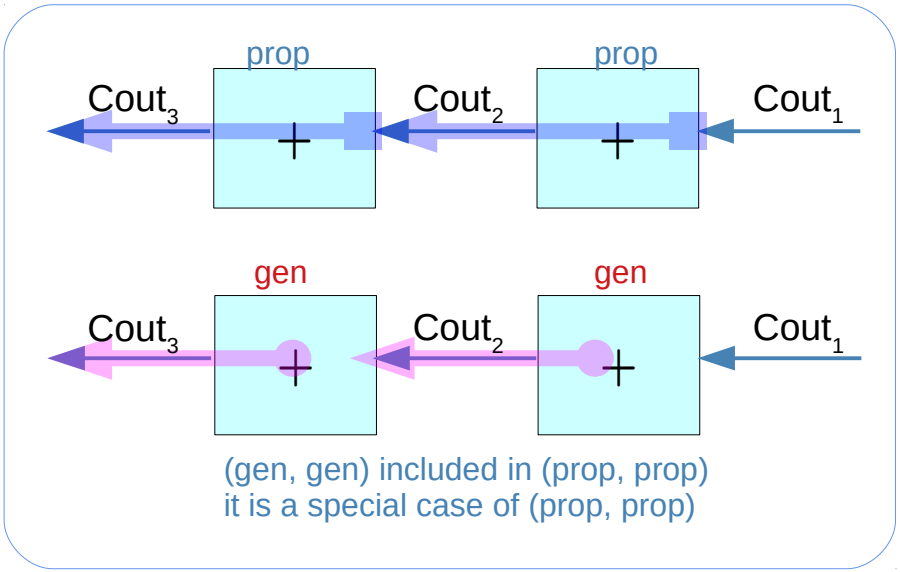
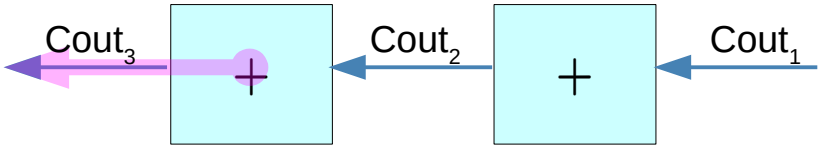
Design C (11) – When Cout1 = 1



$$C1_3 \cdot C1_2 \cdot Cout_1$$

prop: $\overline{X_3}Y_3$, $X_3\overline{Y_3}$, X_3Y_3

prop: $\overline{X_2}Y_2$, $X_2\overline{Y_2}$, X_2Y_2



$$C0_3 \cdot \overline{C1_2} \cdot Cout_1$$

gen: X_3Y_3

$\overline{\text{prop}}$: $\overline{X_2}\,\overline{Y_2}$

$$Cout_3 = (Cout_1 \cdot (C1_3 \cdot C1_2 + C0_3 \cdot \overline{C1_2})) + (\overline{Cout_1} \cdot (C1_3 \cdot C0_2 + C0_3 \cdot \overline{C0_2}))$$

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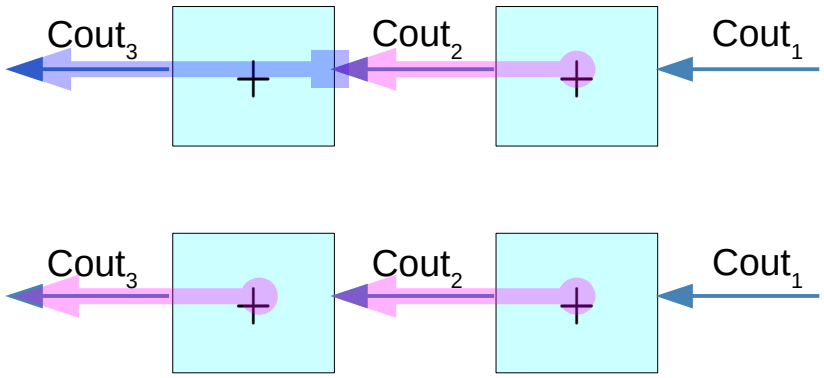
Design C (12) – When Cout1 = 0



(gen, gen) included in (prop, gen)
it is a special case of (prop, gen)

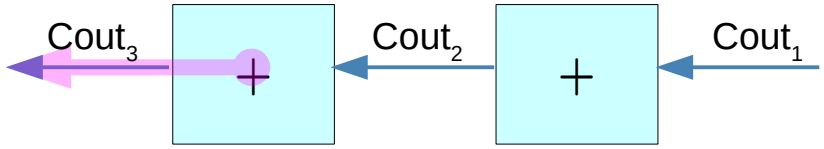
$$C1_3 \cdot C0_2 \cdot \overline{Cout_1}$$

prop

$\overline{X_3}Y_3$
$X_3\overline{Y_3}$
X_3Y_3

gen

X_2Y_2



$$Cout_3 = (Cout_1 \cdot (C1_3 \cdot C1_2 + C0_3 \cdot \overline{C1_2})) + (\overline{Cout_1} \cdot (C1_3 \cdot C0_2 + C0_3 \cdot \overline{C0_2}))$$

$$C0_3 \cdot \overline{C0_2} \cdot \overline{Cout_1}$$

gen

X_3Y_3

$\overline{gen}$

$\overline{X_2}Y_2$
$X_2\overline{Y_2}$
$\overline{X_2}\overline{Y_2}$

$(C1_3\,C1_2 + C0_3\overline{C1_2})Cout_1 + (C1_3\,C0_2 + C0_3\overline{C0_2})\overline{Cout_1}$

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FPGA Carry Chain Cell

$$C1 = \overline{X}\,Y + X\,\overline{Y} + X\,Y \qquad C0 = X\,Y$$

$$\overline{C1} = \overline{X}\,\overline{Y} \qquad \overline{C0} = \overline{X}\,Y + X\,\overline{Y} + \overline{X}\,\overline{Y}$$

C1 and C0 are not mutually exclusive

C1 includes C0

$$C1 \cdot C0 = C0 \qquad C1 + C0 = C1$$

$$\overline{C1} \cdot \overline{C0} = \overline{C1} \qquad \overline{C1} + \overline{C0} = \overline{C0}$$

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