Tutorial 1 Summary (A)

Based on
Electric VLSI Design System Tutorials from CMOSedu.com
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Modified by Young W. Lim

Based on
Electric VLSI Design System Tutorials from CMOSedu.com (Return)

Tutorial 1 – Layout and simulation of a resistive voltage divider

Window -> Color Schemes -> White Background Colors
Using a white background

ON Semiconductor's C5 process and fabrication through MOSIS

two layers of polysilicon to make a poly1-poly2 capacitor, 3 layers of metal, and a hi-res layer to block the implant, and thus decrease in resistance, of poly2 to fabricate higher-value (than what we would get with poly1) poly2 resistors.

MOSIS scalable CMOS (SCMOS) submicron design rules

File -> Preferences then Technology -> Technology
"Analog" Technology is selected

the scale (lambda) for the C5 process is 300 nm using the MOSIS Scalable CMOS (mocmos technology in Electric) submicron design rules.

To set the scale go to File -> Preferences -> Technology -> Scale 300 nm
Mark All Libs

preferences (right click and save as), **electricPrefs.xml**

File -> Import -> User Preferences

set up to fabricate a chip in the C5 process via MOSIS (technology code is SCN3ME_SUBM with a lambda of 0.3 um, see the MOSIS page here at CMOSedu.com).

File -> Save Library As -> tutorial_1.jelib

the schematic of a resistive divider.

Cell -> New Cell and enter the **cell name** (*R_divider*) and **view** (*schematic*) seen below.

selecting the Component tab

The **library name** and **cell name** above the Components, Explorer,
and **Layers**

a box containing a resistor and the word "Normal."
Click and select N-Well (the N-Well schematic resistor Node)

a Node : a component in a schematic / layout.
An Arc, : connects Nodes together

cycling: Ctrl+mouse click

selects/de-selects :Shift + the left mouse button

Edit -> Properties -> Object Properties (Ctrl+I)

800 ohms.
The minimum width of n-well is 12 lambda
a 10k resistor using a width of 15 and a length 187.5

Tools -> DRC -> Check Hierarchically (or just hit F5) *to check the schematic for errors*.

make a layout corresponding to this schematic-view cell.

Cell -> New Cell and enter the **Name** and **View** seen below.

The red circle : a schematic view
the yellow circle : the cell's layout view.

Blue : an icon
black : a Verilog view

the ***library*** name : **tutorial_1**
the active ***cell*** name : **R_divider{lay}**.

at the bottom : the ***technology*** and ***scale***.
Components tab and select the N-well resistor Node
(Analog option in the preferences)

Set the size
Edit -> Properties -> Object Properties or Ctrl+I)
W=15, L=187.5, and a resistance of 10k.

Tools -> DRC -> Check Hierarchically (or just hit F5) to perform a design rule check.

the width is 5.
to step through the errors we press the >, <

Ctrl+Z
Ctrl+I
Press F5

Window -> Fill Window to zoom back out.

verify that the schematic and layout views of the R_divider cells are equivalent.
This layout versus schematic (LVS) verification
using Network Consistency Checking (NCC).

Tools -> NCC -> Schematic and Layout Views of Cell

File -> Preferences -> General -> Key Bindings
Tools -> NCC -> Schematic and Layout Views of Cell in Current Window

Add and bind L important.
“Remove All” conflicts (important).

connection of the n-well and p-substrate.
the C5 process used is an n-well process
the p-type substrate is common to all NMOS devices and *grounded*.

One of the electrical rule checks **(ERCs)** is
to verify that the p-well (p-substrate) is always connected to ground.

Further, in this n-well process, for digital circuits
the n-well to be connected to *VDD*.
To setup the ERC Well Check
Preferences -> Tools -> Well Check

verify that a contact is found in every area (floating wells are bad!).
verify that the p-substrate (p-well) is always tied to ground.
verify that the n-well is tied to vdd if a digital only design (no N-Well resistors)

Tools -> ERC -> Check Wells
To eliminate these errors,
our design isn’t only digital (*analog box*) change the settings
Mark All Libs

using the Explorer, schematic view of the R_divider cell
Select the N-Well resistor Node and then hit Ctrl+C
deselect the Node. Press Ctrl+V and then left-click
Ctrl-Z
select the bottom resistor Node
Edit -> Rotate -> 90 Degrees Counterclockwise (Ctrl+J)

select the top Nodes right port by the left mouse
makes this port *active*
ready of a wire connection.
above the vertical Node and RIGHT
F5.
cursor over the corner in the wire you will see a Pin
Pins can be moved
error : unnecessary Pins
remove by Edit -> Cleanup Cell -> Cleanup Pins
key bindings : F4
(available in **electricPrefs.xml**, right click to save
then File -> Import -> User Preferences)

add a couple more wires
left click for *selecting a port on a Node*
right click to *add the Arc (wire)*

1.symbols for gnd and vdd from the component menu
2. label the Arcs (the wires)

the SPICE components by clicking SPICE box under the Component menu
Select an Arc and press Ctrl+I to edit the properties of the Arc or
simply just double-click on the Arc.
Label the Arcs

gnd
vdd

click ***Misc box*** in the Component menu to add SPICE code to the schematic
Place the SPICE code in the schematic
Ctrl+I to edit its properties.
Ensurethe Multi-line Text box is checked.
specifying a SPICE transient analysis and an input voltage source.
F5

Tools -> Simulation (Spice) -> Write Spice Deck
LTspice window will open.
show the waveforms
Select V(vout) and V(vin)
The LTpsice waveform doesn't allow for cross-probing

To plot SPICE results using Electric's probe,
in LTspice, not Electric Tools -> Control Panel -> Operation
waveform files (.raw files) are not automatically deleted.
When LTspice is closed, with the setups seen here,
Electric's probe will run as seen below
(after the explorer was used to select vin and vout).

To bypass the LTspice Window and
use Electric's probe
only change from the –i (interactive) to –b (batch) modes

Next let's layout the resistive divider.
Open the layout view of the R_divider cell then copy/paste (Ctrl+C/Ctrl+V) an additional resistor as seen below.
To move the resistor Node (the layout of an N-Well resistor) either the mouse can be used or you can select the Node

0.5 scale above.
Running a DRC (pressing F5)
By several >, too little space between the N-wells.
Move the Nodes apart until the layout passes the DRCs.

left click (to select the top node and its right port).
RIGHT clicking (over the right side of the highlight box on the bottom resistor node)
will connect the metal1 Arc to the bottom resistor.
over the right side of the highlight box

how many Pins ? Answer, 2.
The ends of the metal Arcs that aren't connected to anything
contain **Pins**.
Pins at any bends or corners in the metal Arcs.

in the Component menu below the metal1 Pin
Placing a Pin in a layout is
useful for drawing an Arc without first having a Node.
with this Pin selected, RIGHT click somewhere to draw a metal1 Arc
Please experiment with drawing Arcs from Pins, these Nodes, and to other Arcs.

increase the width of the metal1 Arc
to match the connection to the N-Well resistor.
Select the Arc and hit Ctrl+I (Edit -> Properties -> Object Properties)

Change the width of the Arc to **4** and hit OK
Note the field "End Extension"
This field specifies how the ends of the Arc are drawn.
Remember to DRC the cell

label the Arcs: **vin**, **vout**, and **gnd**.
select and press Ctrl+I (or just double click on the Arc).

Using Ctrl+click may be very useful here.

Edit the *properties of this **text***, the Arc's name, by Ctrl+I.
Change the ***text size*** from 1 to 10
Change the size of all of the other Arc names resulting in the following.

should be *DRC clean* (F5)
running the NCC (aka LVS check).
The Arc names are useful for humans but don't affect circuit operation ;-)
We are ready to simulate the layout view off this cell.

the schematic view of the cell and copy the SPICE code (select, Ctrl+C).
Go back to the layout view and paste the SPICE code as seen below (the SPICE code is circled).

Change **the text size** used in the SPICE code to 10
Run a DRC, NCC, and a Well Check

tutorial_1.jelib (right click to save to C:\Electric).