Structure (2A)

- Configuration

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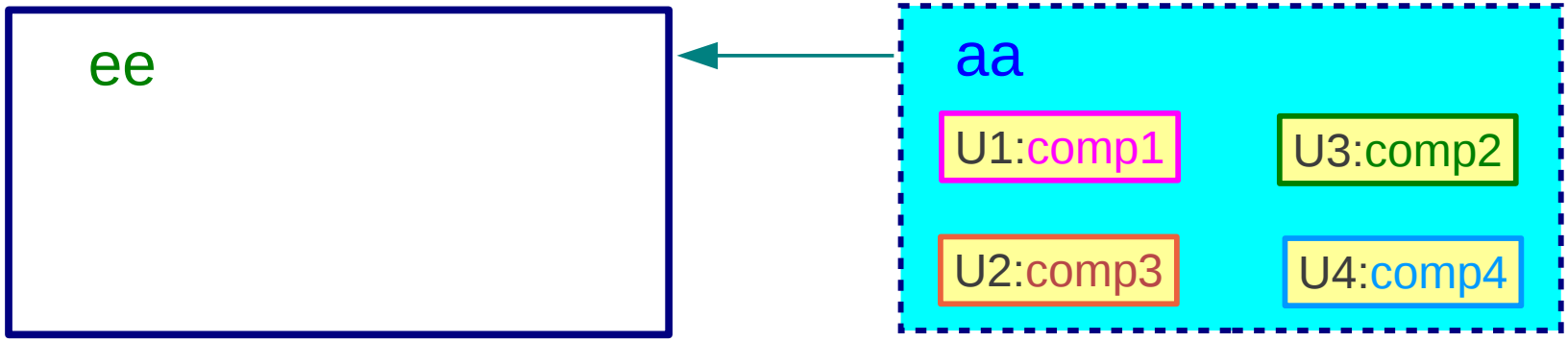
Structural Hierarchy

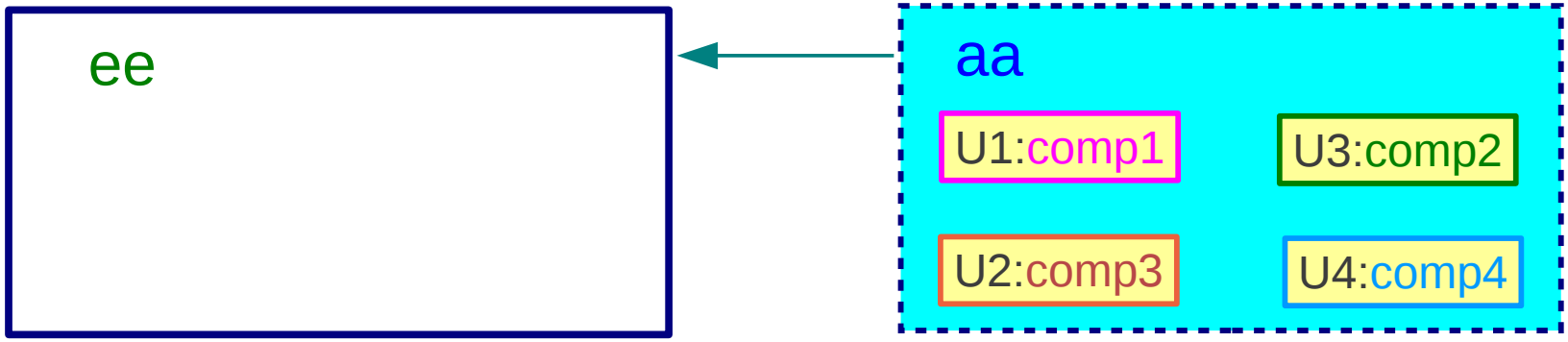


Component Declaration

```
component comp1 is
        port (        );
end component;

component comp2 is
        port (        );
end component;

component comp3 is
        port (        );
end component;

component comp4 is
        port (        );
end component;
```

```
architecture aa of ee is

begin

        Component Instantiation

U1: comp1 port map (      );
U2: comp2 port map (      );
U3: comp3 port map (      );
U4: comp4 port map (      );


end aa;
```

Which Entity – Architecture pairs?



- *Default Binding*
- *Configuration Specification*
- *Configuration Declaration*
  - *Default Configuration*
  - *Component Configuration*
    - *entity-architecture configuration*
    - *low level configuration*
  - *Block Configuration*

architecture aa **of** ee **is**

begin

Component Instantiation

```
U1: comp1 port map (      );
U2: comp2 port map (      );
U3: comp3 port map (      );
U4: comp4 port map (      );
```

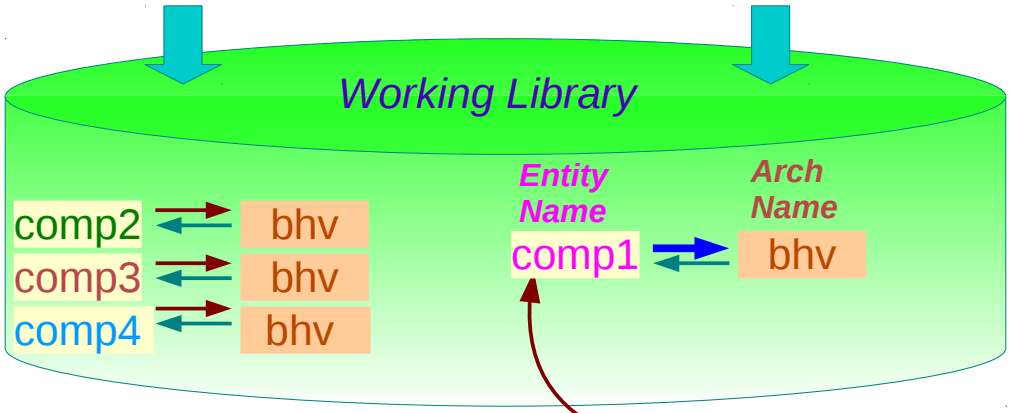
end aa;

Default Binding

```
entity comp1 is
      port (       );
end comp1;

entity comp2 is
      port (       );
end comp2;

entity comp3 is
      port (       );
end comp3;

entity comp4 is
      port (       );
end comp4;
```

```
architecture bhv of  comp1 is
      . . .
end comp1;

architecture bhv of comp2 is
      . . .
end comp2;

architecture bhv of comp3 is
      . . .
end comp3;

architecture bhv of comp4 is
      . . .
end comp4;
```

```
architecture aa of ee is


begin
        Component
        Name
    U1: comp1 port map (      );
    U2: comp2 port map (      );
    U3: comp3 port map (      );
    U4: comp4 port map (      );


end aa;
```



Component – Entity Binding

Component Name = Entity Name

Entity – Architecture Binding

Last compiled Architecture

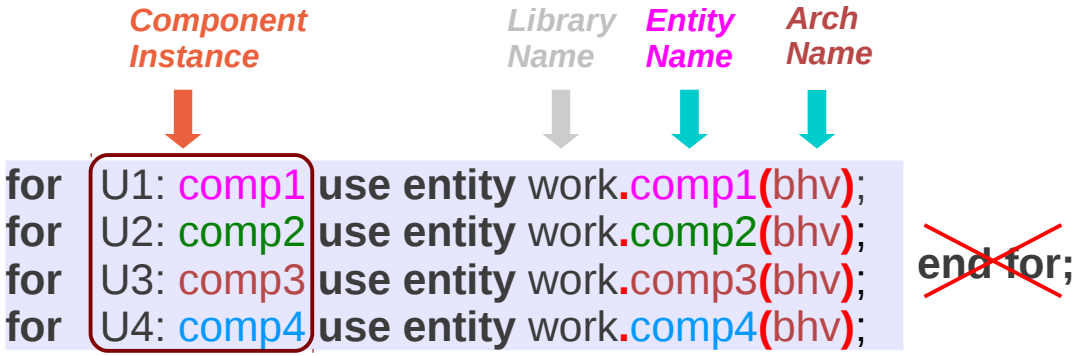
Configuration Specification (1)

Configuration Specification :

For each component instance,

Specify the selection of

- ***Entity declaration and***
- ***Architecture body.***



*Also known as **Architecture Configuration** since the specification of configuration exists in the architecture declarative region*

Configuration Specification (2)

Component Declaration

Interface

```
component comp1 is
        port (        );
end component;

component comp2 is
        port (        );
end component;

component comp3 is
        port (        );
end component;

component comp4 is
        port (        );
end component;
```

Component Instance | *Library Name* | *Entity Name* | *Arch Name*

```
for U1: comp1 use entity work.comp1(bhv);
for U2: comp2 use entity work.comp2(bhv);
for U3: comp3 use entity work.comp3(bhv);
for U4: comp4 use entity work.comp4(bhv);
end for;
```

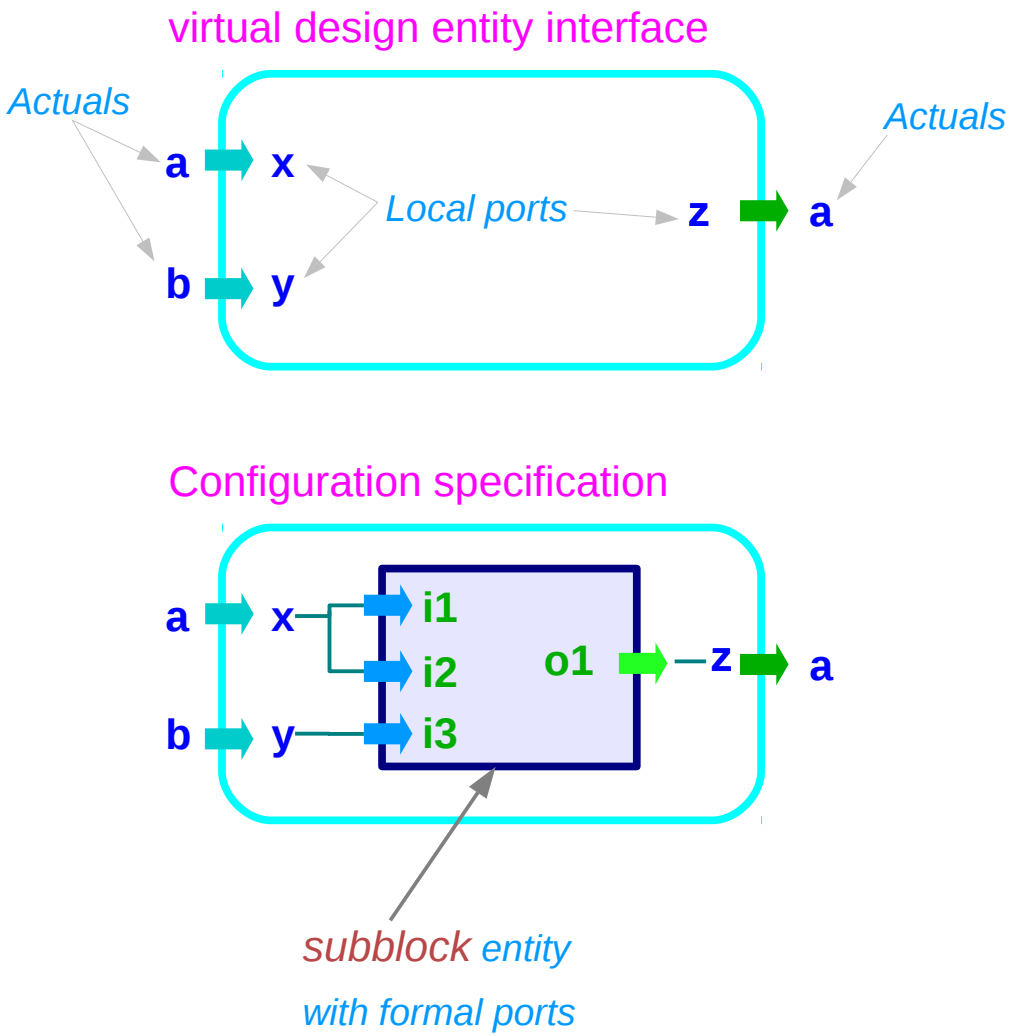
```
architecture aa of ee is

begin

        Component Instantiation
        U1: comp1 port map (      );
        U2: comp2 port map (      );
        U3: comp3 port map (      );
        U4: comp4 port map (      );

        Component Name

end aa;
```

Configuration Specification :
For each component instance, Specify the selection of

- ***Entity declaration and***
- ***Architecture body.***

2-Step Association of Ports

```
architecture aa of ee is

    component comp1 is
        port (x, y in bit; z: out bit);
    end component;      Local ports

        Configuration Specification

    for   U1: comp1
          use entity work.subblock(bhv)
          port map (x, x, y, z);

                Formal port map
begin
        Component Instantiation

    U1: comp1 port map (a, b, c );

                Actuals
end aa;
```



Configuration Declaration (1)

*The **configuration** of an **entity** is*

*for a specific **architecture** specify*

- *Default Configuration*
- *Component Configuration*
- *Block Configuration*

```
configuration conf1 of ee is
  for aa
      • Default Configuration
      • Component Configuration
      • Block Configuration
  end for;
end conf1;
```

A Configuration :

A Design Unit

complied separately
stored in a library

Recompilation

of the entire design can be avoided

Component Configuration

- *entity-architecture configuration*
- *low level configuration*

```
for   U1: comp1 use entity work.entity_name(arch_name);  end for;

for   U1: comp1 use configuration work.ll_conf_name;  end for;
```

Configuration Declaration (2)

*The **configuration** of an **entity** is*

*for a specific **architecture** specify*

- *Default Configuration*

```
configuration conf1 of ee is
  for aa
  end for;
end conf1;
```

*The **configuration** of an **entity** is*

*for a specific **architecture** specify*

- *Component Configuration*

```
configuration conf1 of ee is
  for aa
      for   U1: comp1 * * *  end for;
      for   U2: comp2 * * *  end for;
      for   U3: comp3 * * *  end for;
      for   U4: comp4 * * *  end for;
  end for;
end conf1;
```

*The **configuration** of an **entity** is*

*for a specific **architecture** specify*

- *Block Configuration*

```
configuration conf1 of ee is
  for aa
      for   block/arch_name
            • Component Configuration
            • Block Configuration
      end for;
  end for;
end conf1;
```

Default Configuration (1)

*The **configuration** of an **entity** is*

*for a specific **architecture** specify*

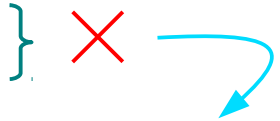
- *Default Configuration*

```
configuration conf1 of ee is
  for aa
  end for;
end conf1;
```

The configuration of an entity is

For a specific architecture specify

- *Component Configuration*
- *Block Configuration*



No Component Configuration
No Block Configuration

Use Default Binding

Default Configuration:
No specific configuration
for any block or component

Default Binding

last architecture compiled
is used for an entity

Can be used for models that do not contain
any blocks or components to configure

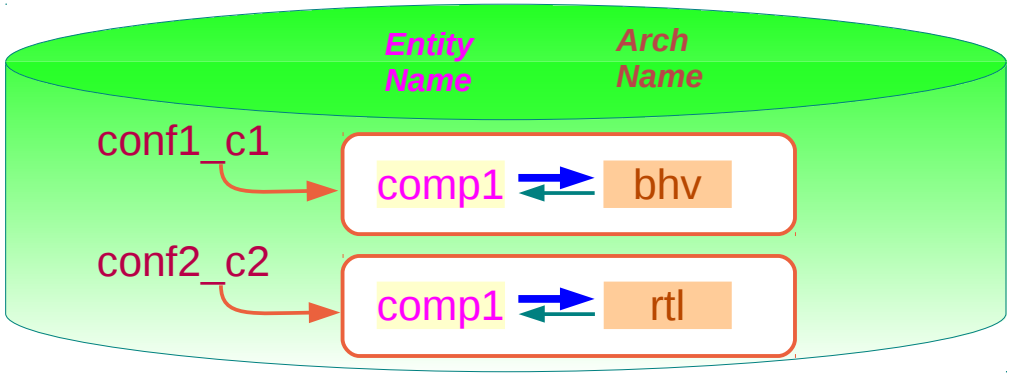
Default Configuration (2)

```
entity comp1 is
      port (       );
end comp1;
```

```
architecture bhv of comp1 is
        . . .
end comp1;
```

```
architecture rtl of comp1 is
        . . .
end comp1;
```

default configurations
of the entity comp1



Default Binding

components in the bhv architecture of the comp1 entity

components in the rtl architecture of the comp1 entity

```
architecture aa of ee is


begin
```

Component Name

```
    U1: comp1 port map (      );
    U2: comp2 port map (      );
    U3: comp3 port map (      );
    U4: comp4 port map (      );
```

```
end aa;
```

```
configuration conf1_c1 of comp1 is
      for bhv
      end for;
end conf1_c1;
```

```
configuration conf2_c1 of comp1 is
      for rtl
      end for;
end conf2_c1;
```

Component Configuration (1)

*The **configuration** of an **entity** is*

*for a specific **architecture** specify*

- *Component Configuration*

```
configuration conf1 of ee is
  for aa
      for  U1: comp1 * * *  end for;
      for  U2: comp2 * * *  end for;
      for  U3: comp3 * * *  end for;
      for  U4: comp4 * * *  end for;
  end for;
end conf1;
```

Component Configuration

- *entity-architecture configuration*
- *low level configuration*

```
for  U1: comp1 use entity work.entity_name(arch_name);  end for;

for  U1: comp1 use configuration work.ll_conf_name;  end for;
```

Component Configuration (2)

Entity-Arch Configuration

Library Name *Entity Name* *Arch Name*

```
configuration conf1 of ee is
  for aa
       for   U1: comp1 use entity work.comp1(bhv);  end for;
       for   U2: comp2 use entity work.comp2(bhv);  end for;
       for   U3: comp3 use entity work.comp3(bhv);  end for;
       for   U4: comp4 use entity work.comp4(bhv);  end for;
  end for;
end conf1;
```

Low Level Configuration

Library Name *Conf Name*

```
configuration conf1 of ee is
  for aa
       for   U1: comp1 use configuration work.conf_c1;  end for;
       for   U2: comp2 use configuration work.conf_c2;  end for;
       for   U3: comp3 use configuration work.conf_c3;  end for;
       for   U4: comp4 use configuration work.conf_c4;  end for;
  end for;
end conf1;
```

Entity – Architecture Configuration

Component Declaration

```
component comp1 is
        port (          );
end component;

component comp2 is
        port (          );
end component;

component comp3 is
        port (          );
end component;

component comp4 is
        port (          );
end component;
```

```
architecture aa of ee is

begin

        Component Instantiation
        U1: comp1 port map (      );
        U2: comp2 port map (      );
        U3: comp3 port map (      );
        U4: comp4 port map (      );

end aa;
```

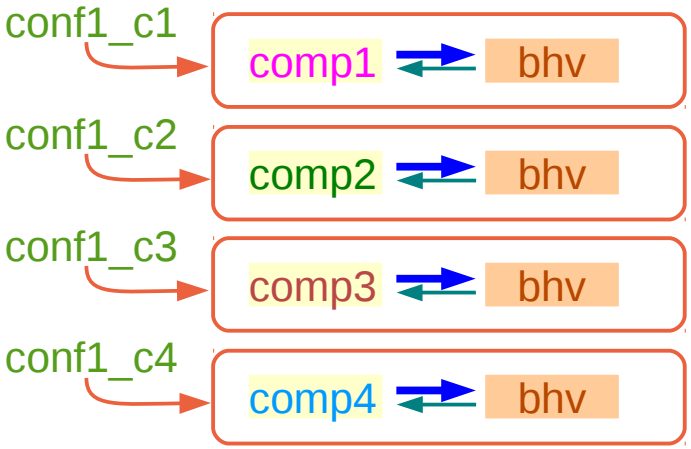
```
configuration conf_ea of ee is
  for aa
      for   U1: comp1 use entity work.comp1(bhv);  end for;
      for   U2: comp2 use entity work.comp2(bhv);  end for;
      for   U3: comp3 use entity work.comp3(bhv);  end for;
      for   U4: comp4 use entity work.comp4(bhv);  end for;
  end for;
end conf_ea;
```

Library Name *Entity Name* *Arch Name*

Low Level Configuration (1)

Component Declaration

```
component comp1 is
        port (          );
end component;
```

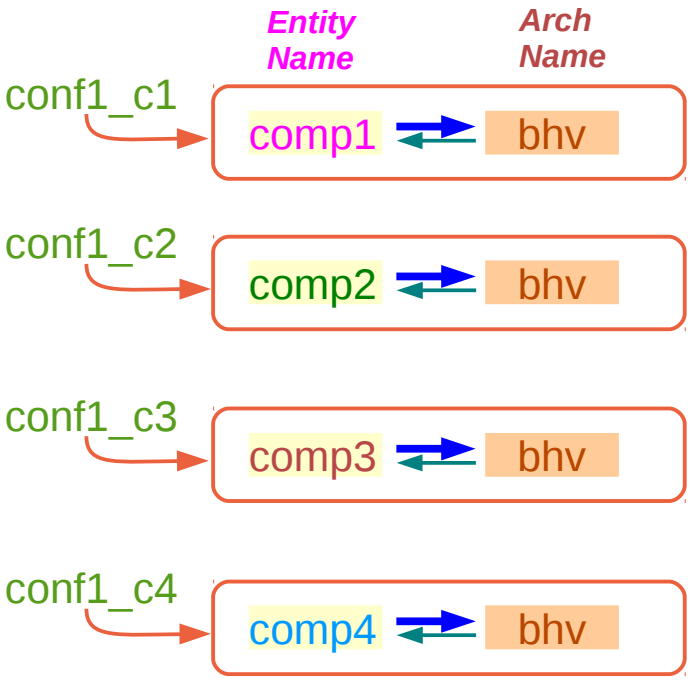



```
architecture aa of ee is

begin

        Component Instantiation
        U1: comp1 port map (      );
        U2: comp2 port map (      );
        U3: comp3 port map (      );
        U4: comp4 port map (      );

end aa;
```

```
configuration conf_II of ee is
  for aa
      for  U1: comp1 use configuration work.conf1_c1;  end for;
      for  U2: comp2 use configuration work.conf1_c2;  end for;
      for  U3: comp3 use configuration work.conf1_c3;  end for;
      for  U4: comp4 use configuration work.con1f_c4;  end for;
  end for;
end conf_II;
```

Library Name — *Configuration Name*

Low Level Configuration (2)



Configuration Name — Entity Name

Arc Name
```
configuration conf1_c1 of comp1 is
    for bhv    end for;
end conf1;
```

Arc Name
```
configuration conf1_c2 of comp2 is
    for bhv    end for;
end conf1;
```

Arc Name
```
configuration conf1_c3 of comp3 is
    for bhv    end for;
end conf1;
```

Arc Name
```
configuration conf1_c4 of comp4 is
    for bhv    end for;
end conf1;
```

```
configuration conf_ll of ee is
  for aa
      for  U1: comp1 use configuration work.conf1_c1;  end for;
      for  U2: comp2 use configuration work.conf1_c2;  end for;
      for  U3: comp3 use configuration work.conf1_c3;  end for;
      for  U4: comp4 use configuration work.con1f_c4;  end for;
  end for;
end conf_ll;
```

Library Name — Configuration Name

Block Configuration (1)

The configuration of an entity is

for a specific architecture specify

- ***Block Configuration***

```
configuration conf1 of ee is
  for aa
    for   block/arch_name
          • Component Configuration
          • Block Configuration
    end for;
  end for;
end conf1;
```

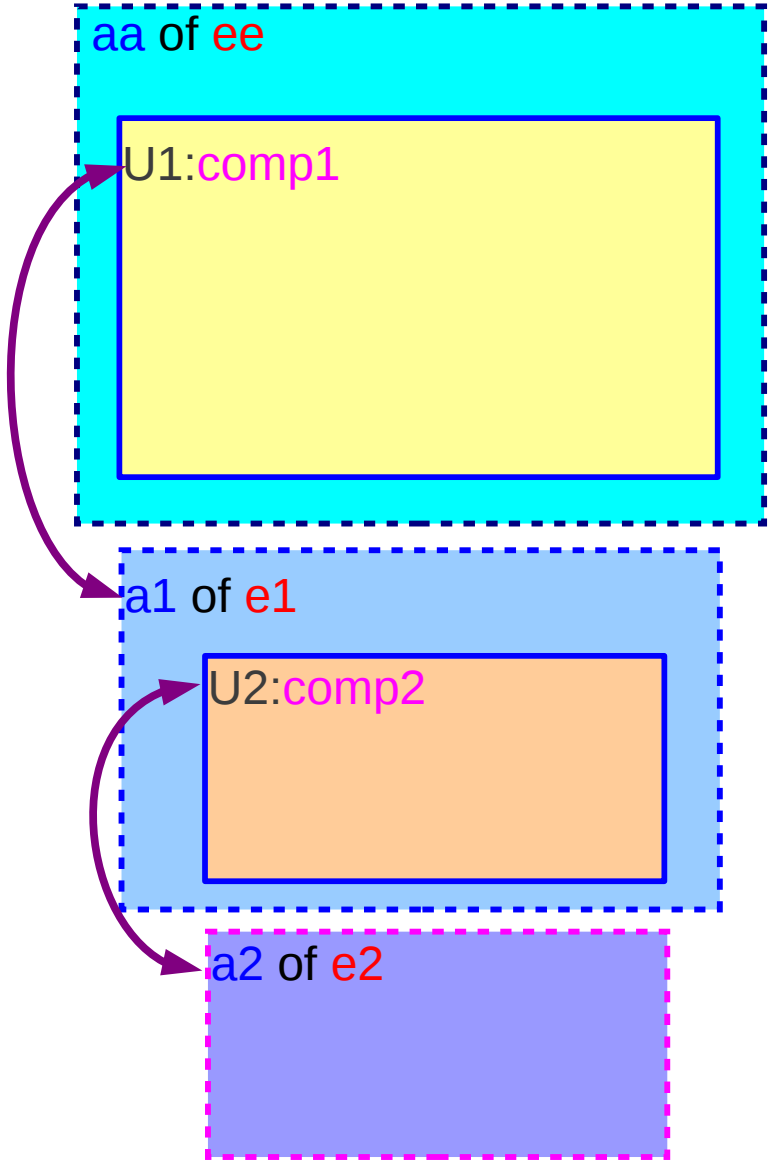
Block configuration *is used, for* ***visibility*** *into an architecture or a block*

Component configuration *is used, for* ***binding*** *a component label to an actual component*

A component configuration is possible only when an instance of that component has been made ***visible*** *by the use of* ***nested block configurations***

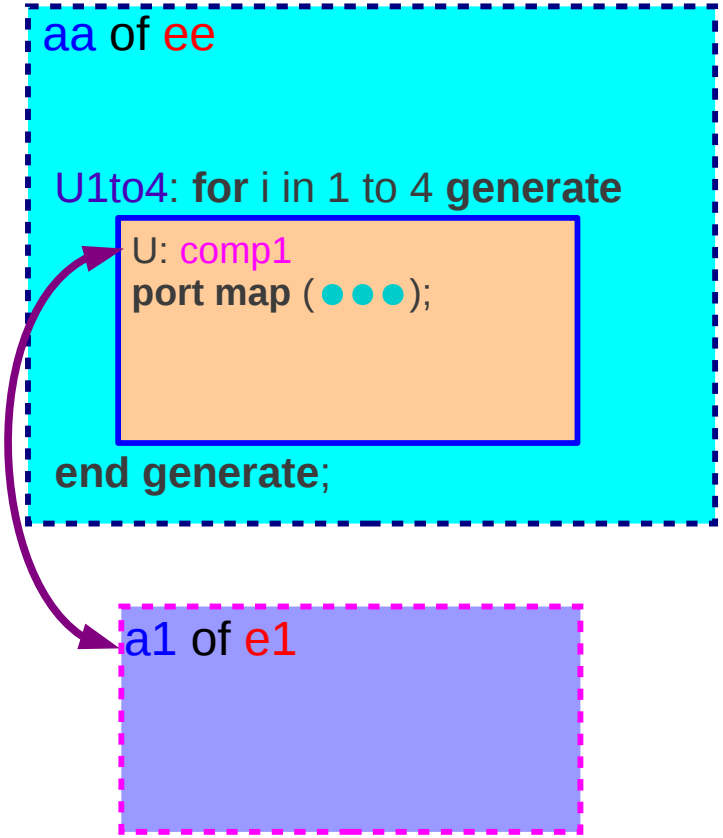
At each level of nesting, ***block configurations*** *are needed to obtain the visibility of a component, and* ***component configurations*** *are needed to associate instances of components with actual components*

Block Configuration (2)




```
configuration conf of ee is
  for aa
      for   U1: comp1
            use entity work.e1(a1);
            for   a1   ←  block configuration
                  use entity work.e2(a2);
                  for  a2   ←  block configuration
                     ●●●
                  end for;
            end for;
      end for;
  end for;

end conf;
```

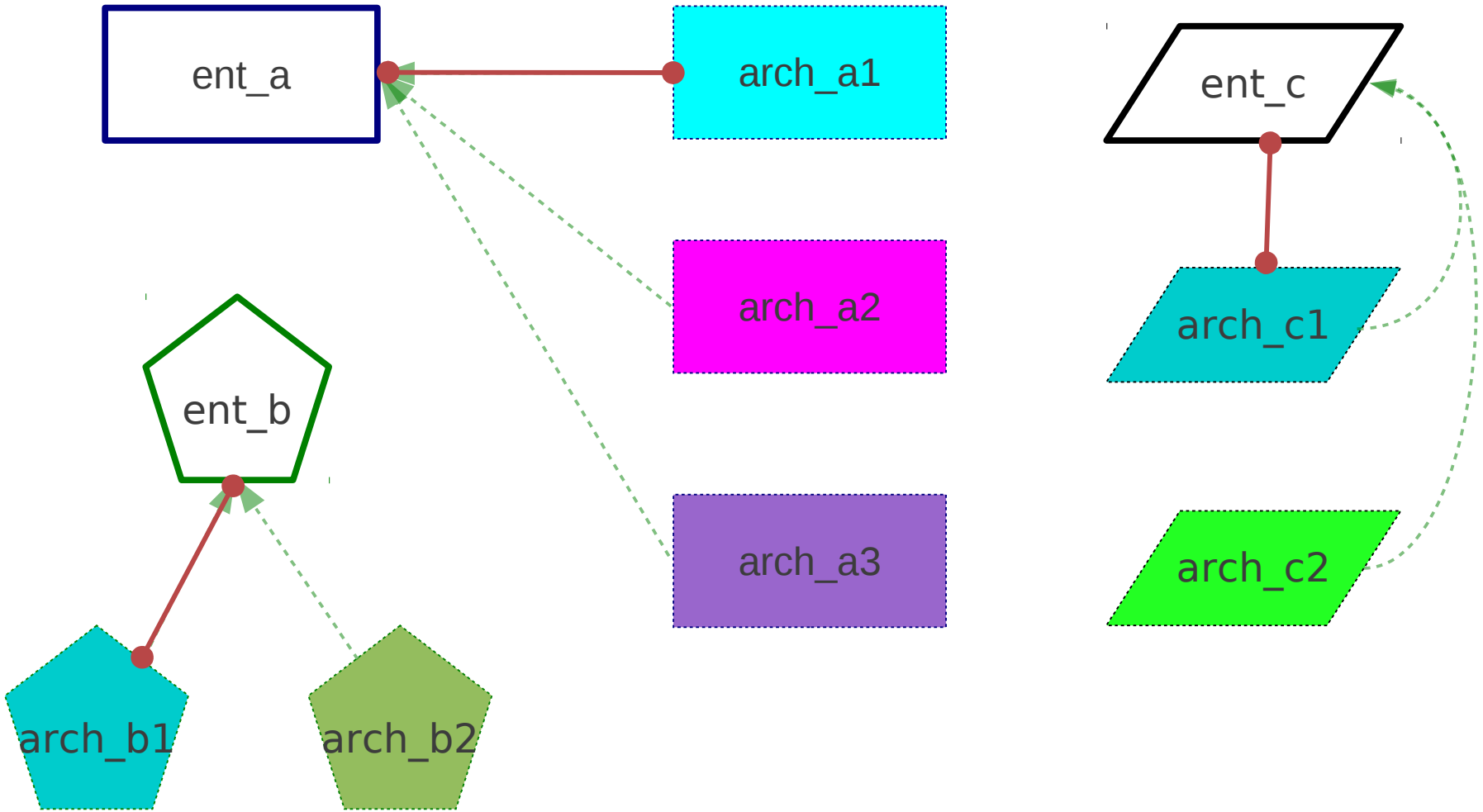
Block Configuration (3)



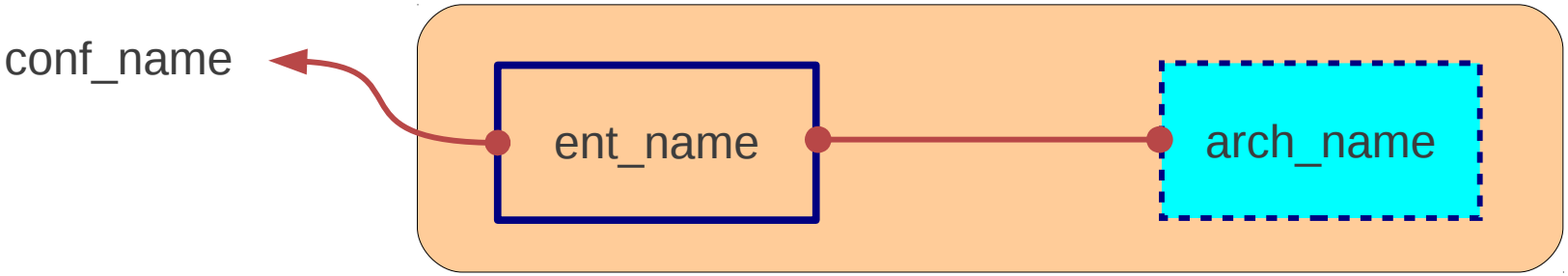

```
configuration conf of ee is
  for aa
      for   U1to4   ←  block configuration
            for   U: comp1
                  use entity work.e1(a1);
            end for;
      end for;
  end for;

end conf;
```

Sequential Assignment (1)

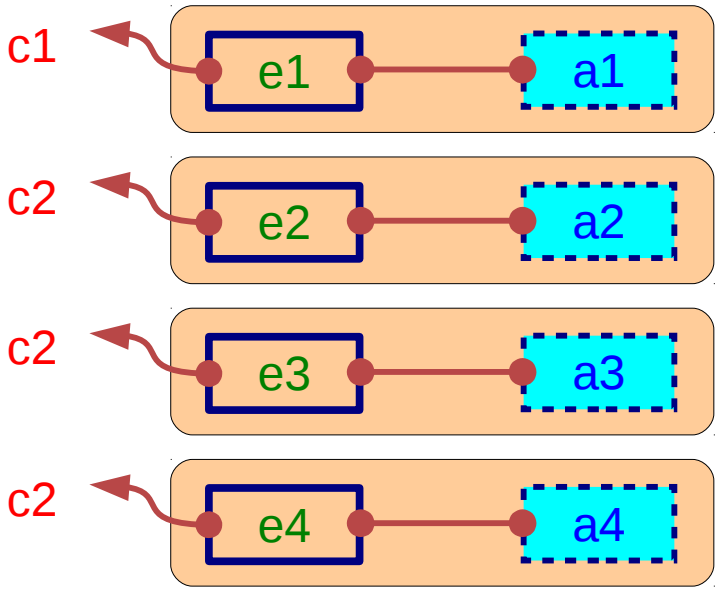
Entity – Architecture Binding



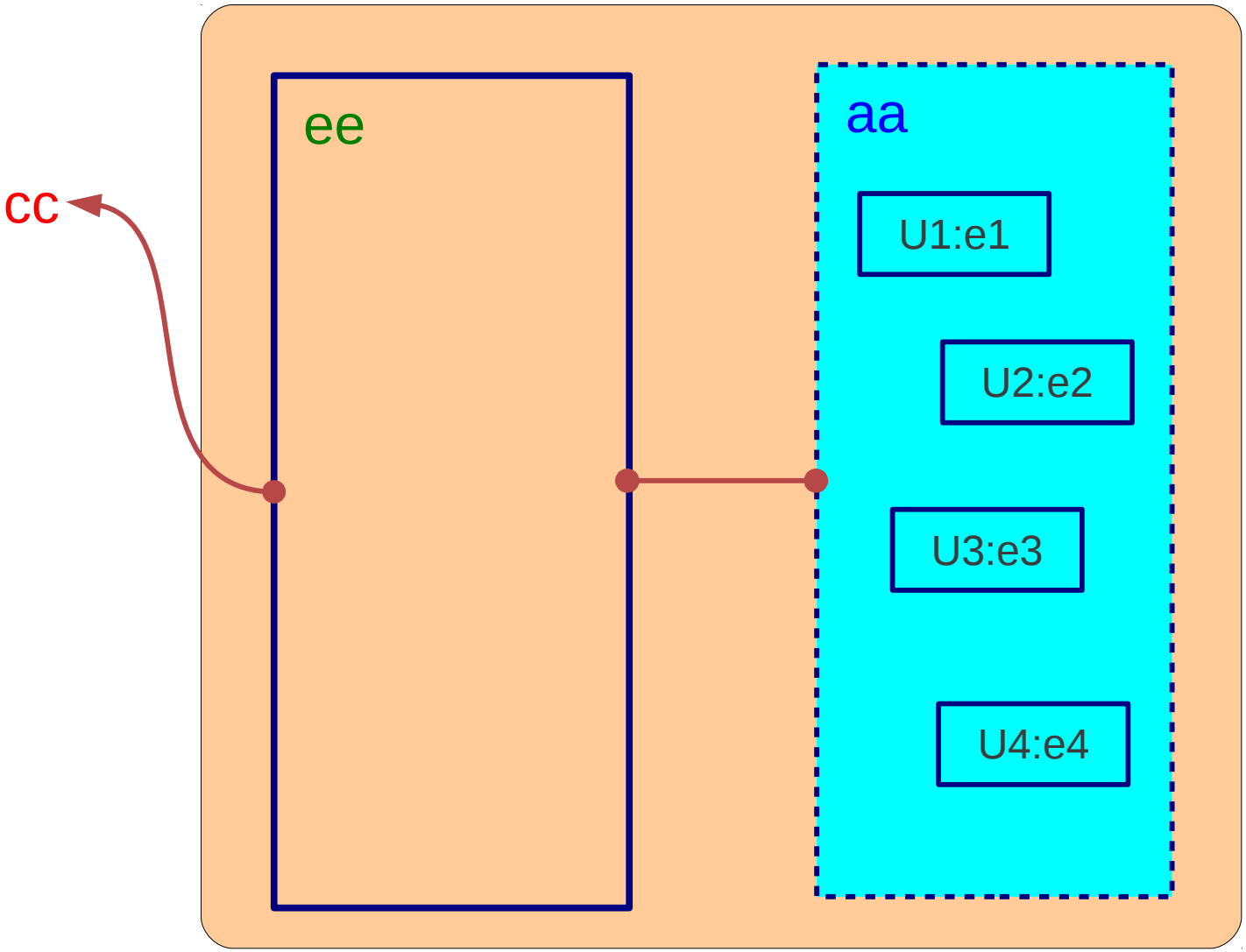
Configuration



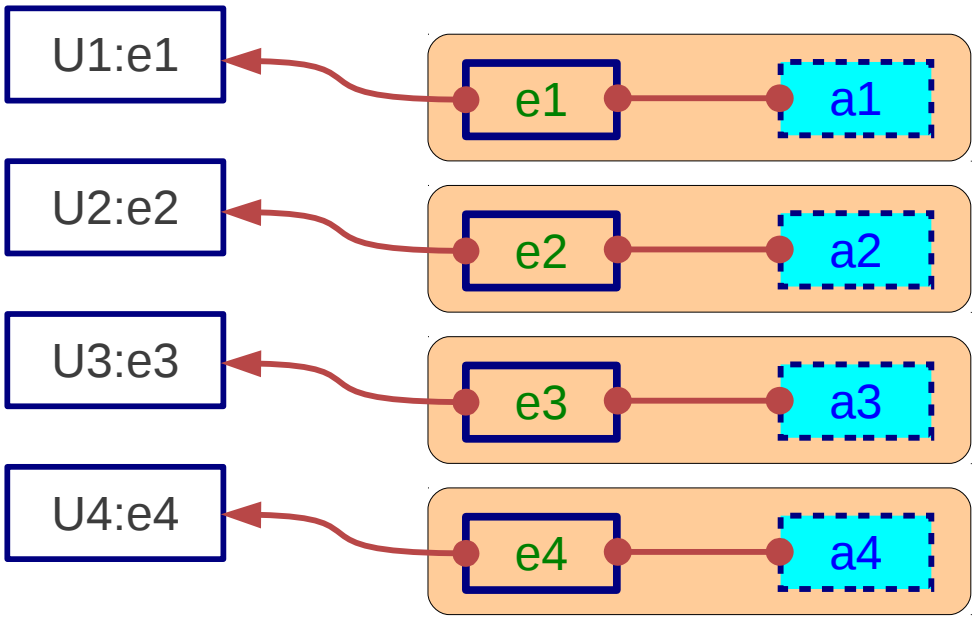
Configuration



Sequential Assignment (2)



Sequential Assignment (2)



Sequential Assignment (2)

References

[1] http://en.wikipedia.org/
[2] J. V. Spiegel, VHDL Tutorial,
http://www.seas.upenn.edu/~ese171/vhdl/vhdl_primer.html
[3] J. R. Armstrong, F. G. Gray, Structured Logic Design with VHDL
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[7] VHDL Tutorial - VHDL onlinewww.vhdl-online.de/tutorial/