# Logic Families Static-2 (H.2)

20151215

# References

Some Figures from the following sites


[1] http://pages.hmc.edu/harris/cmosvlsi/4e/index.html
Weste & Harris Book Site

[2] en.wikipedia.org

[3] Digital Integrated Circuits : A Design Perspective,
Jan M. Rabaey,
(http://bwrcs.eecs.berkeley.edu/Classes/IcBook/)

[4] Digital Electronics and Design with VHDL
Pedroni

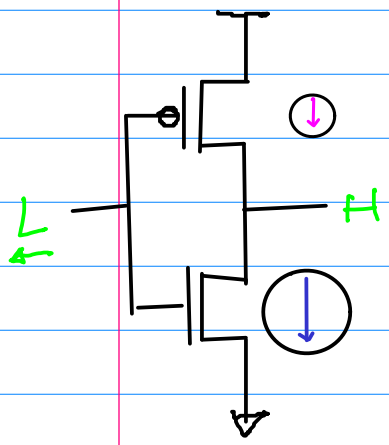
# Other MOS Archtectures

Static MOS
- Pseudo-nMOS Logic
- Transmission-gate Logic
- BiCMOS Logic

Dynamic MOS
- Dynamic Logic
- Domino Logic
- C2MOS Logic

# Weak / Strong pMOS

the same size
pMOS, nMOS

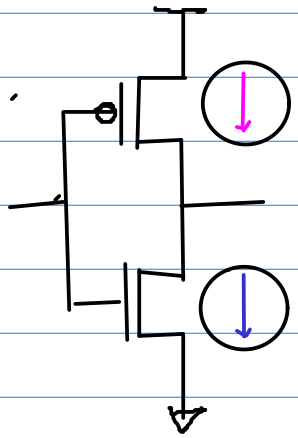



**Weak pMOS**

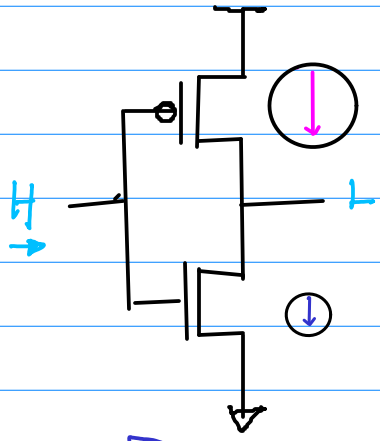
hard to turn off nMOS
hard to become "H"
decreased input Vth

$V_{iL}$ to turn off nMOS
Vin have to be
closer to GND

double size pMOS
minimum size nMOS



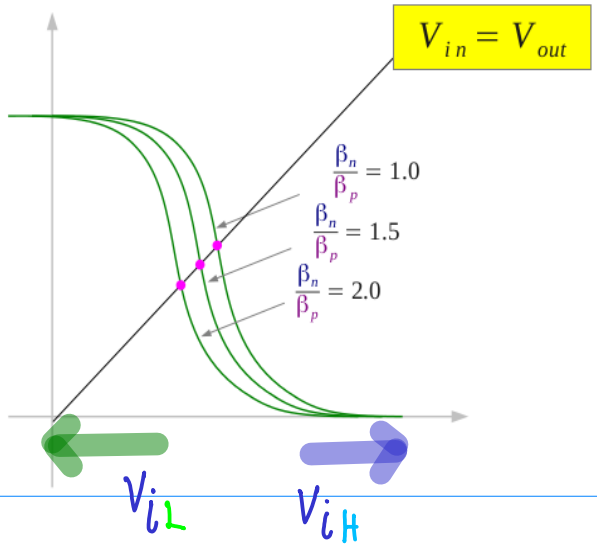
**a Unit Inverter**




**Strong pMOS**

hard to turn off pMOS
hard to become "L"
increased input Vth

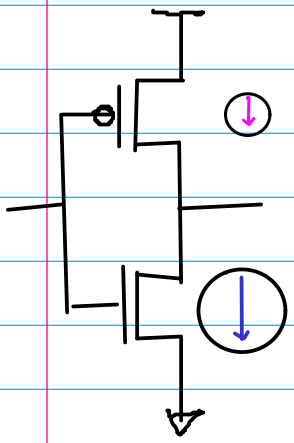
$V_{iH}$ to turn off nMOS
Vin have to be
closer to Vdd



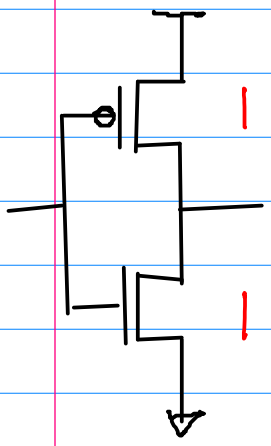
# Skewed Inverters

**Low Skewed Inverter**

fall delay : faster

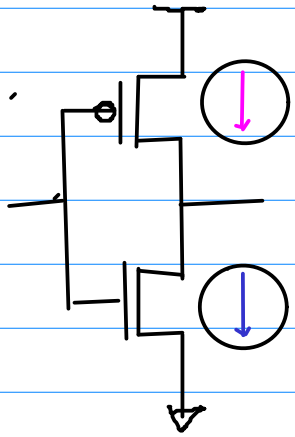


$\left(\frac{W}{L}\right)_p = 1 \left(\frac{W}{L}\right)_n$

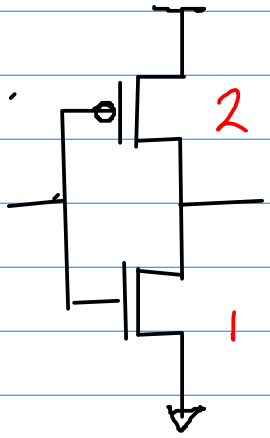



**Unskewed Inverter**

**Symmetric Inverter**
**Unit Inverter**

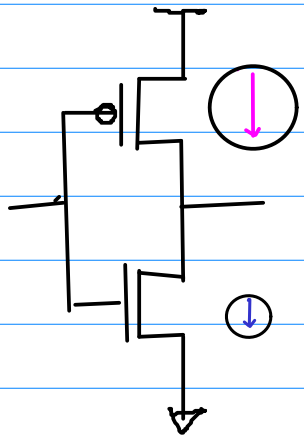


$\left(\frac{W}{L}\right)_p = 2 \left(\frac{W}{L}\right)_n$

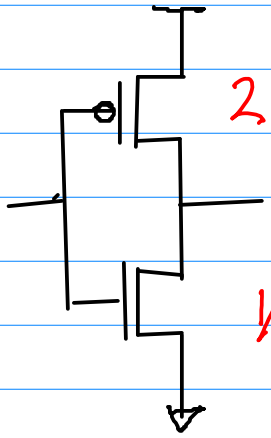



**High Skewed Inverter**

rise delay : faster

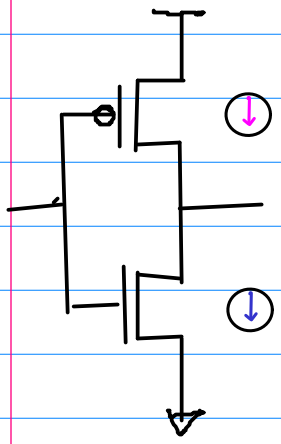


$\left(\frac{W}{L}\right)_p = 4 \left(\frac{W}{L}\right)_n$



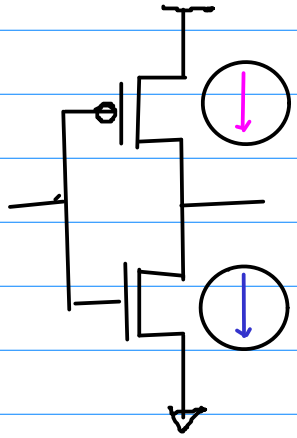
# High Skewed Inverter

**Unskewed Inverter**



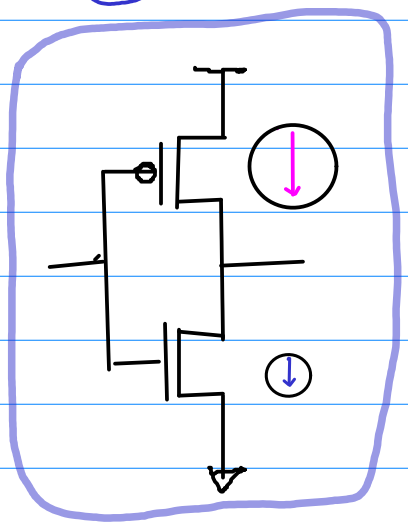
**Unskewed Inverter**

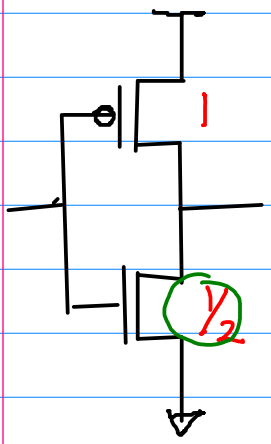
**Unit Inverter**



**High Skewed Inverter**

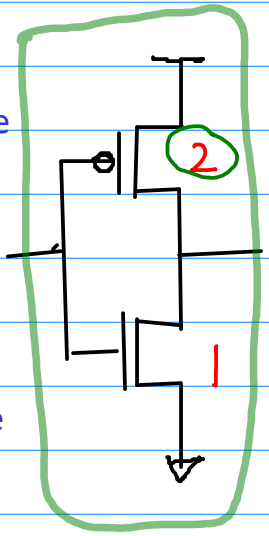
rise delay : faster



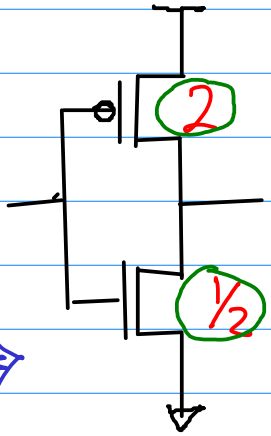



reduce pMOS size

reduce nMOS size




reduce nMOS size




**Unskewed Inverter**

**Unskewed Inverter**

**High Skewed Inverter**

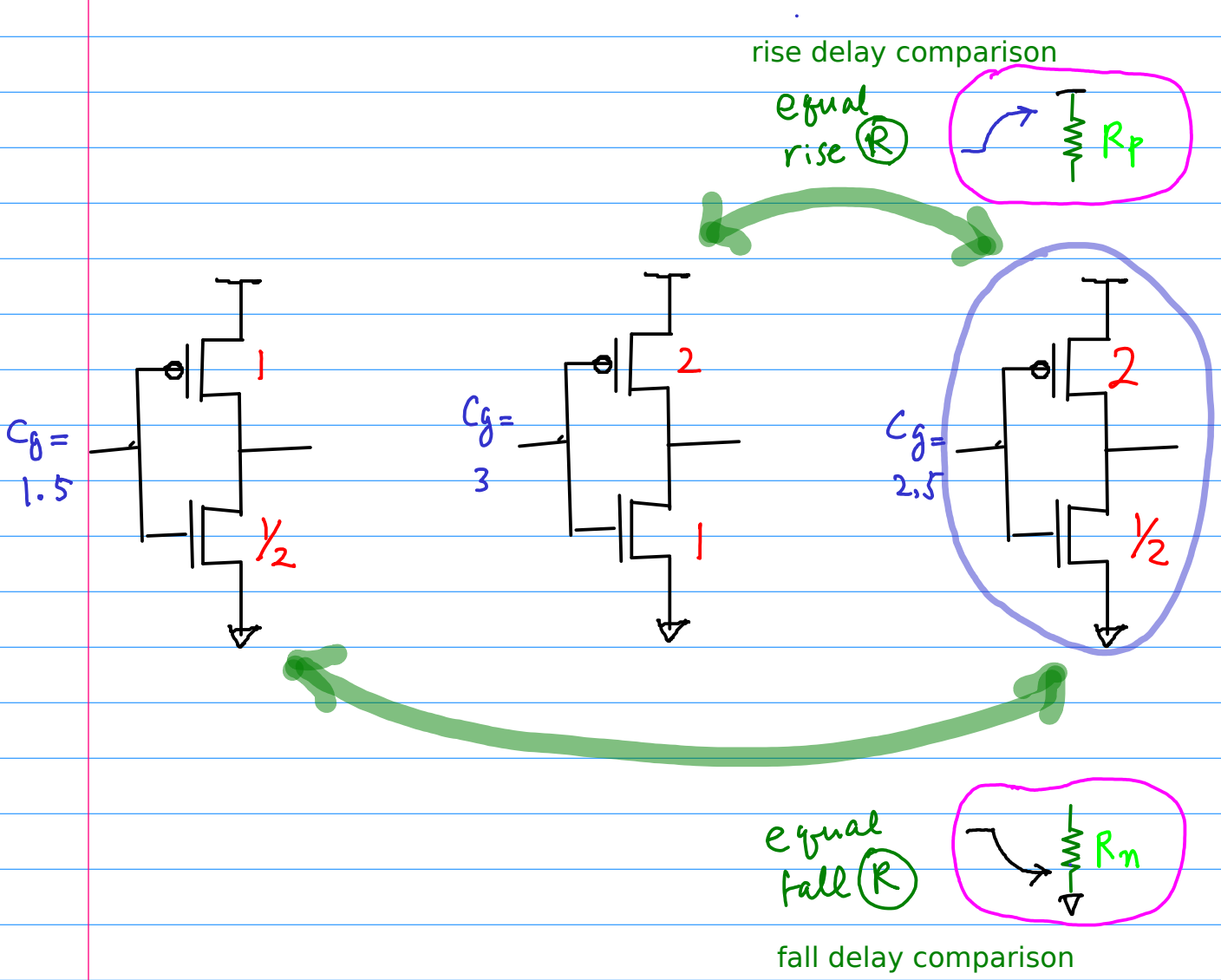
**Unskewed Inverter**

**Unskewed Inverter**

**Unit Inverter**

**High Skewed Inverter**

rise delay : faster




Logic Efftor : the same output current I
==> the same resistance

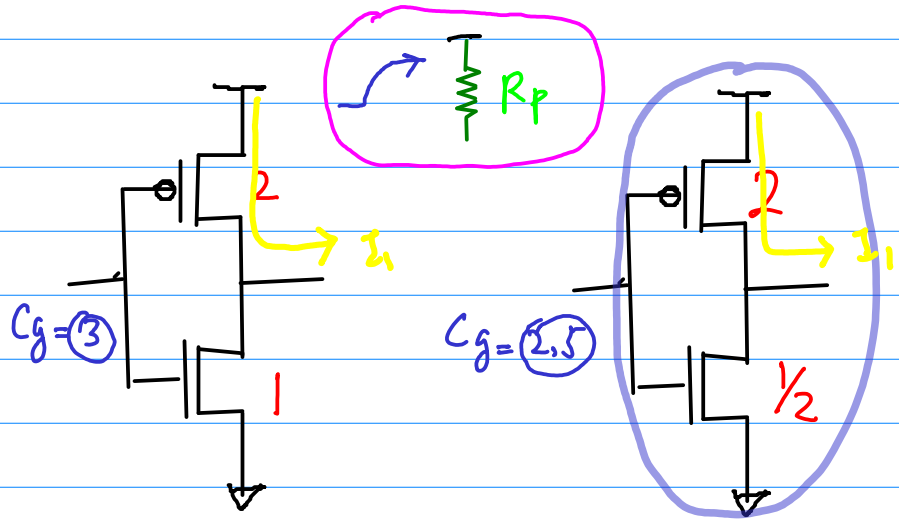
**Unskewed Inverter**

**Unskewed Inverter**

**Unit Inverter**

**High Skewed Inverter**

rise delay : faster




rise logical effort

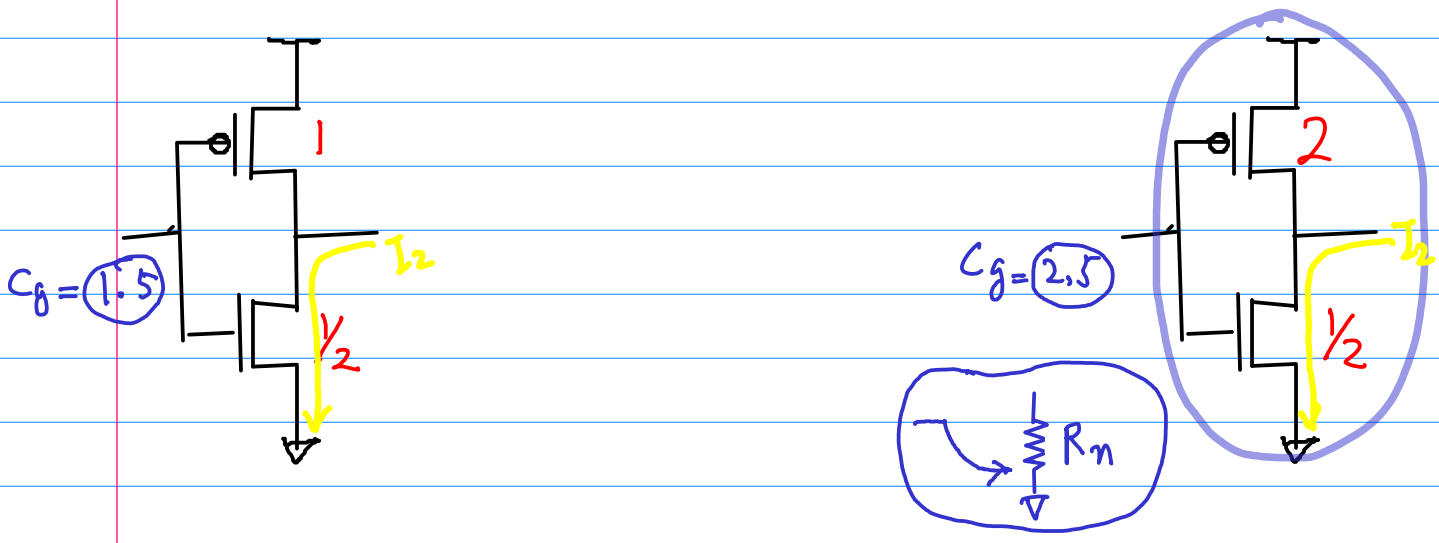
Gu = 2.5/3 = 5/6 < 1

$\Rightarrow$

reduced rise logical effort

better rise delay

$\propto GH$




fall logical effort

Gd = 2.5 / 1.5 = 5/3 > 1

$\Rightarrow$

increase fall logical effort

worse fall delay

$\propto GH$

**Unskewed Inverter**

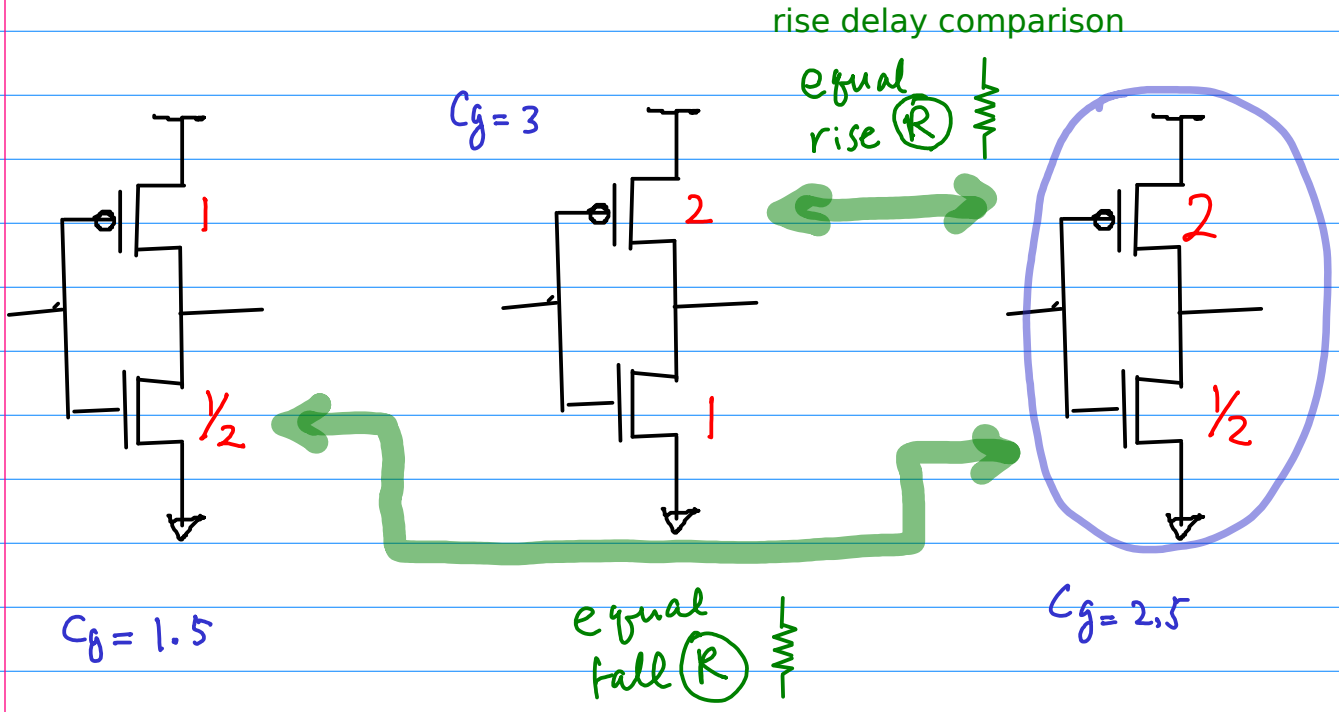
**Unit Inverter * 1/2**

**Unskewed Inverter**

**Unit Inverter**

**High Skewed Inverter**

rise delay : faster




Gu = 2.5/3 = 5/6 < 1

reduced rise logical effort

at the expense of increased fall logical effort

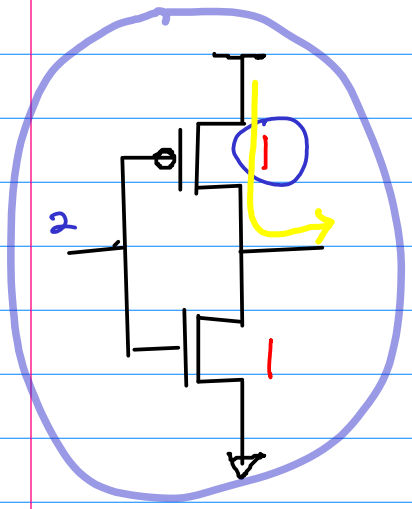
Gd = 2.5 / 1.5 = 5/3 > 1

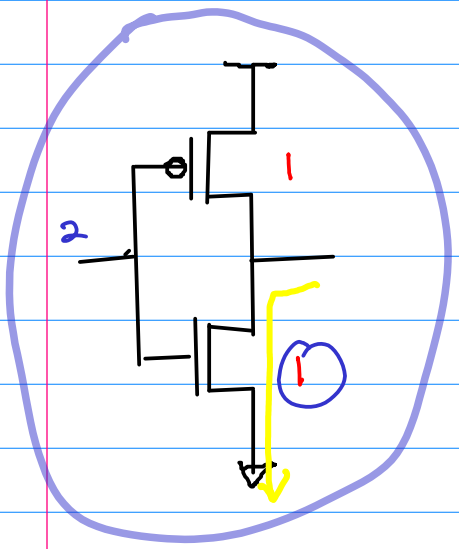
⇒ suitalbe for rise delay critical application

i.e. when it is more important to reduce the rise delay than the fall delay

**Low Skewed Inverter**

fall delay : faster

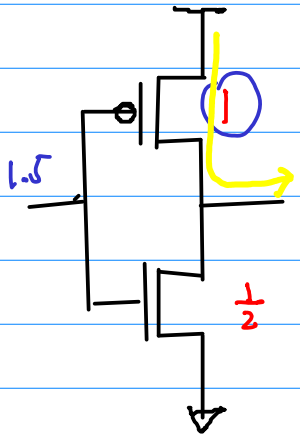


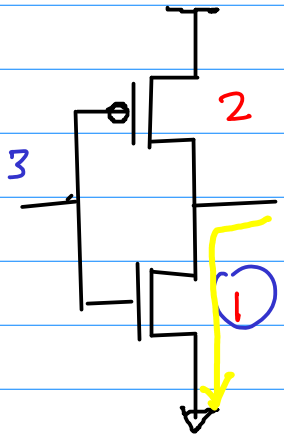

**Low Skewed Inverter**

**Unskewed Inverter**

**Unit Inverter * 1/2**




$g_u = \frac{2}{1.5} = \frac{4}{3} > 1$




$g_d = \frac{2}{3} < 1$

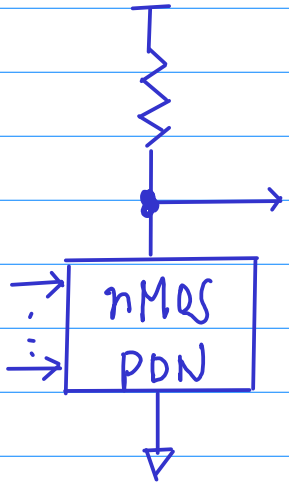
**Unskewed Inverter**

**Unit Inverter**

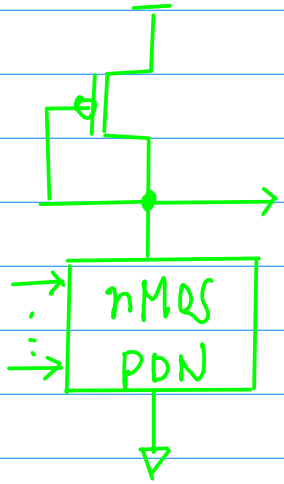
suitalbe for fall delay
critical application

# Ratioed Logic

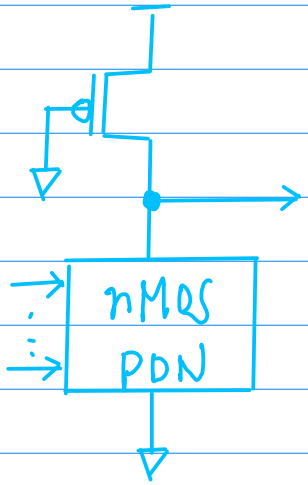
resistive load

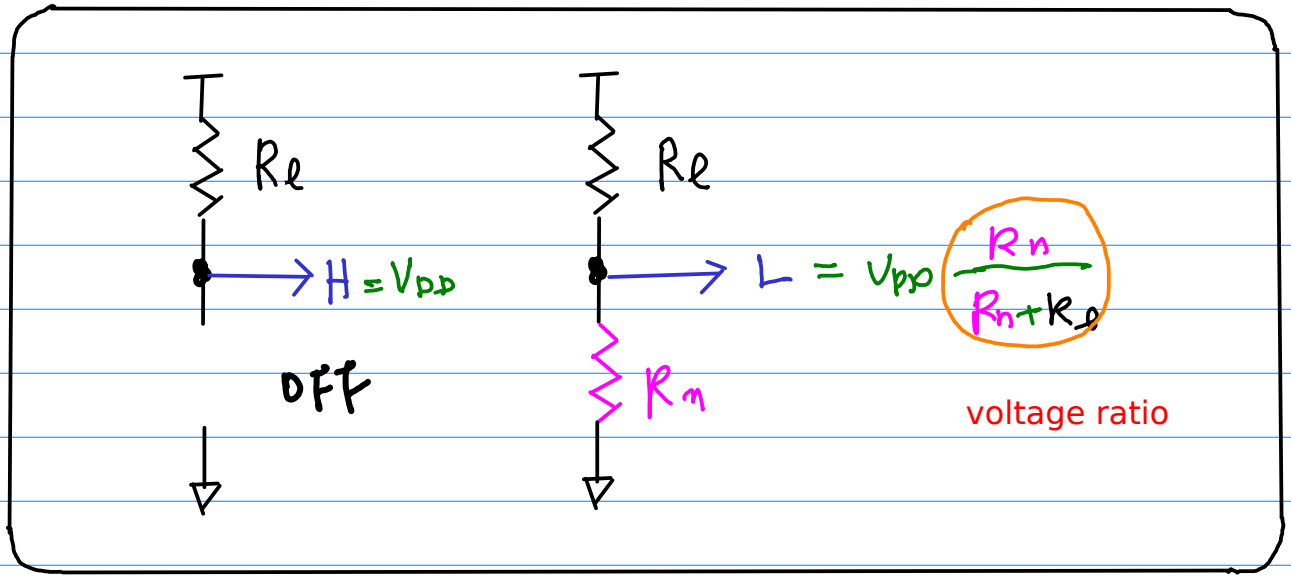



depletion load




pseudo-nMOS



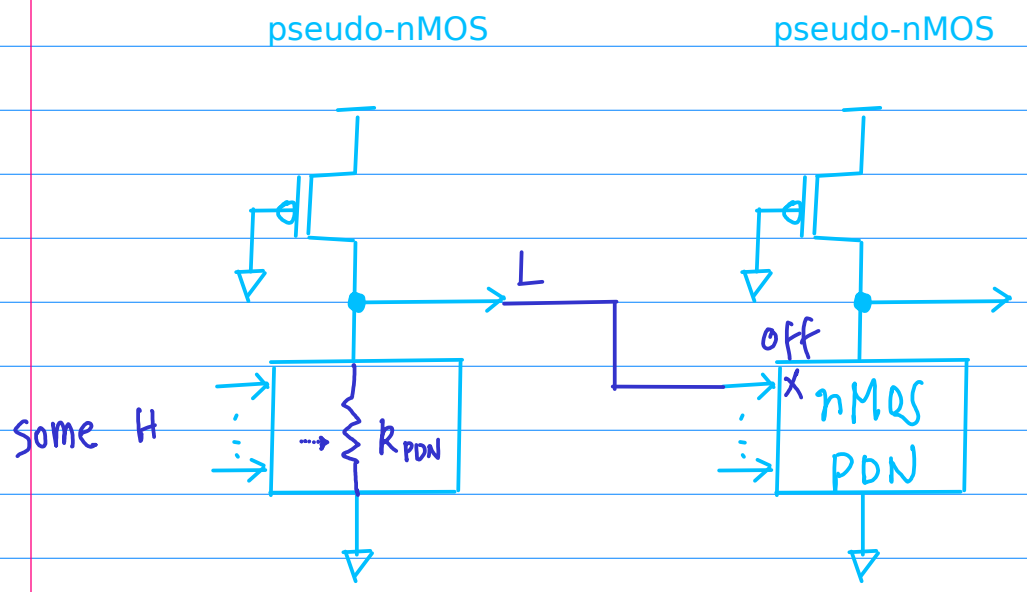

weak pMOS

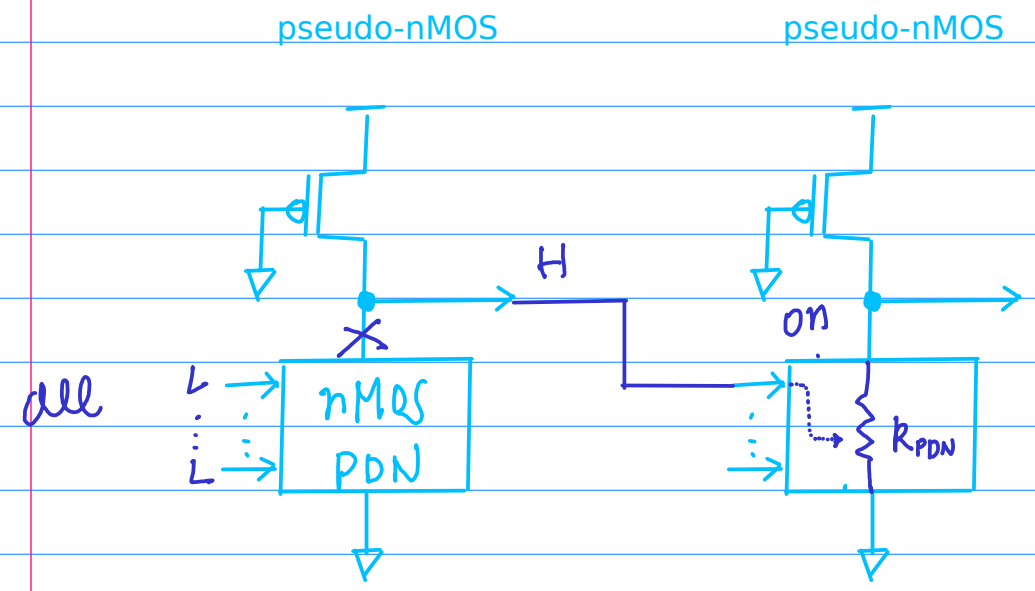
$R_\ell \uparrow$ → $L \to 0$ NM ↑

$R_\ell \uparrow$ → rise delay ↑

Conflicting

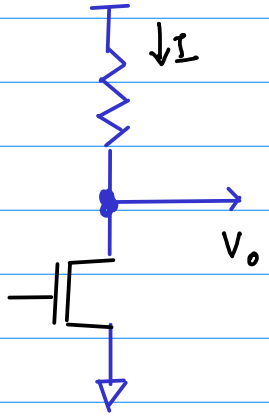
# Cascade Connections of Ratioed Logic



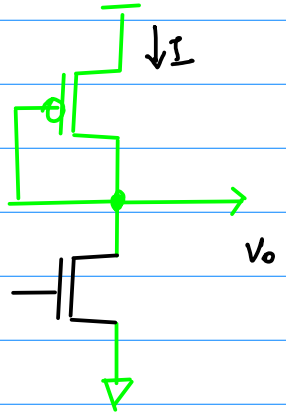



# Load Lines of Ratioed Logic

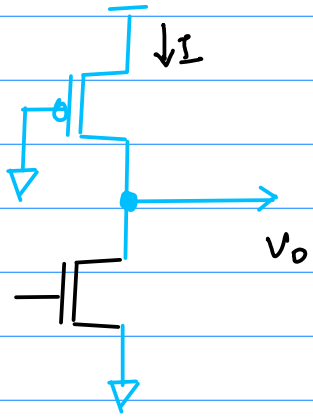
resistive load

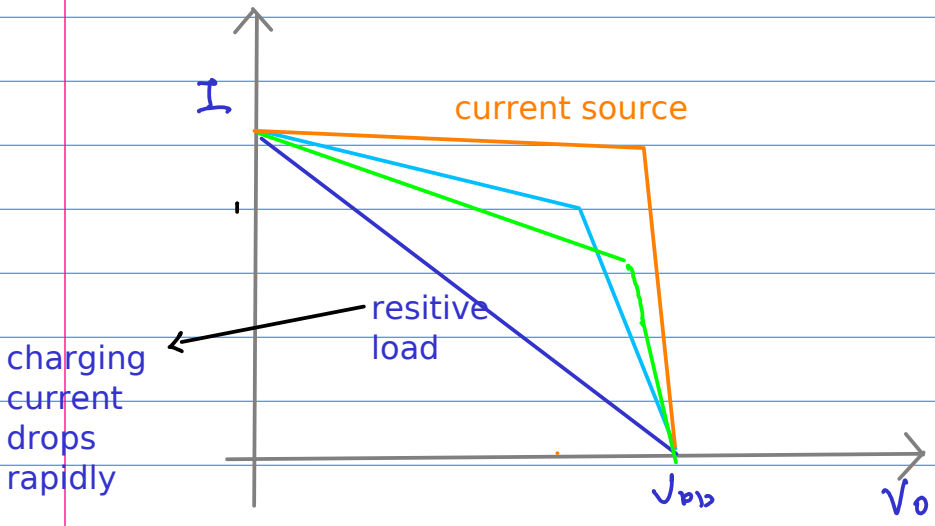


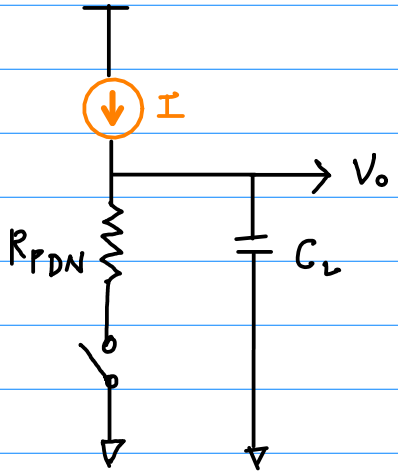

depletion load



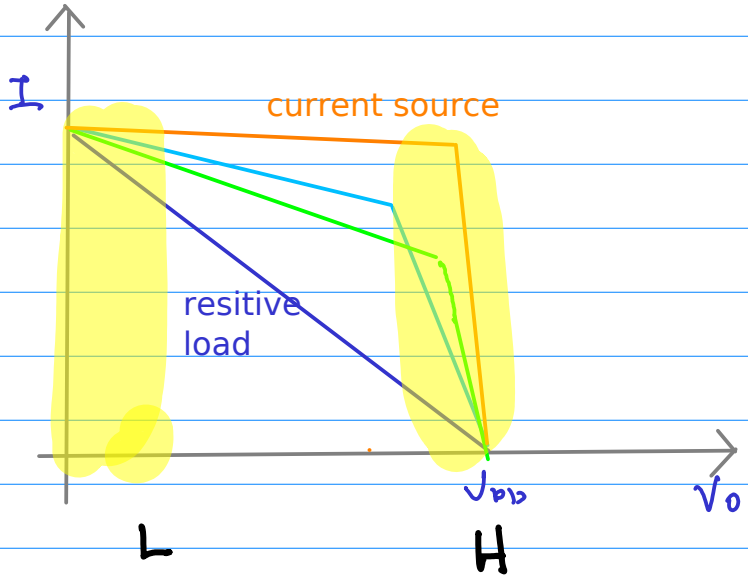

pseudo-nMOS



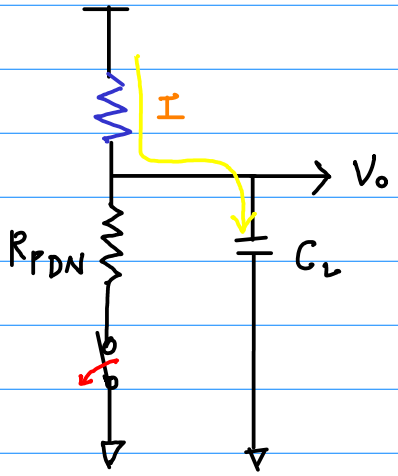



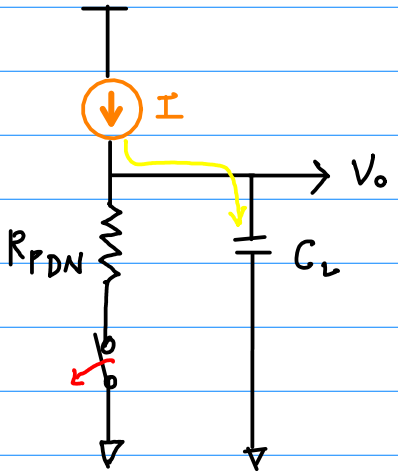




ideal model
current source

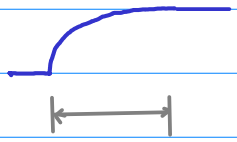


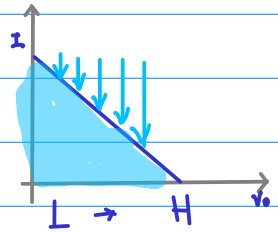
# Charging Current Aspect



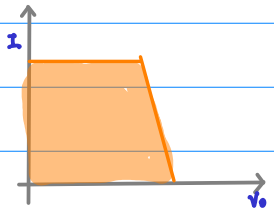

$t_{PLH}$ : large



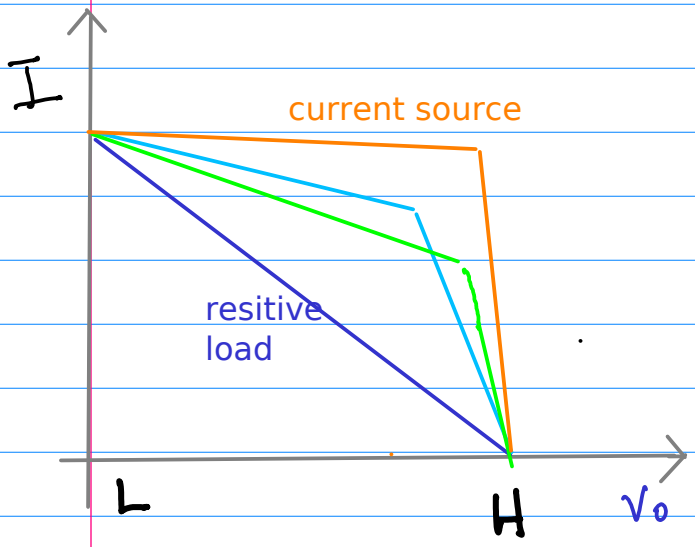


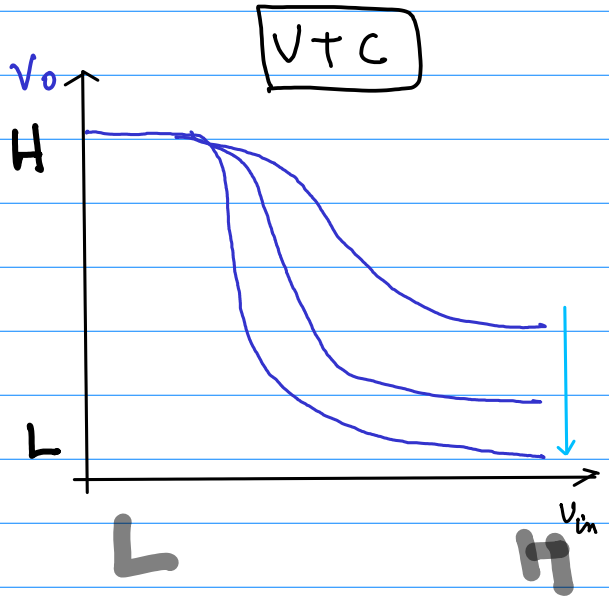

charging current drops rapidly

$t_{PLH}$ : small

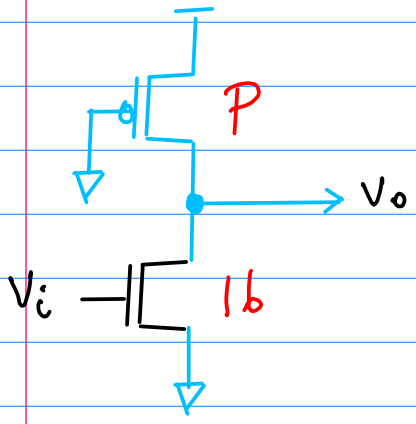


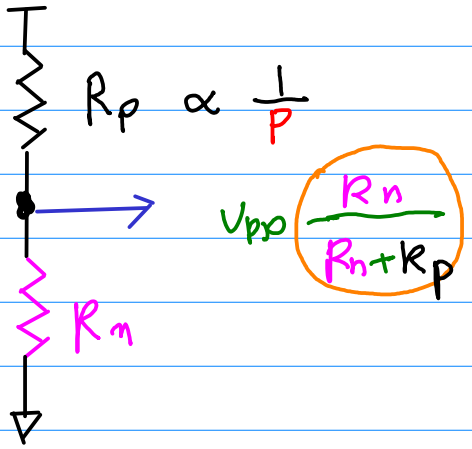

takes shorter time

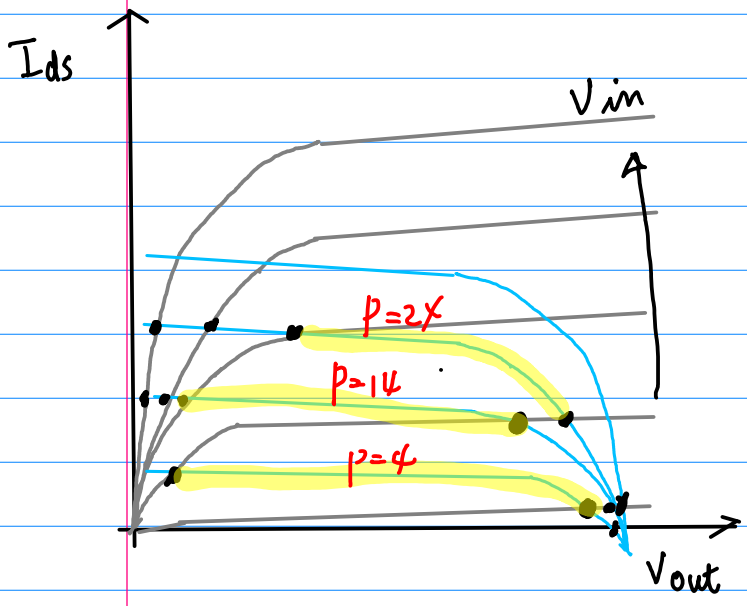


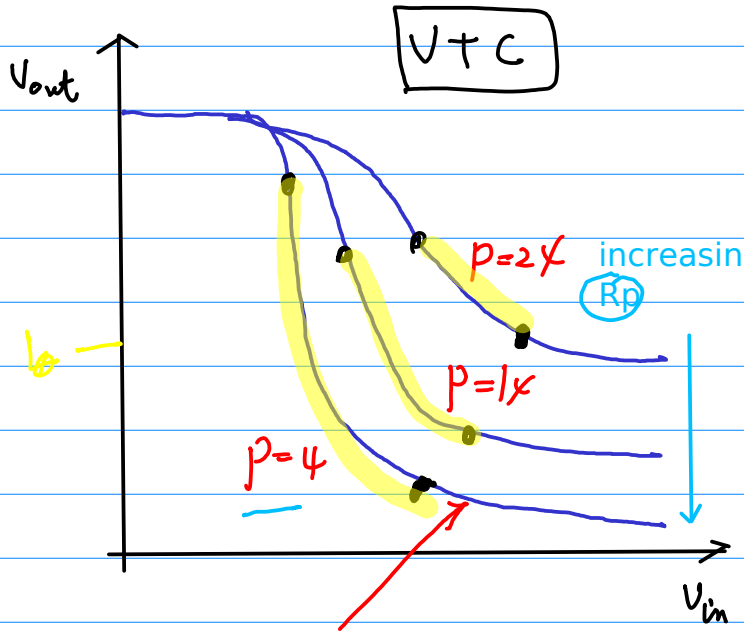



pseudo-nMOS




the weakest pMOS

weak pMOS

$R_p \uparrow$ → L → 0 NM ↑

$R_p \uparrow$ → rise delay ↑

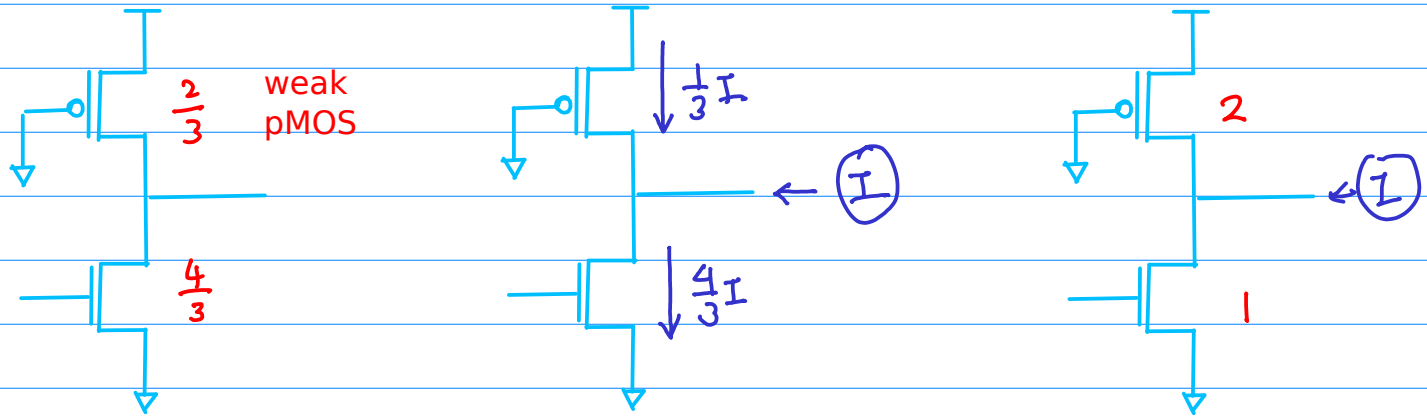
conflicting

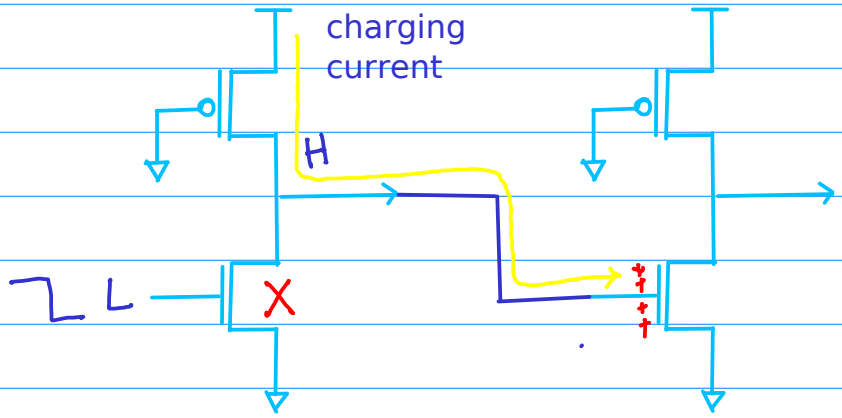
**Low Skewed Inverter**

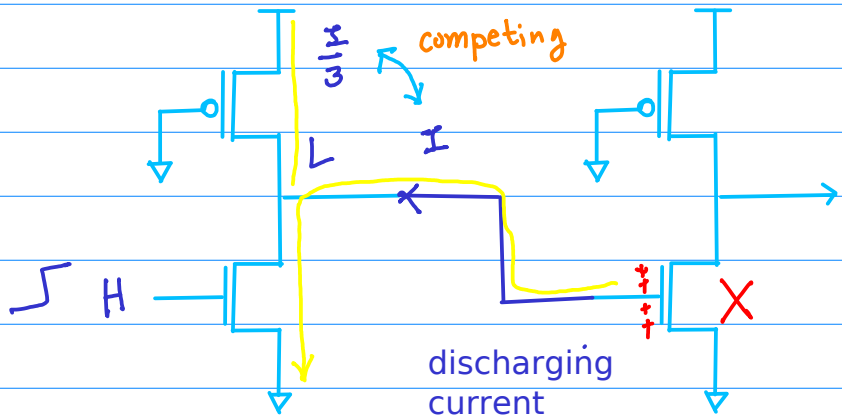
fall delay : faster

**Unskewed Inverter**

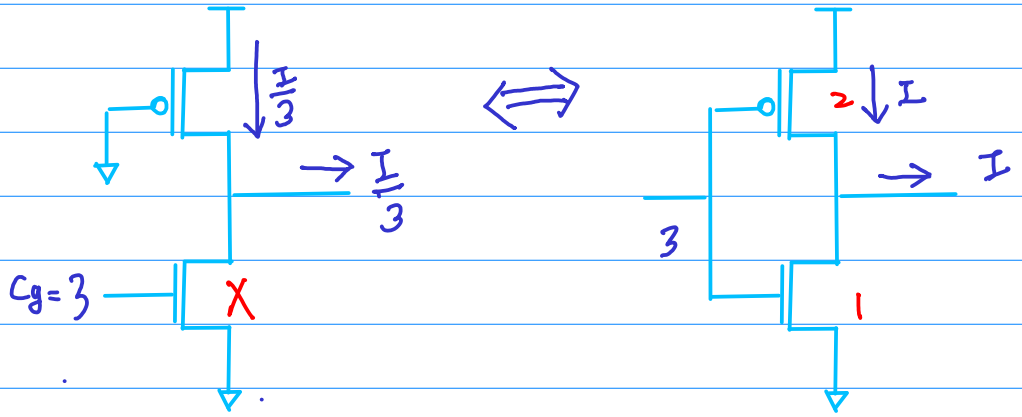
**Symmetric Inverter**
**Unit Inverter**



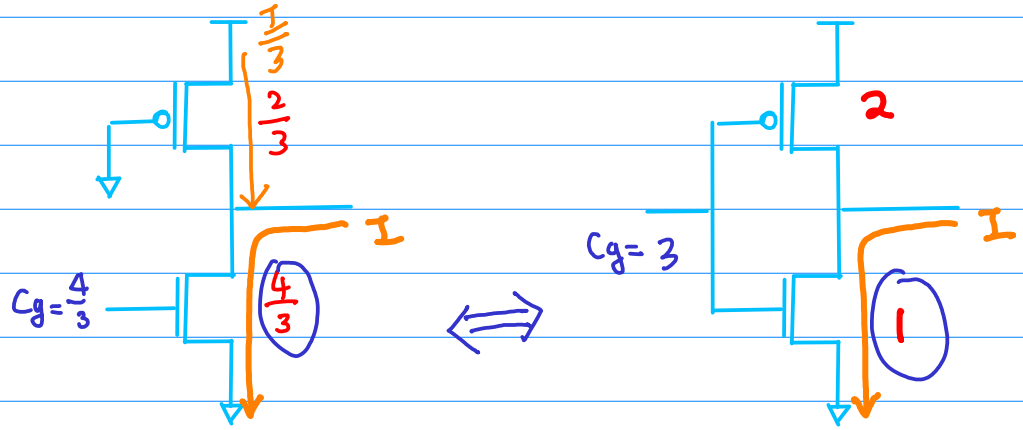



Unskewed Inverter




$g_u = g_d \times 3 = \frac{4}{9} \times 3 = \frac{4}{3} > 1$

Unskewed Inverter




$g_d = \frac{4}{3} / 3 = \frac{4}{9} < 1$