CMOS Sequential Circuits
Seq-3 (H.3)

20151215

References

Some Figures from the following sites

[1] http://pages.hmc.edu/harris/cmosvlsi/4e/index.html
Weste & Harris Book Site

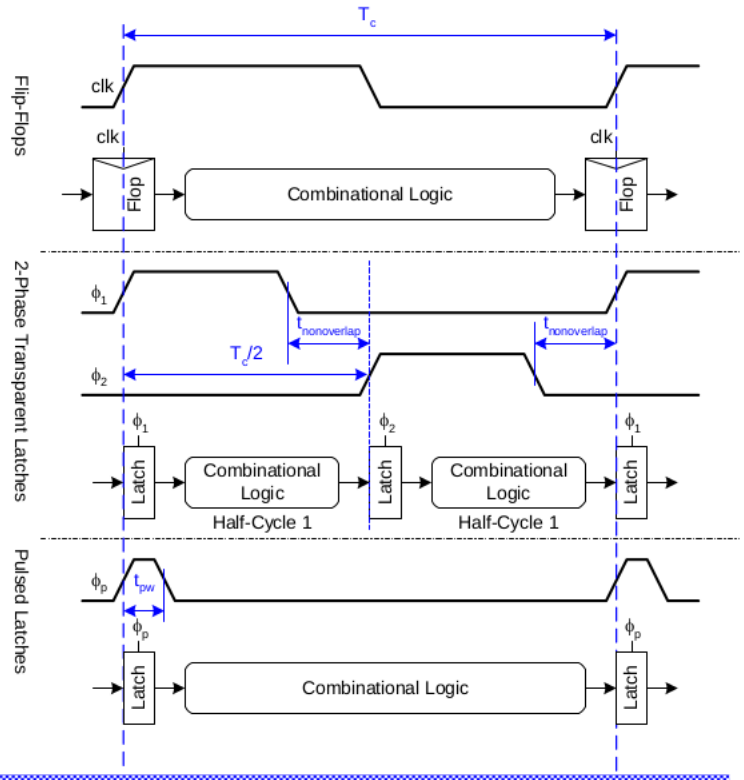
[2] en.wikipedia.org

[3] Digital Integrated Circuits : A Design Perspective,
Jan M. Rabaey,
(http://bwrcs.eecs.berkeley.edu/Classes/IcBook/)

[4] Digital Electronics and Design with VHDL
Pedroni

Sequencing Methods

- Flip-flops
- 2-Phase Latches
- Pulsed Latches

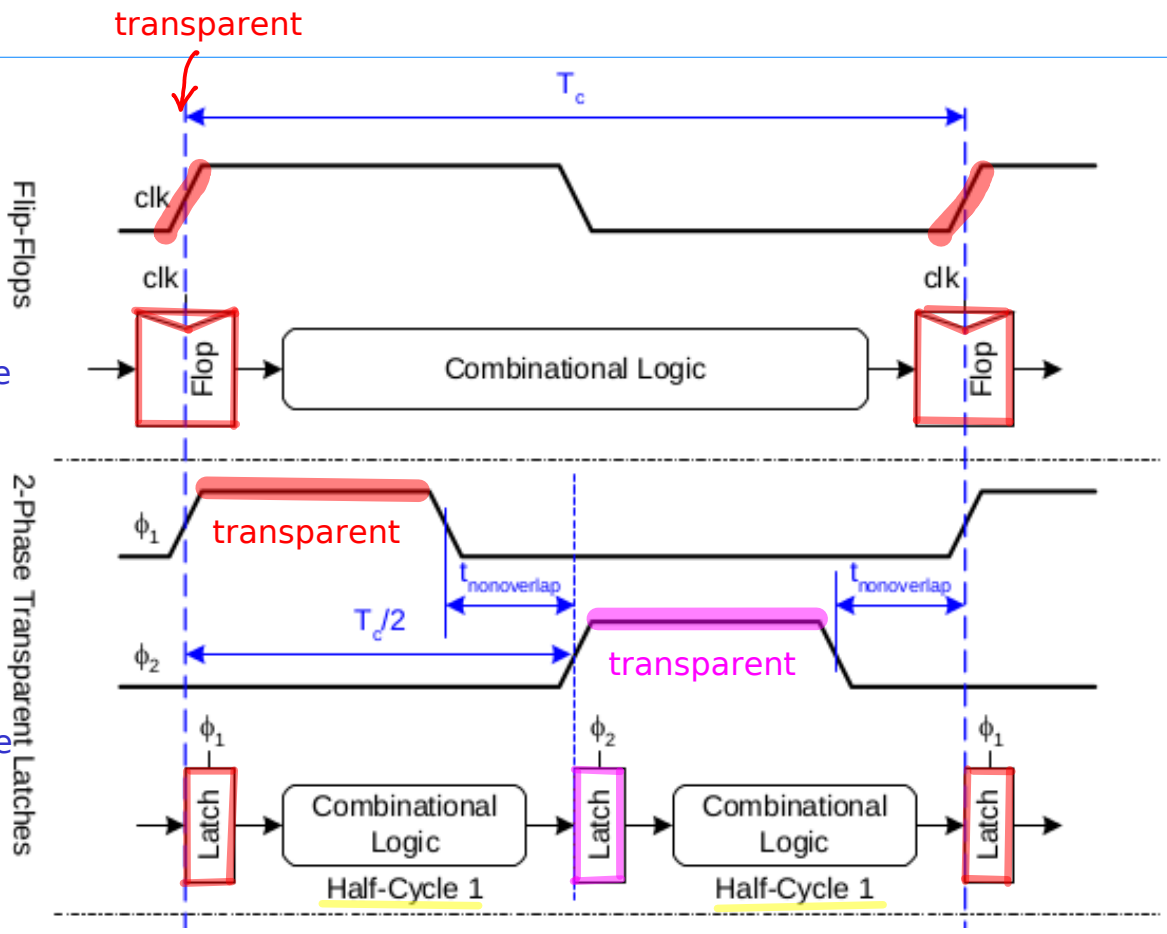


FF

edge sensitive

level sensitive

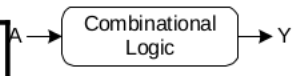
Latch

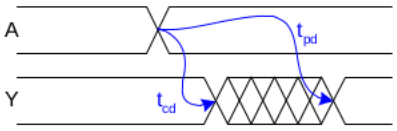


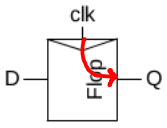
Timing Diagrams

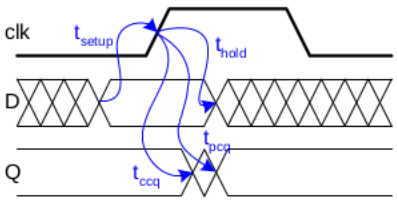
Contamination and Propagation Delays

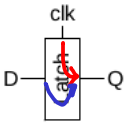
t_{pd}	Logic Prop. Delay
t_{cd}	Logic Cont. Delay
t_{pcq}	Latch/Flop Clk->Q Prop. Delay
t_{ccq}	Latch/Flop Clk->Q Cont. Delay
t_{pdq}	Latch D->Q Prop. Delay
t_{cdq}	Latch D->Q Cont. Delay
t_{setup}	Latch/Flop Setup Time
t_{hold}	Latch/Flop Hold Time

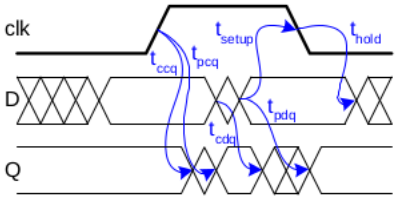




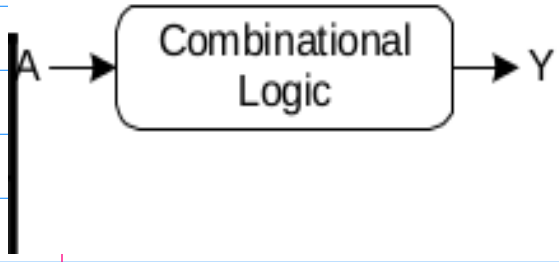


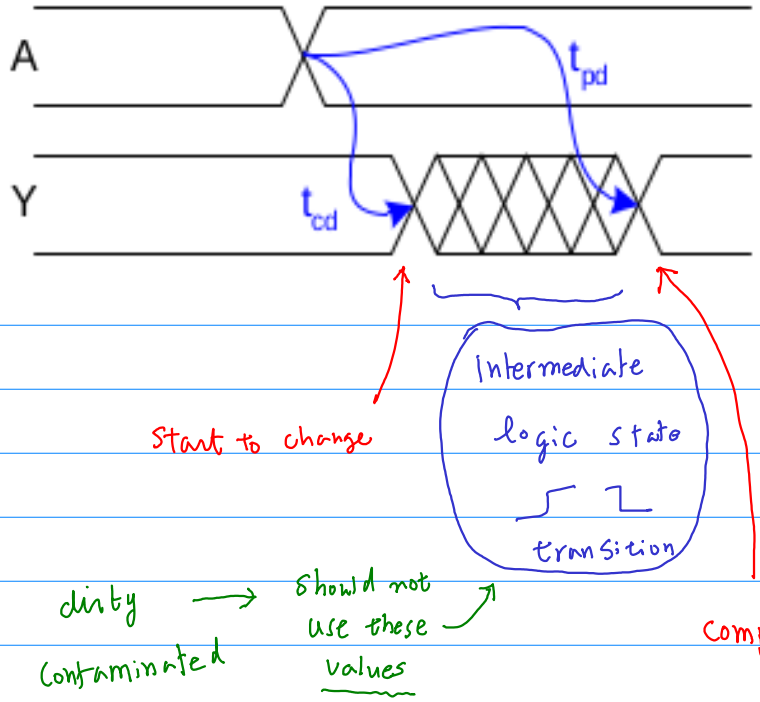


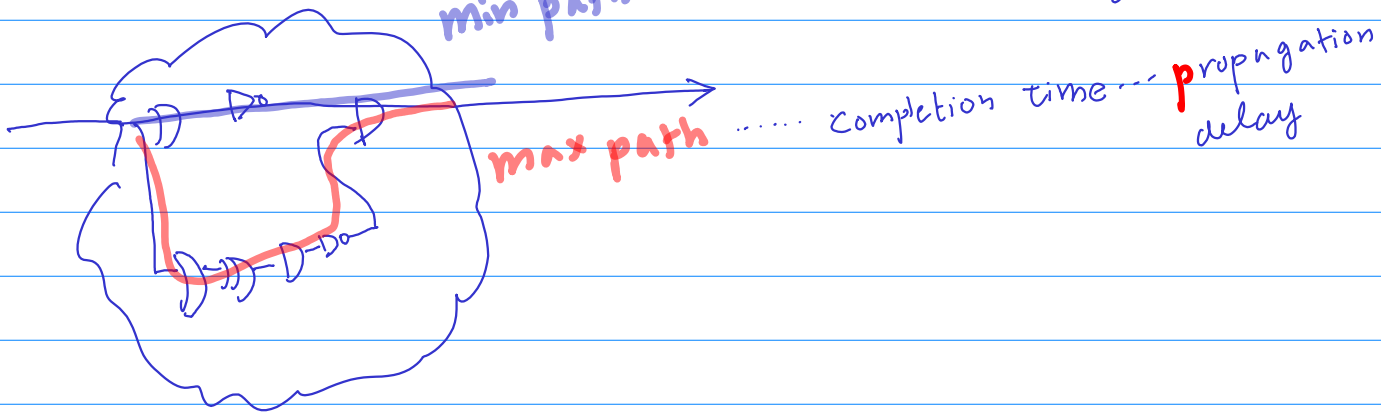




Logic Delay



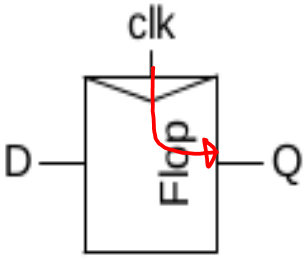


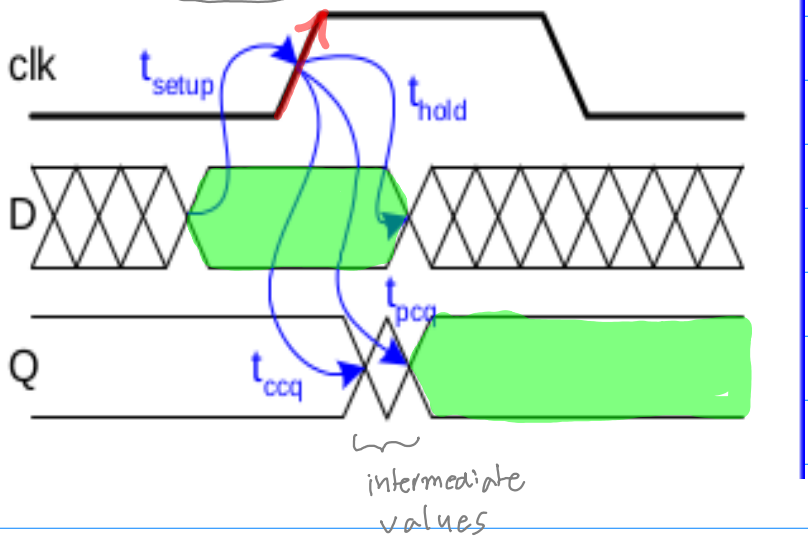


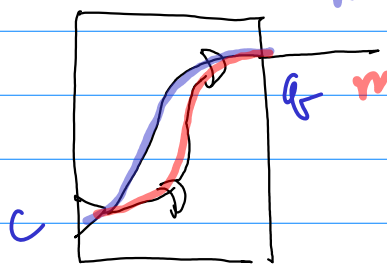
t_{pd}	Logic Prop. Delay
t_{cd}	Logic Cont. Delay

Clock to Output Delay (Flipflop)

at the posedge, must sample clean value







min path — start time — contamination delay

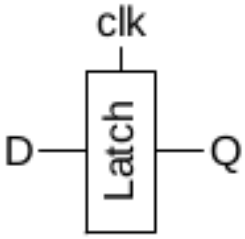
max path — completion time — propagate delay

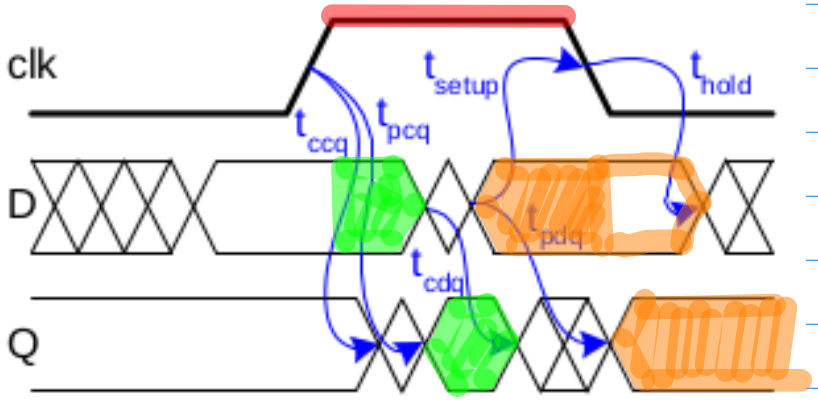
t_{pcq}	Latch/Flop Clk->Q Prop. Delay
t_{ccq}	Latch/Flop Clk->Q Cont. Delay

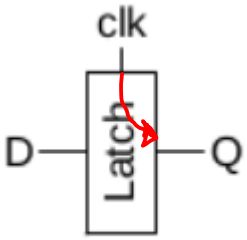
max min

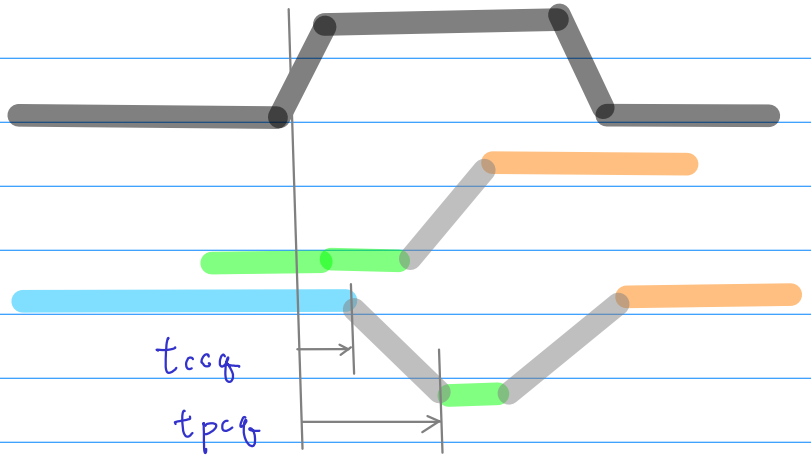
cq

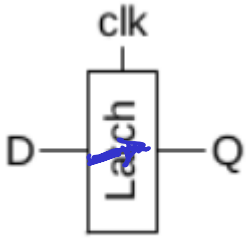
Clock to Output Delay (Latch)

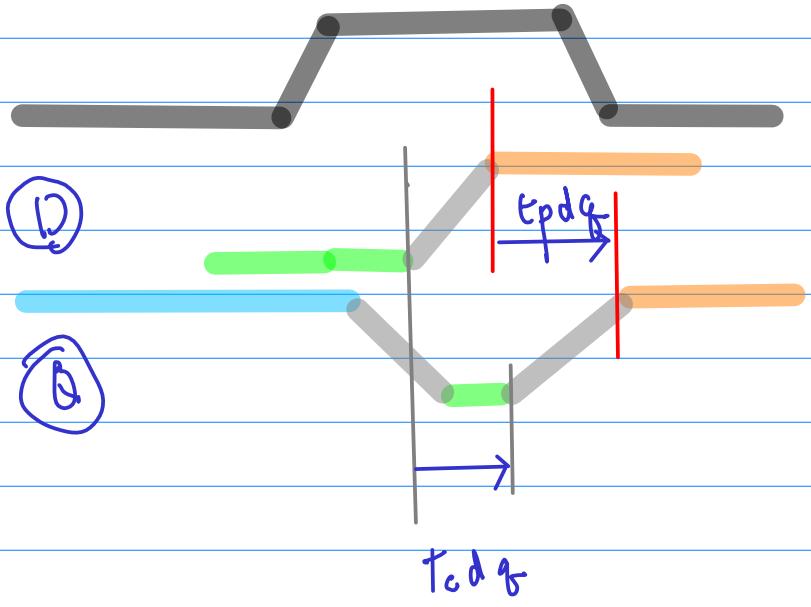






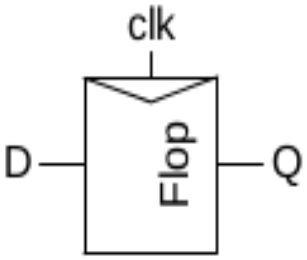


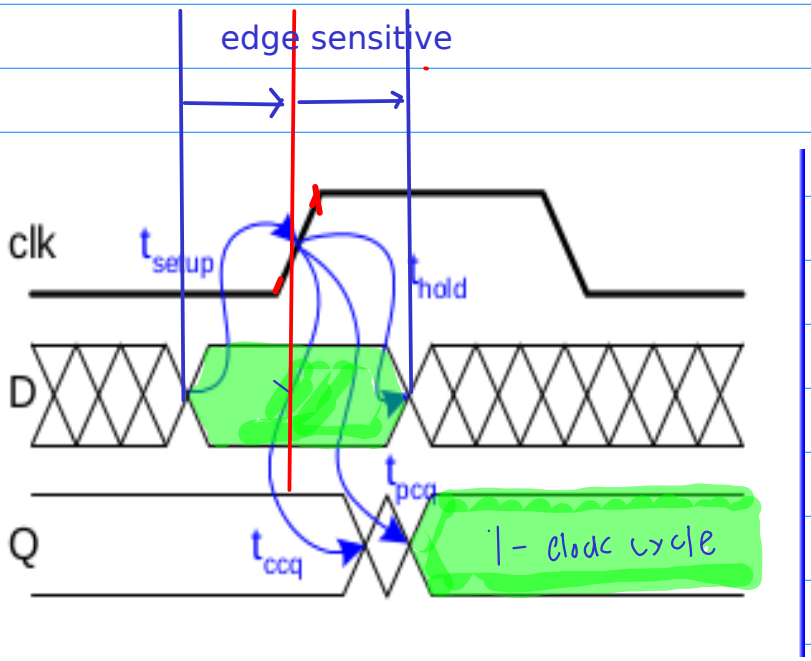


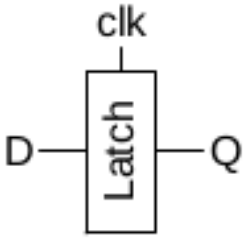


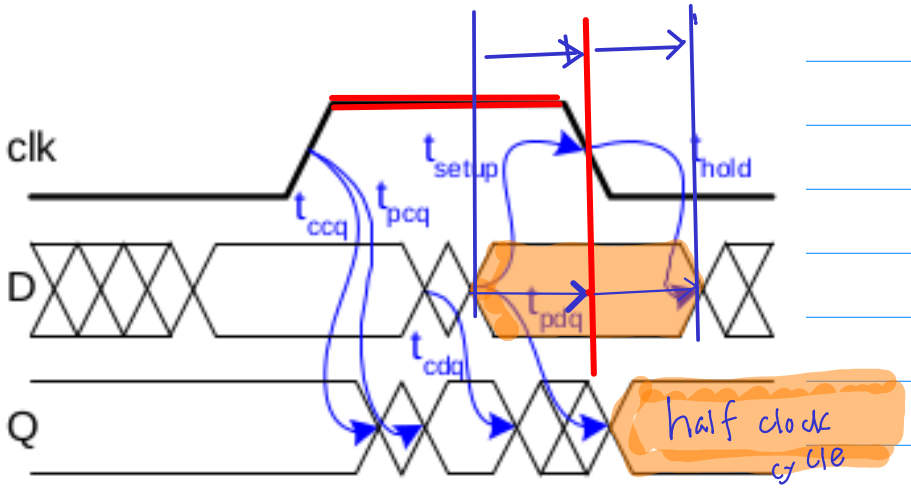
t_{pcq}	Latch/Flop Clk->Q Prop. Delay
t_{ccq}	Latch/Flop Clk->Q Cont. Delay
t_{pdq}	Latch D->Q Prop. Delay
t_{cdq}	Latch D->Q Cont. Delay

Setup & Hold Time (Latch & FF)





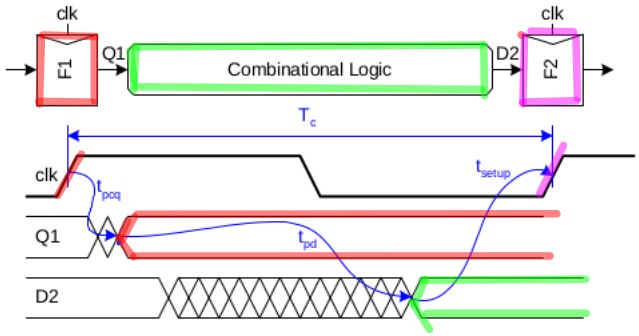




Max-Delay Path Constraints (FF)

Max-Delay: Flip-Flops

$$t_{pd} \leq T_c - \underbrace{(\quad)}_{\text{sequencing overhead}}$$

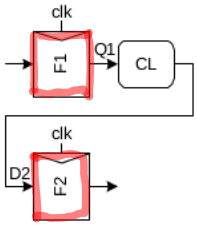


$$t_{pcq} + t_{pd} + t_{setup} \leq T_c$$

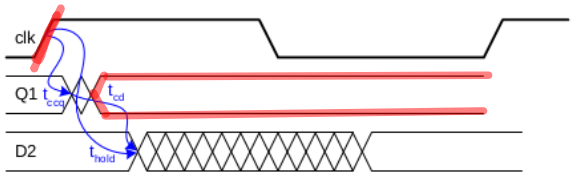
Min-Delay Path Constraints (FF)

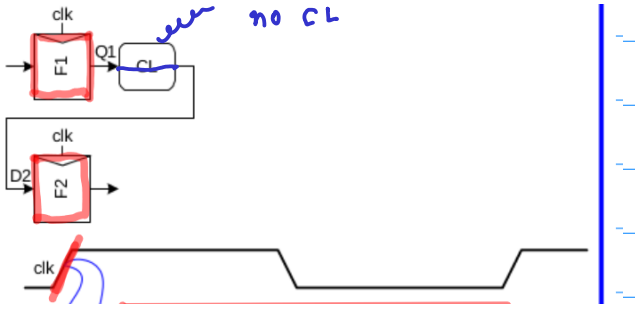
Min-Delay: Flip-Flops

$t_{cd} \geq$

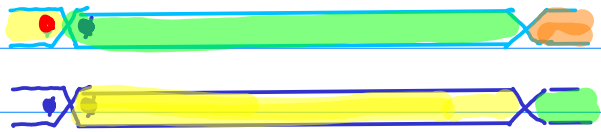


$t_{ccq} + t_{pcd} > t_{hold}$

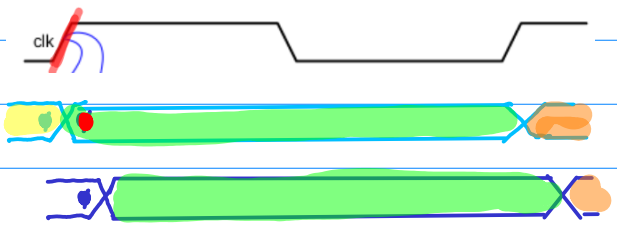




normal



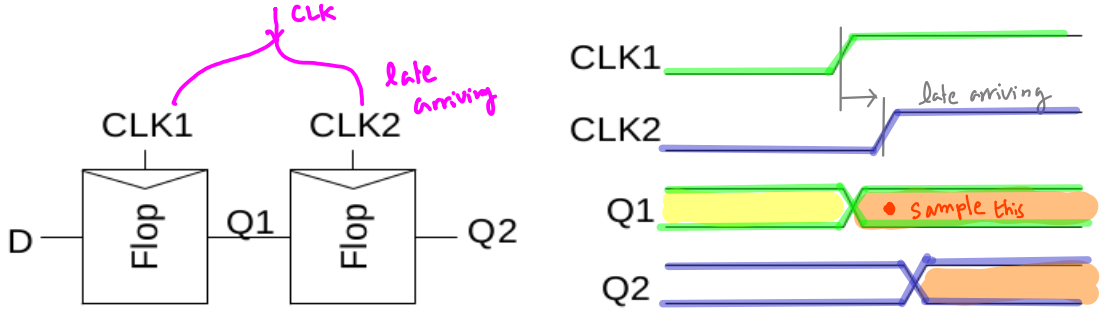
too fast

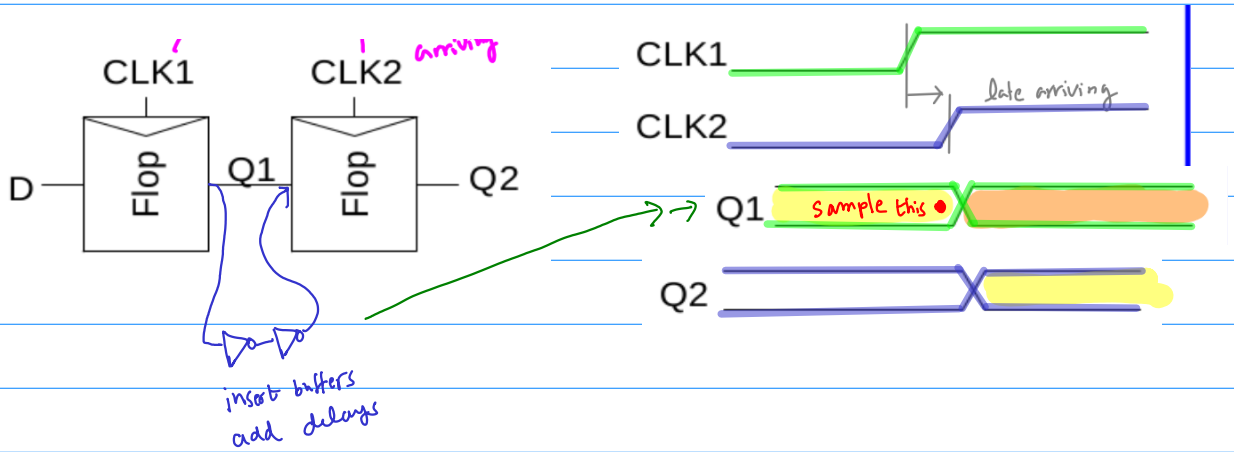


Hold Time Violation (FF)

Race Condition

- Back-to-back flops can malfunction from clock skew
  - Second flip-flop fires late
  - Sees first flip-flop change and captures its result
  - Called *hold-time failure* or *race condition*

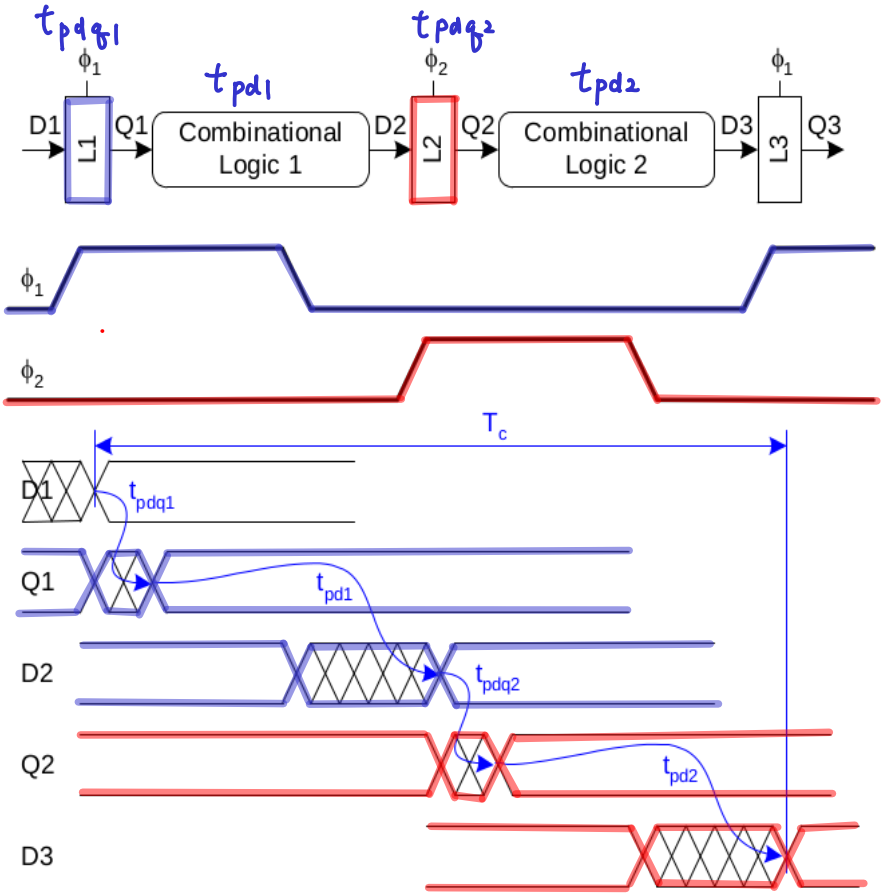




Max-Delay Path Constraints (Latch)

Max Delay: 2-Phase Latches

$$t_{pd} = t_{pd1} + t_{pd2} \leq T_c - \underbrace{(\quad)}_{\text{sequencing overhead}}$$



Min-Delay Path Constraints (Latch)

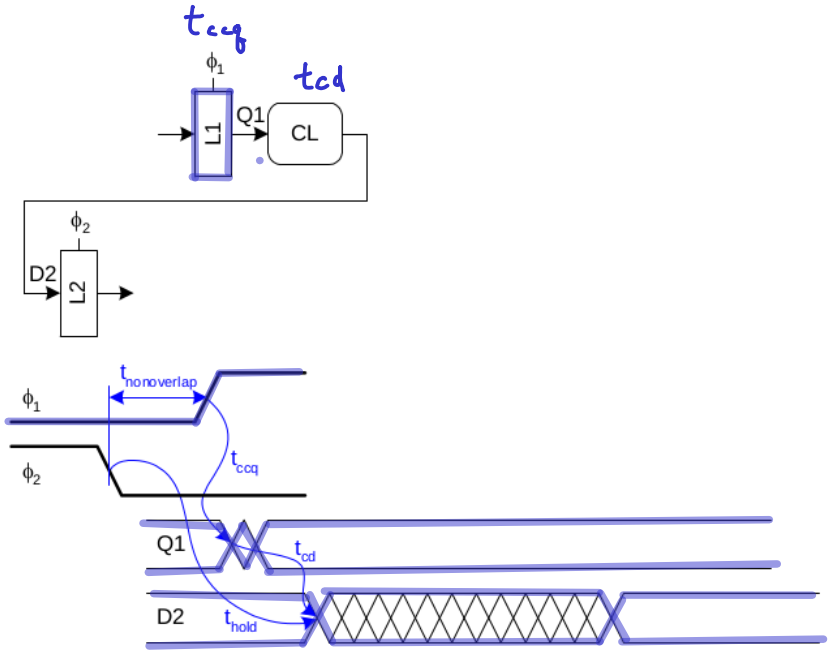
Min-Delay: 2-Phase Latches

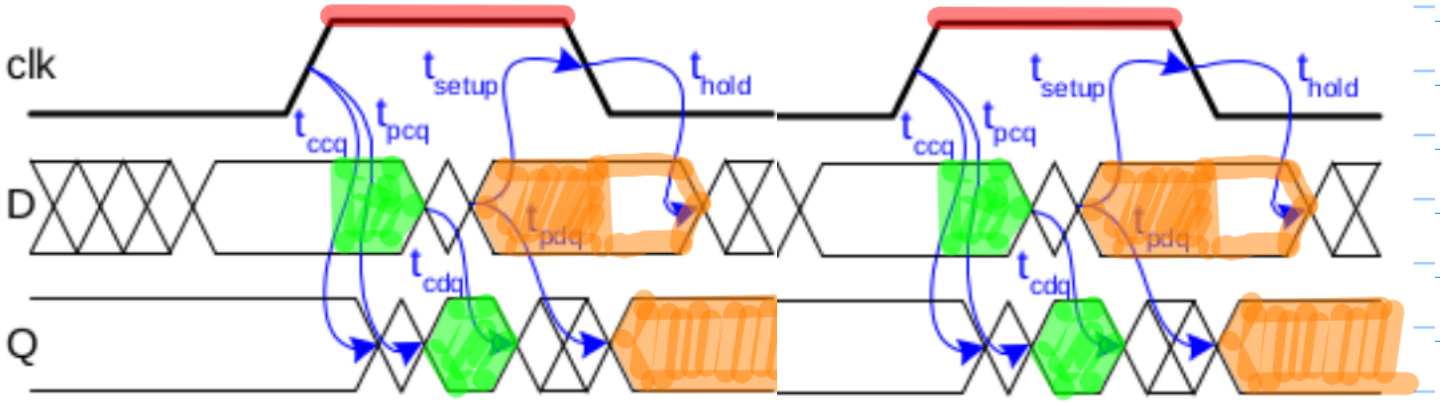
$t_{cd1}, t_{cd2} \geq$

Hold time reduced by nonoverlap

Paradox: hold applies twice each cycle, vs. only once for flops.

But a flop is made of two latches!




clk
D
Q
t_{setup}
t_{hold}
t_{ccq}
t_{pcq}
t_{pdq}
t_{cdq}
t_{setup}
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t_{pcq}
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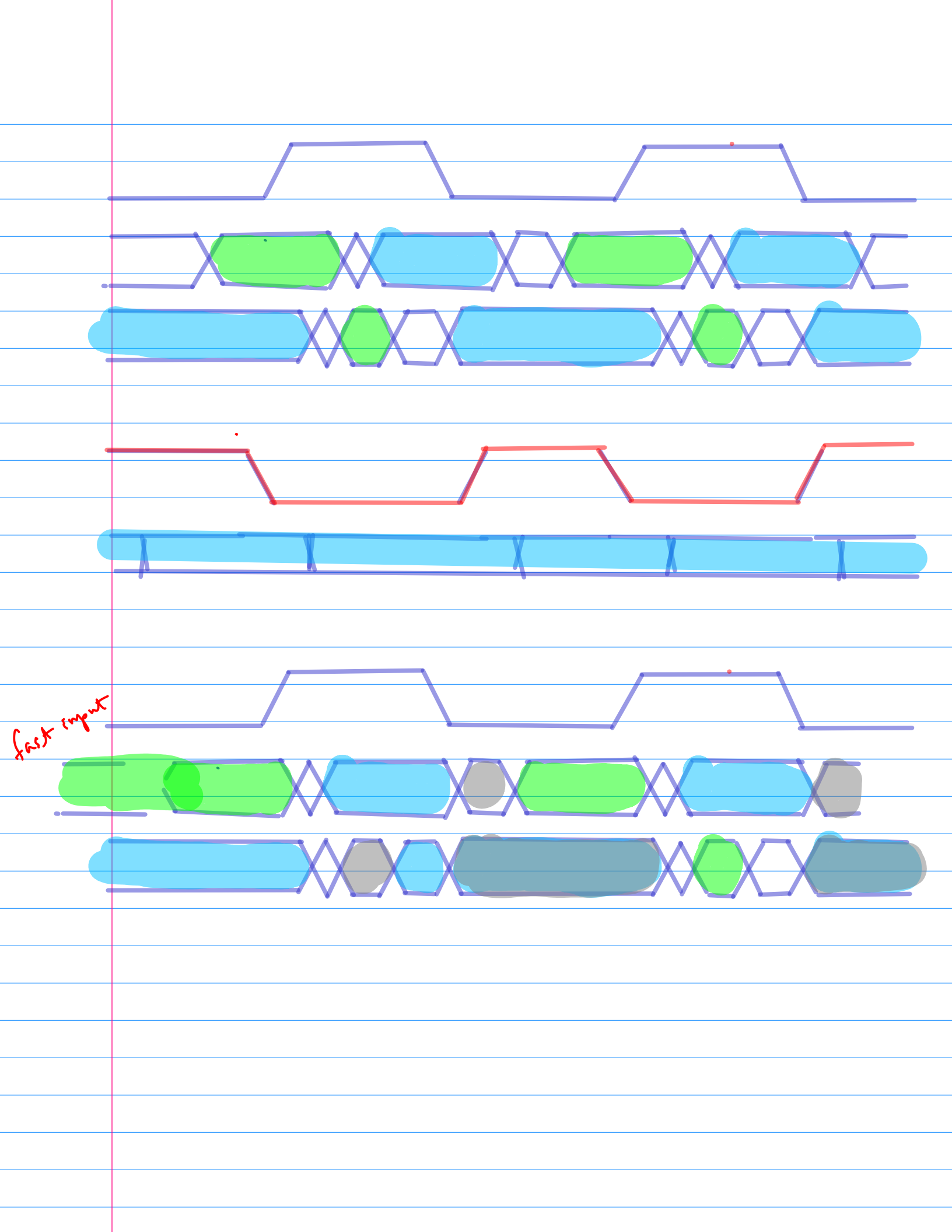
fast input