SRAM (H.1)

20151217

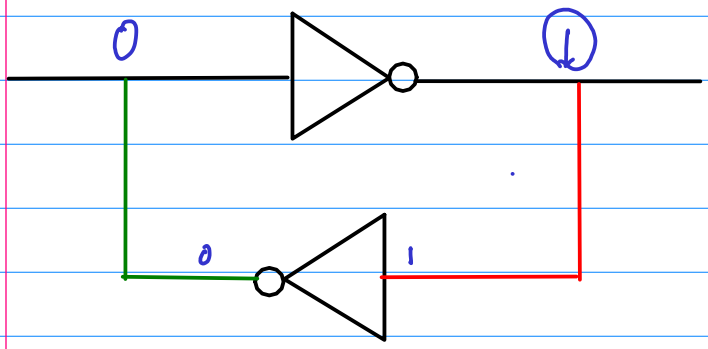
Static RAM (SRAM)

* Data stored as long as power is on
* Large area (6 transistors / cell)
* Fast access time
* Differential

Dynamic RAM (DRAM)

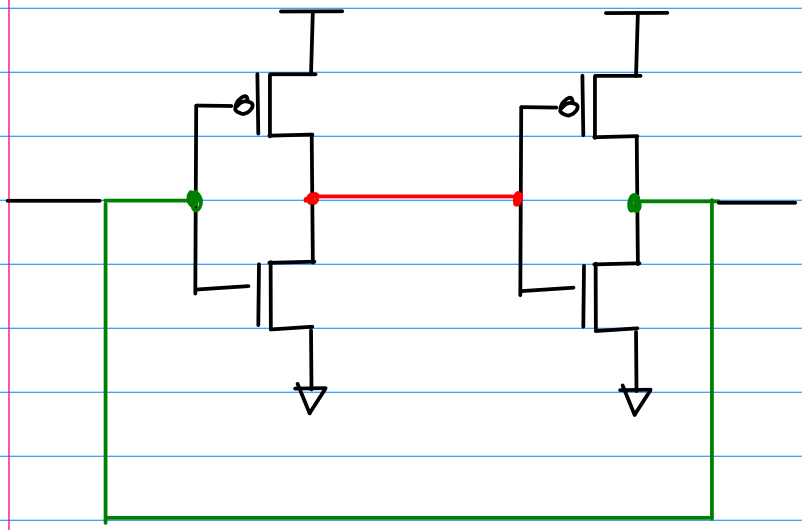
* Periodic refresh necessary
* Small area (1~3 transistors / cell)
* Slow access time
* Single ended

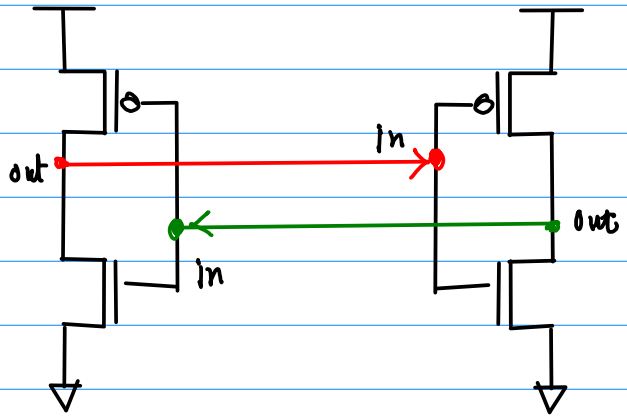
Back-to-back inverters : Latch



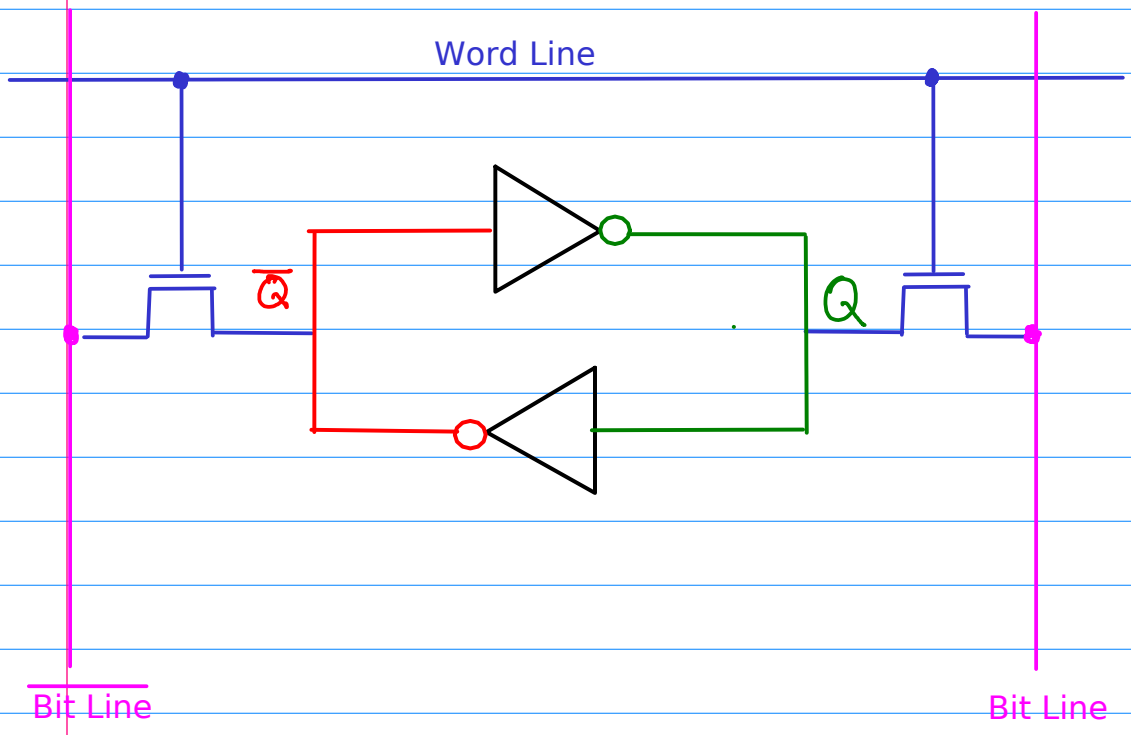
restoring charateristic

bistable





6-Tr CMOS SRAM Bit Cell



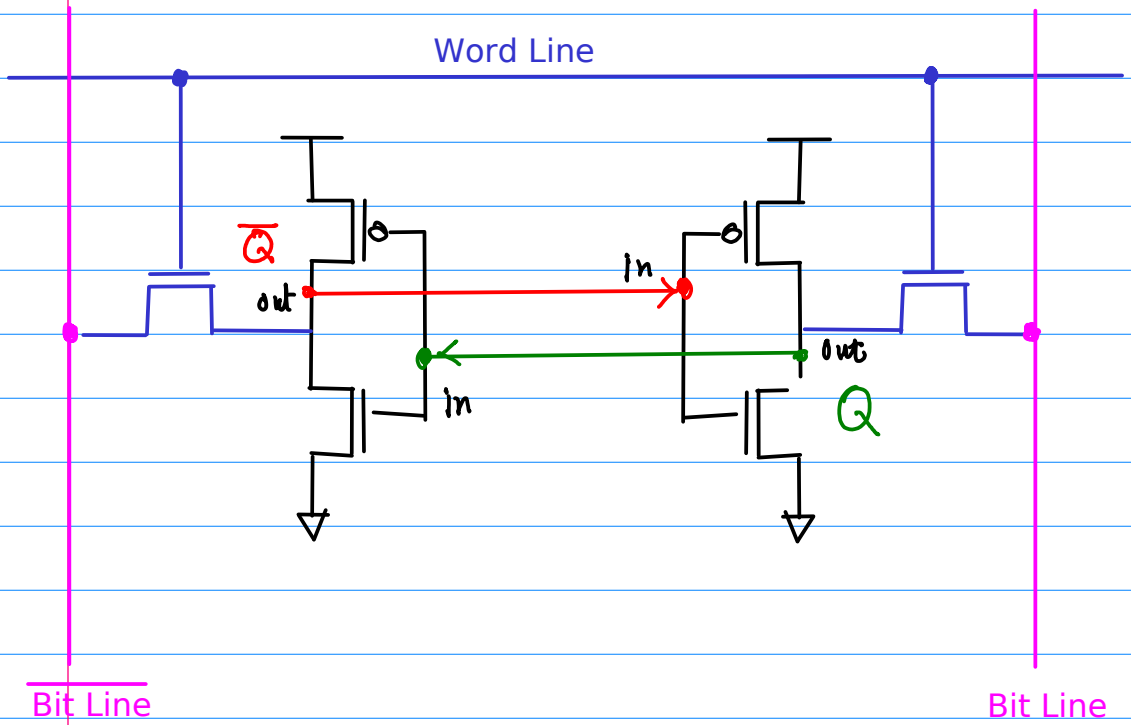
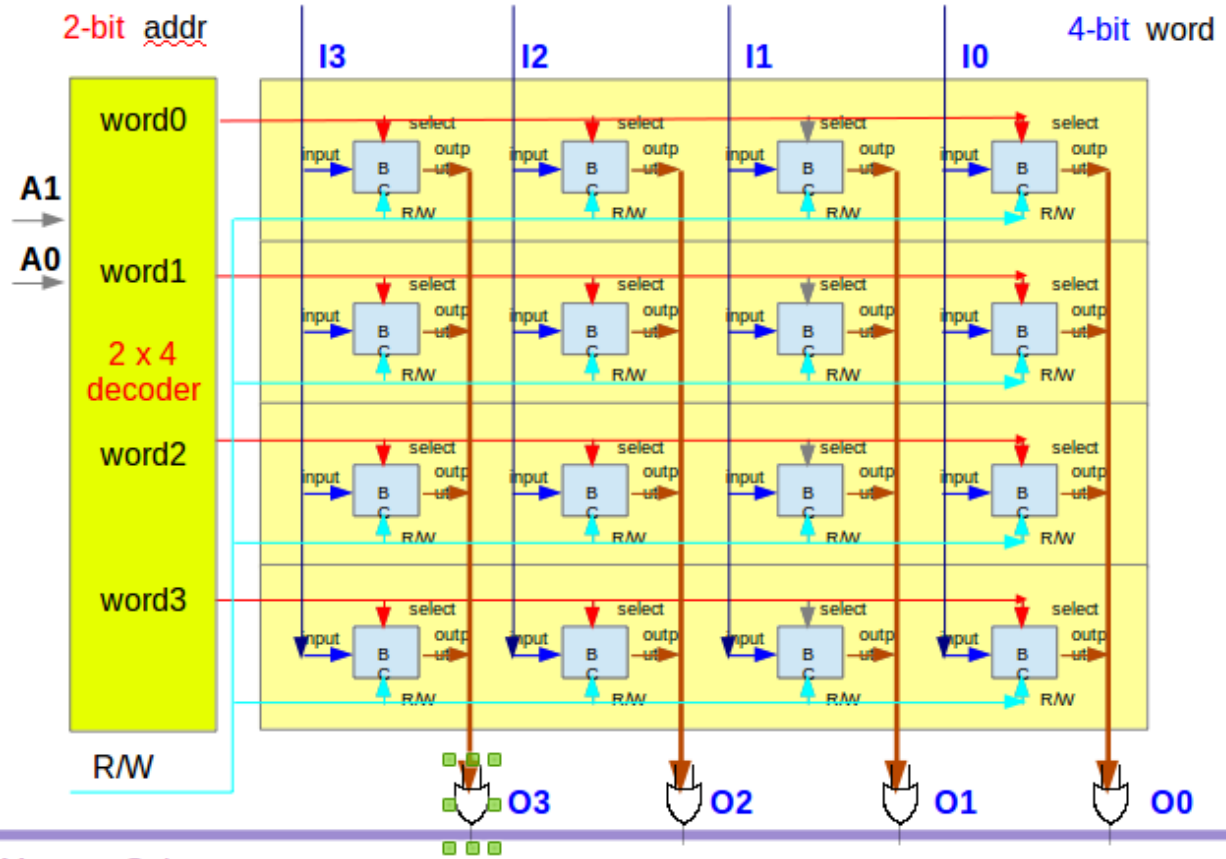
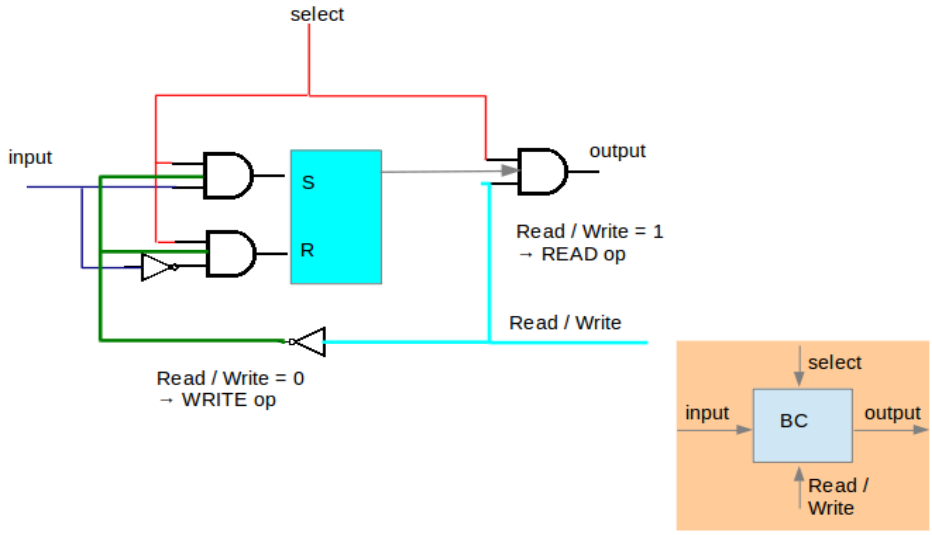
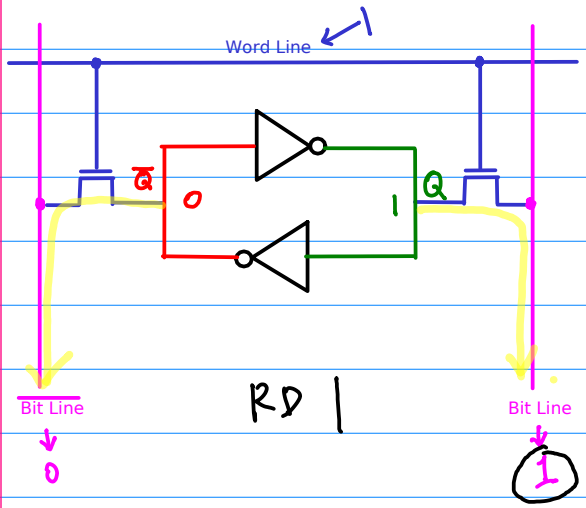


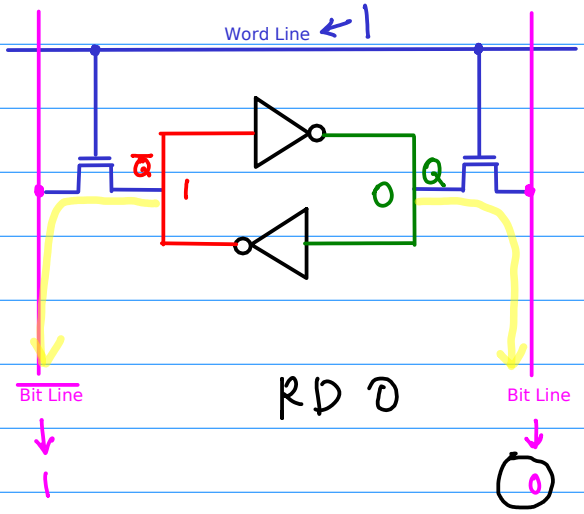
Diagram for a 4x4 Memory

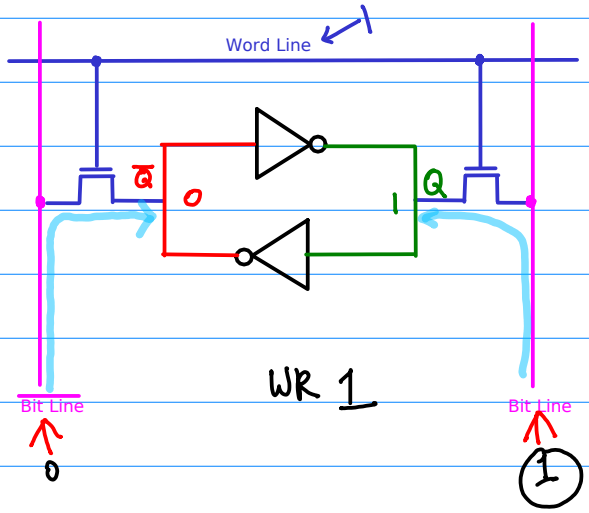


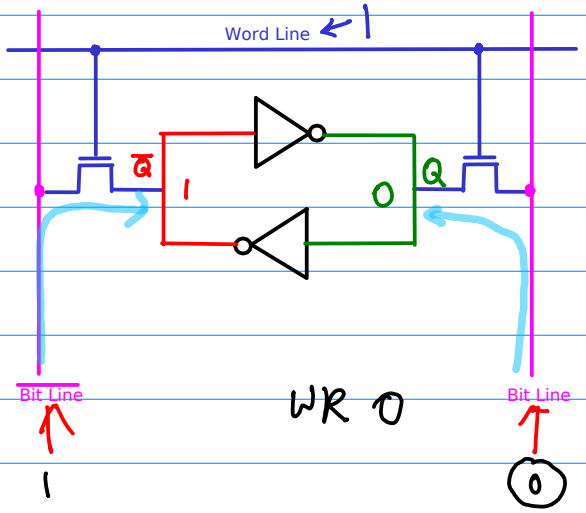
Selecting a Word



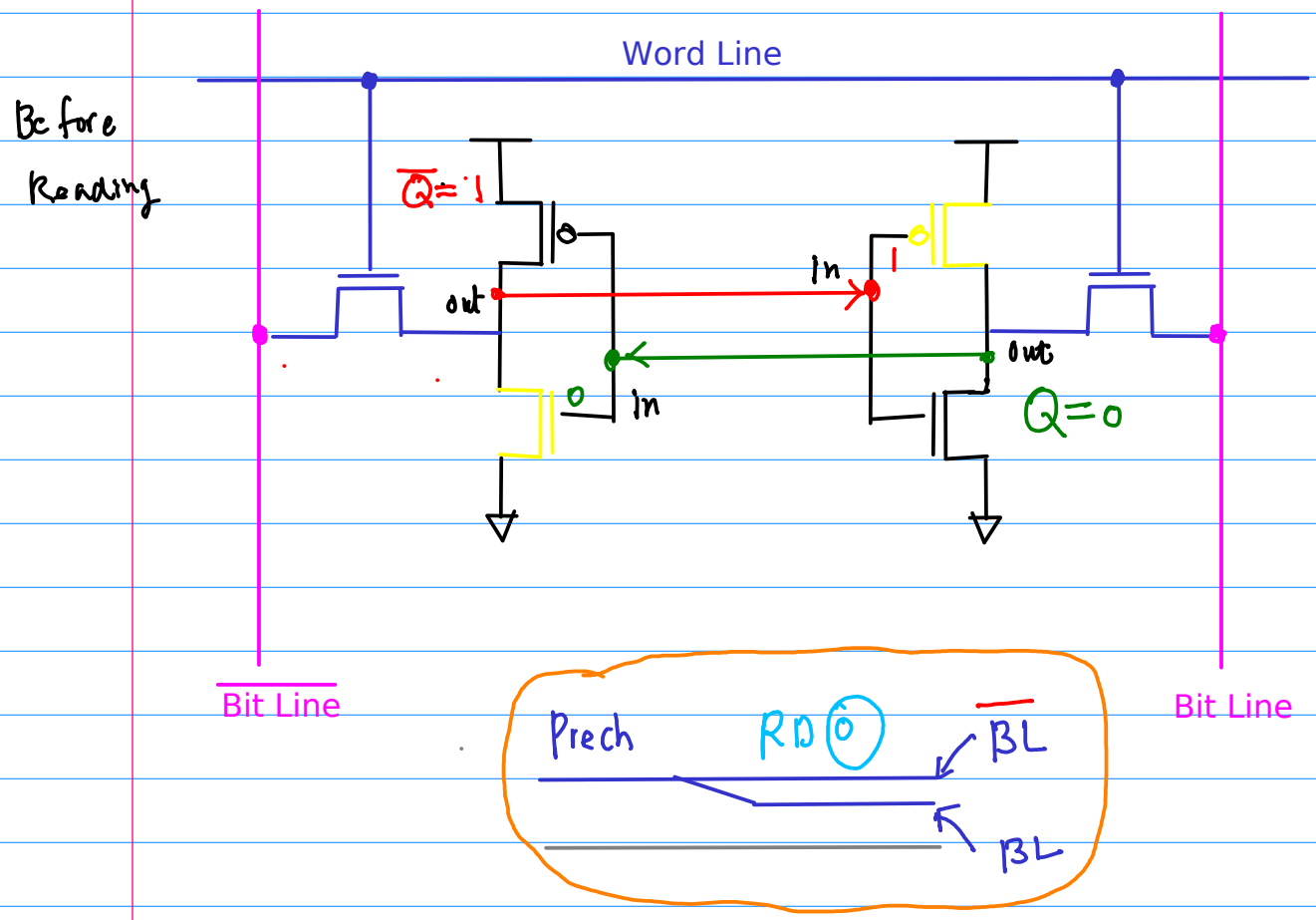




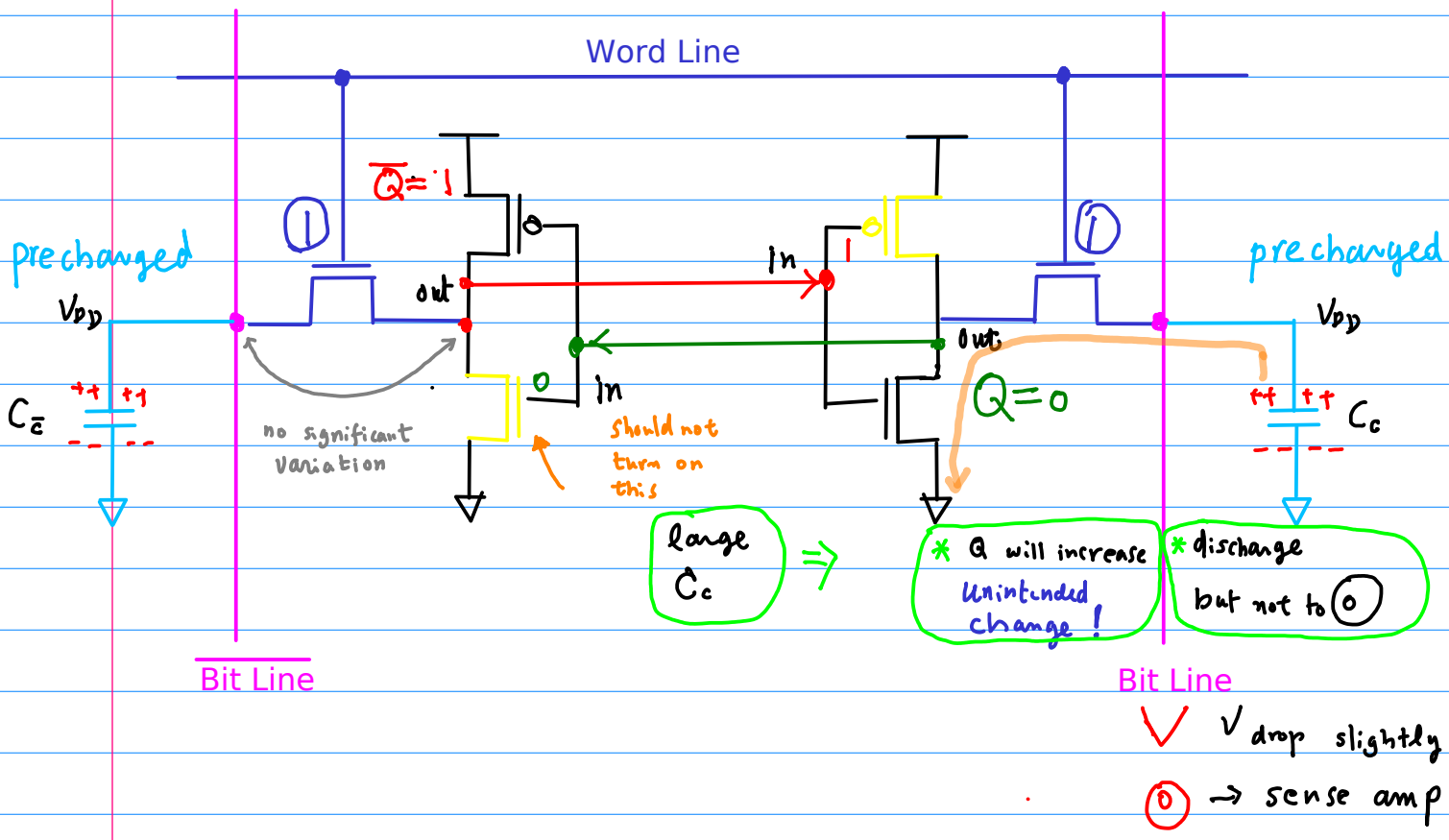




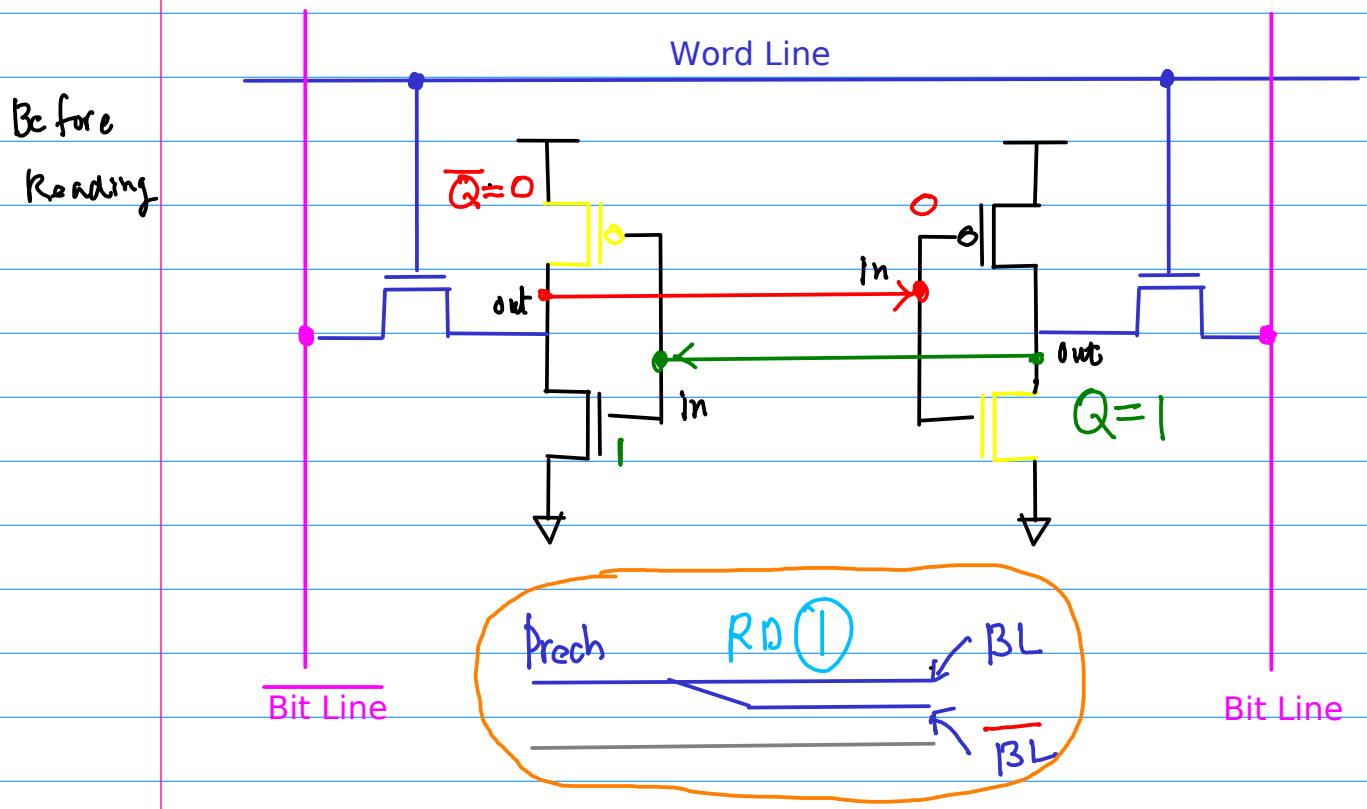
Read 0

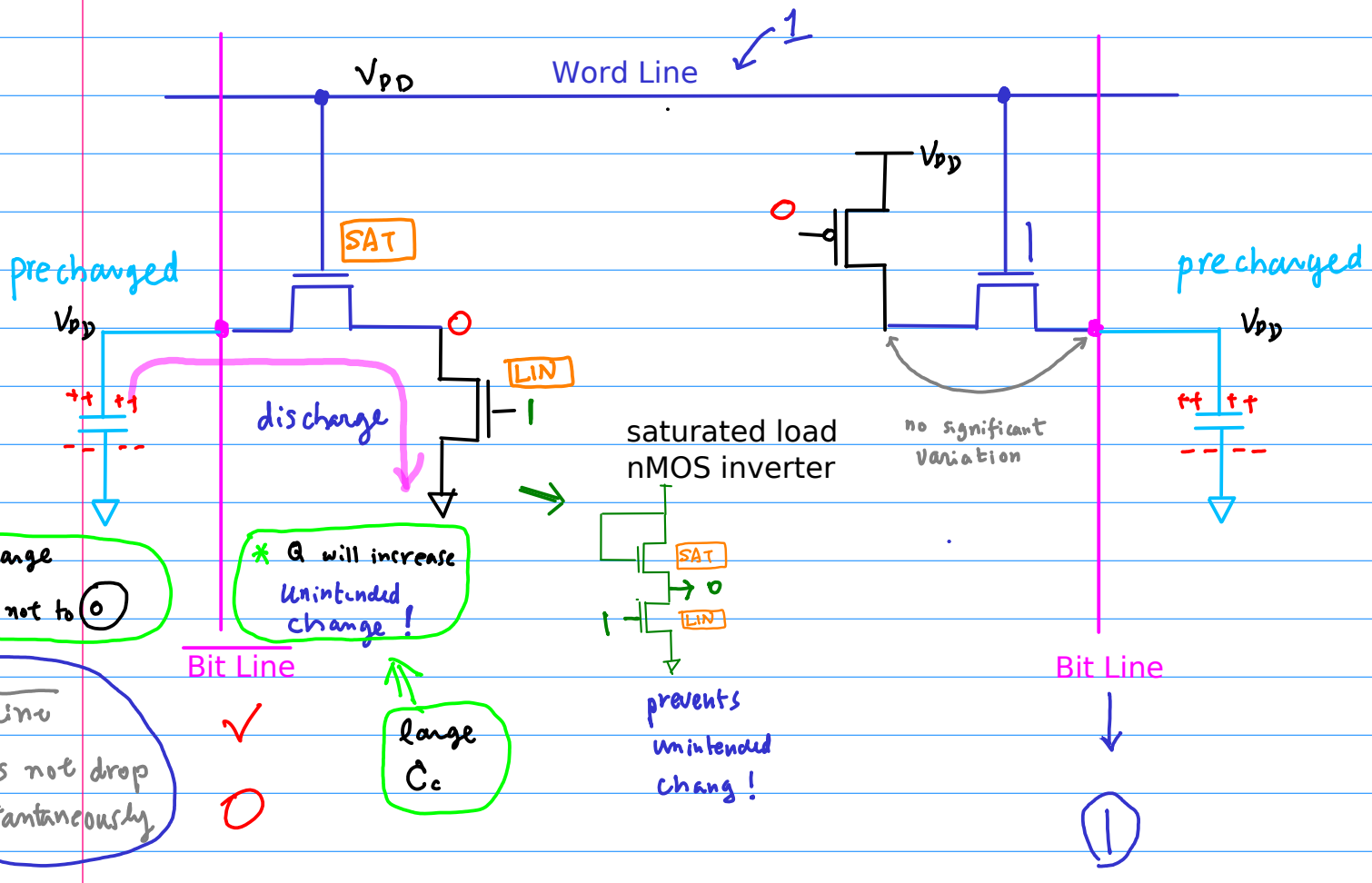

Before Reading
Word Line
Q=1
out
In
Out
Q=0
Bit Line
Bit Line

Prech
RD 0
BL
BL


Word Line
precharged
V_{DD}
C_c
Q=1
out
In
Out
Q=0
no significant variation
Should not turn on this
large C_c
* Q will increase
Unintended change!
* discharge
but not to 0
Bit Line
Bit Line
V drop slightly
0 → sense amp

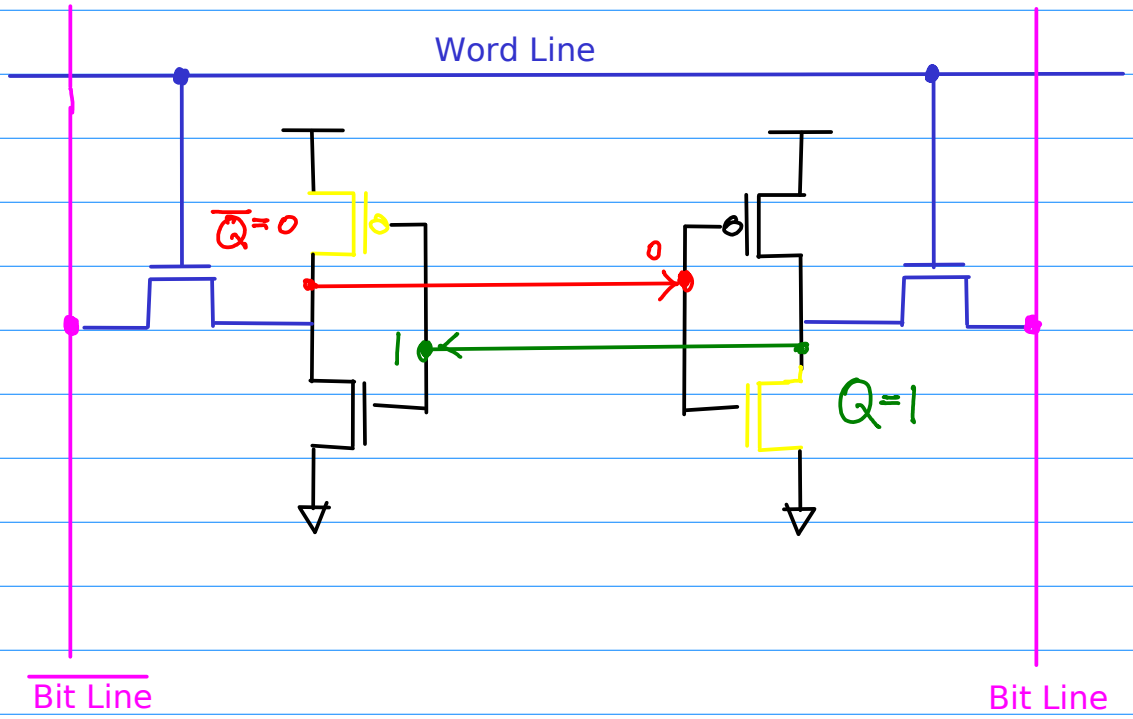
Read 1

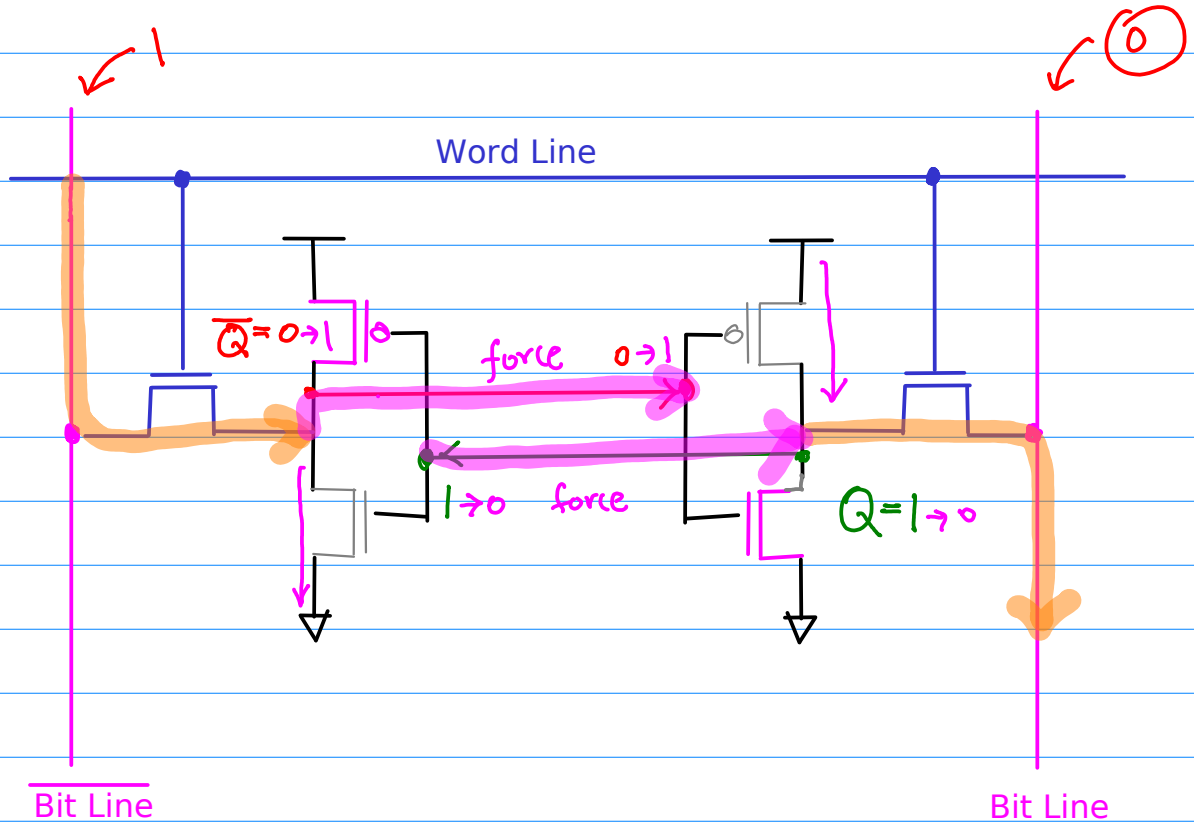

Before Reading
Word Line
Q=0
out
in
in
out
Q=1
1
Prech
RD 1
BL
BL
Bit Line
Bit Line


1
VDD
Word Line
SAT
precharged
VDD
LIN
1
discharge
* discharge but not to 0
* Q will increase
Unintended change !
Bit Line
Bit Line does not drop instantaneously
Large Cc
saturated load nMOS inverter
SAT
LIN
prevents unintended chang !
VDD
1
no significant variation
precharged
VDD
Bit Line
1

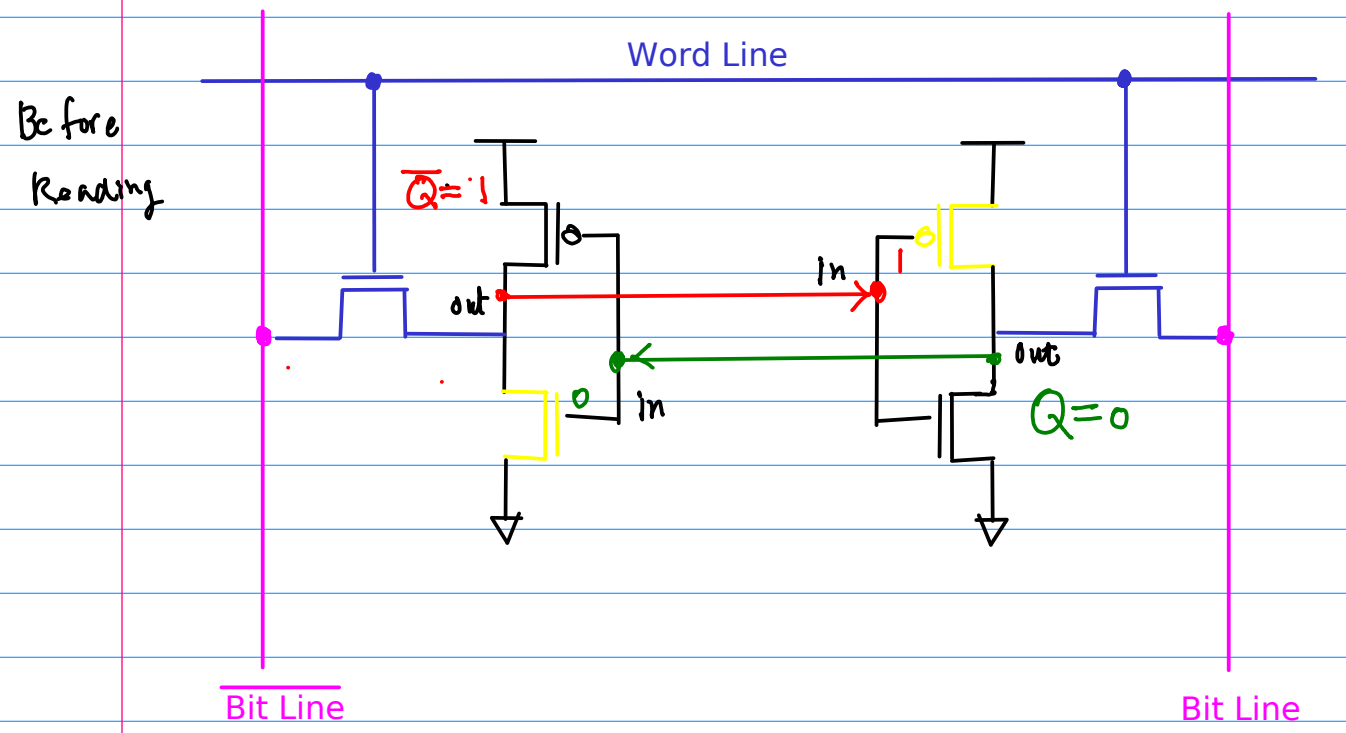
Write 0

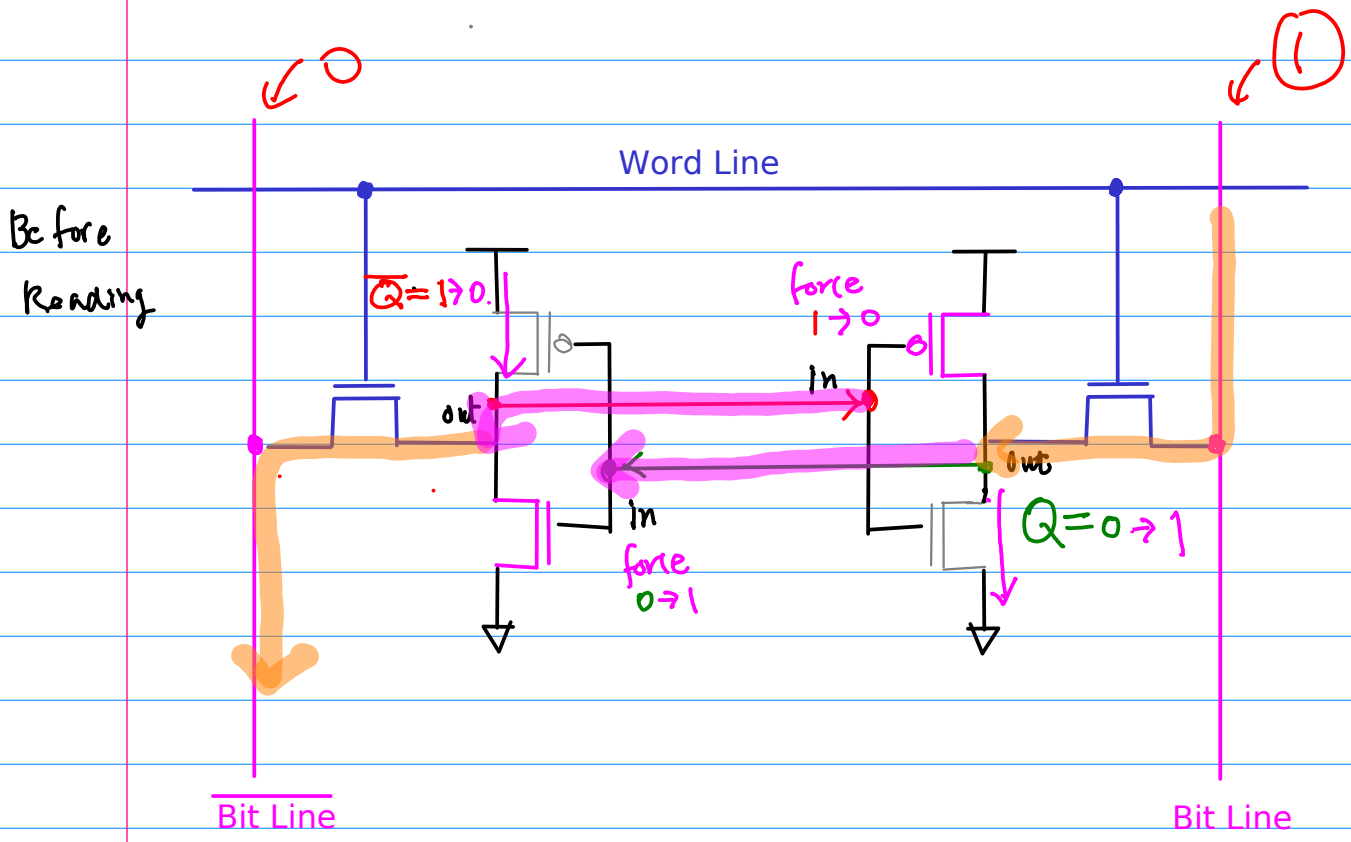
Before writing

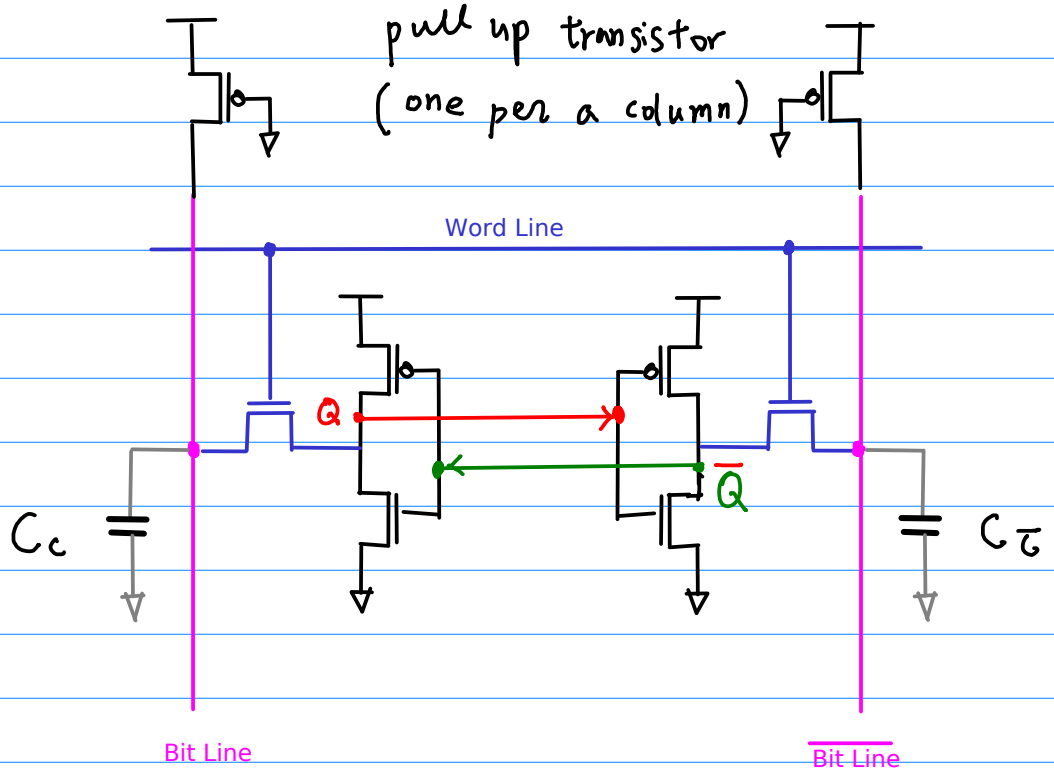




Write 1

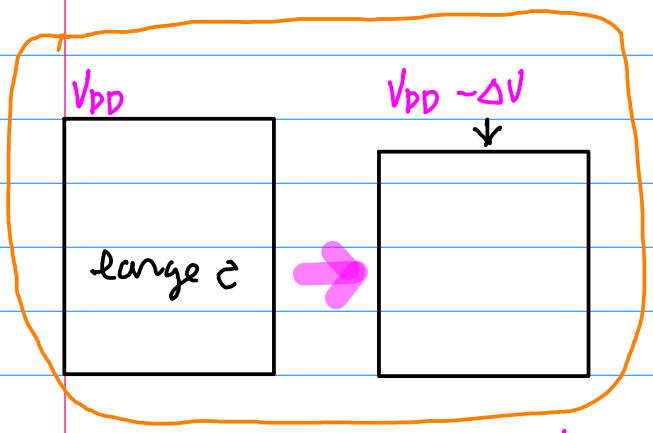

Word Line
Before Reading
Q=1
out
in
in
out
Q=0
Bit Line
Bit Line

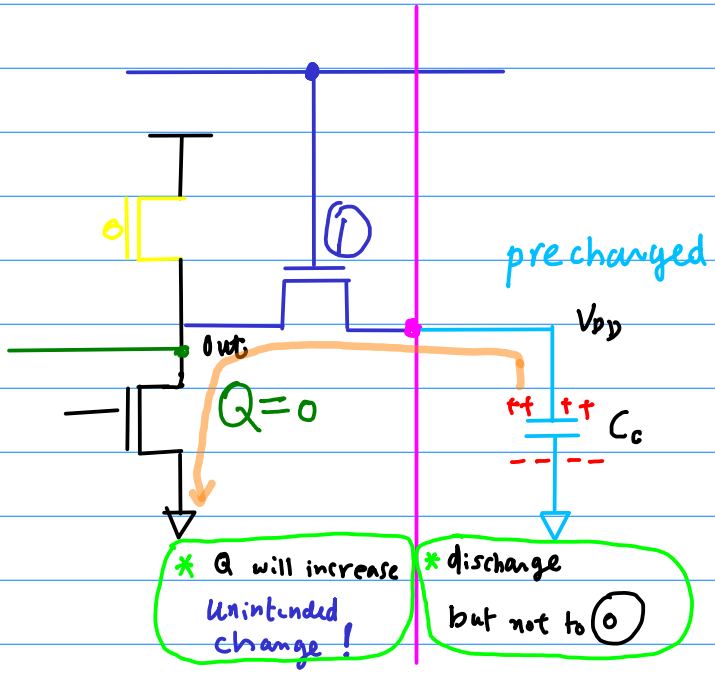

0
1
Word Line
Before Reading
Q=1→0
force 1→0
out
in
in
out
force 0→1
Q=0→1
Bit Line
Bit Line

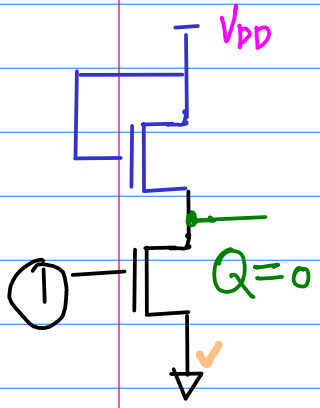

pull up transistor
(one per a column)
Word Line
Q
$\overline{Q}$
C_C
$C_{\overline{C}}$
Bit Line
$\overline{\text{Bit Line}}$

Bit Lines has large Capacitance

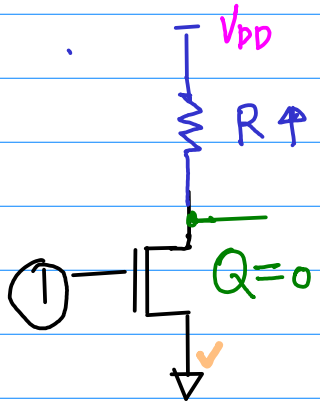
READ



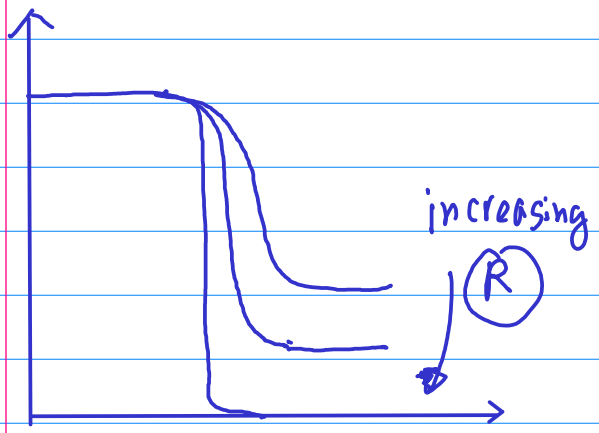




Saturated load inverter



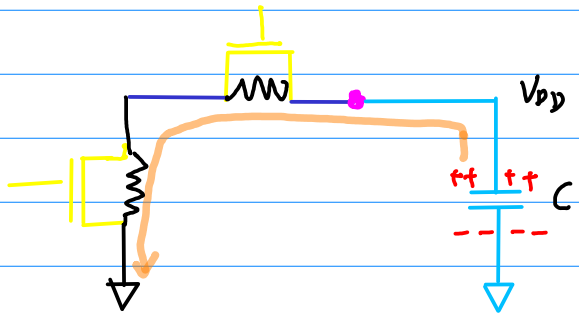
ratioed logic



to prevent malfunction

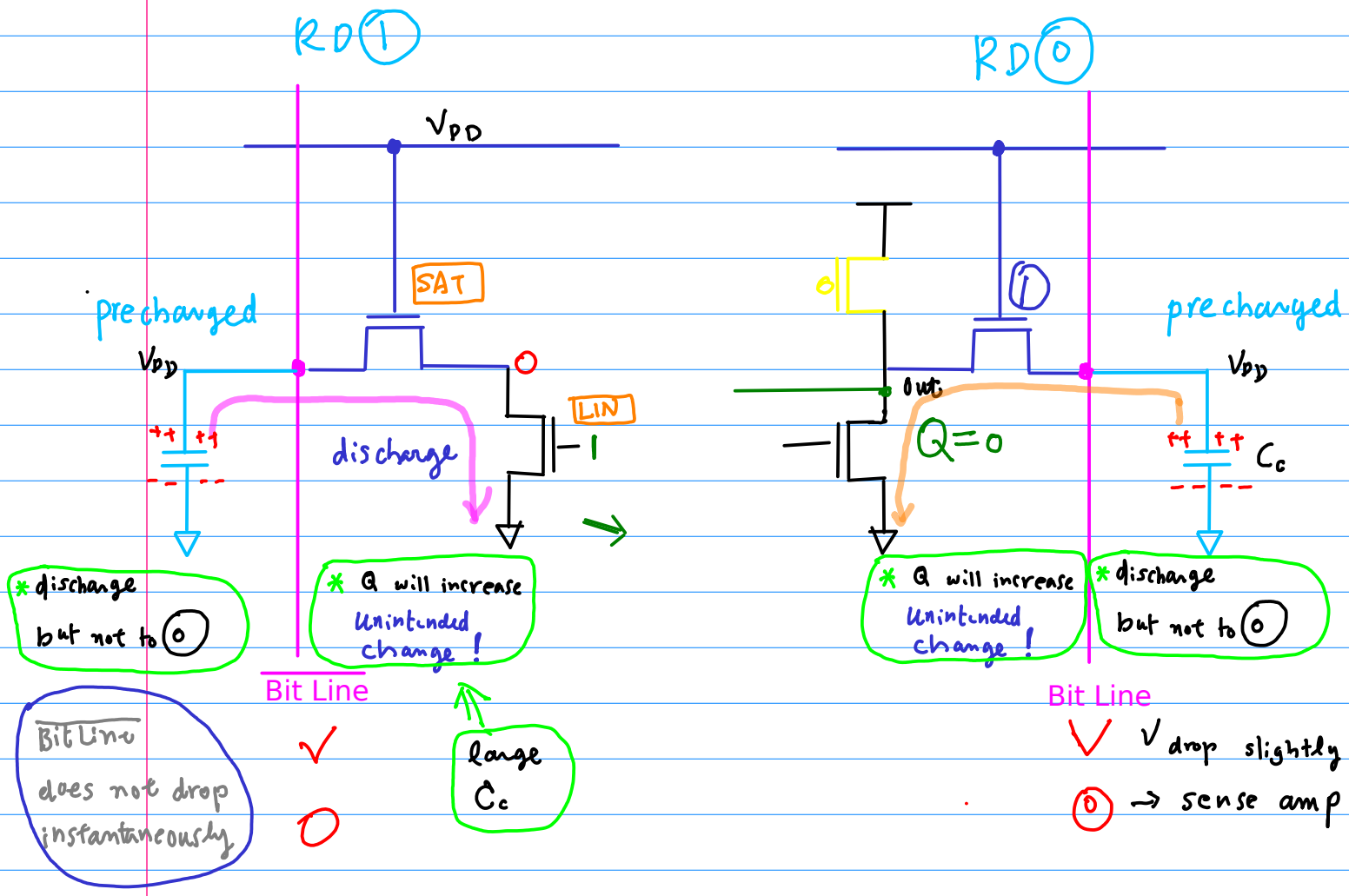
$R \uparrow \quad V_L \downarrow$

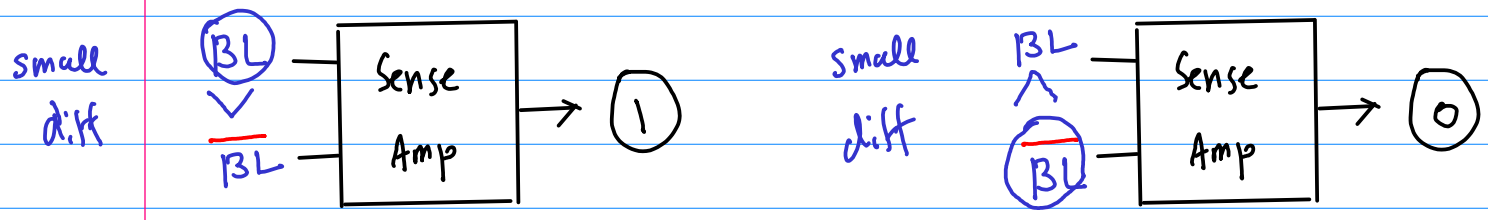
small size



discharging Bit Line takes long → small voltage drop.

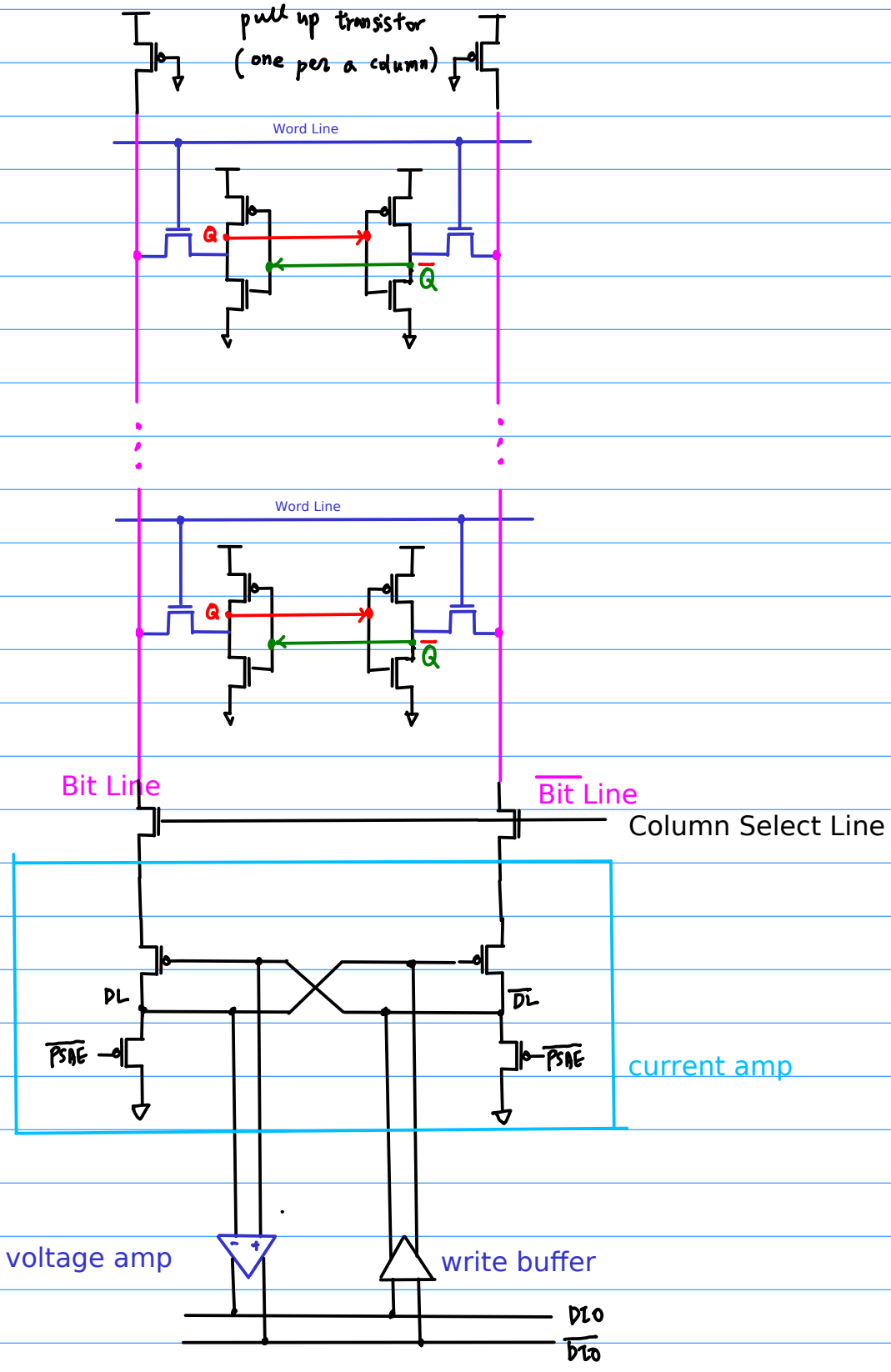
Sense Amp

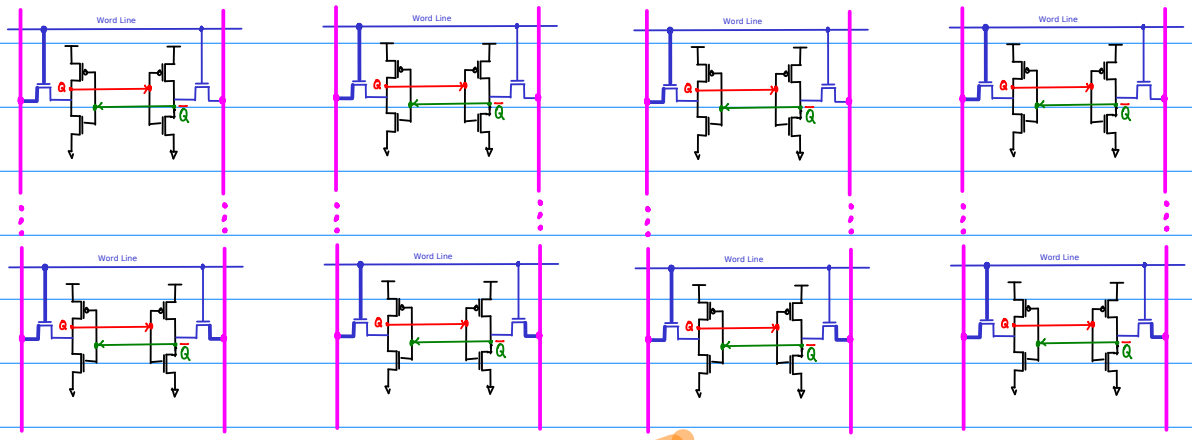




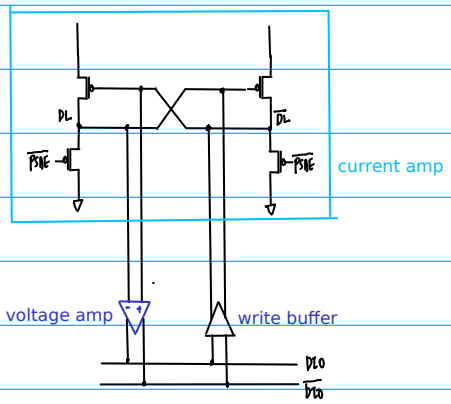
Multi stage Sense Amp = High Gain Curr Amp + Volt Amp

* differential Amp


pull up transistor
(one per a column)
Word Line
Q
$\overline{Q}$
Word Line
Q
$\overline{Q}$
Bit Line
$\overline{\text{Bit Line}}$
Column Select Line
DL
$\overline{DL}$
PSAE
$\overline{PSAE}$
current amp
voltage amp
write buffer
DIO
$\overline{DIO}$



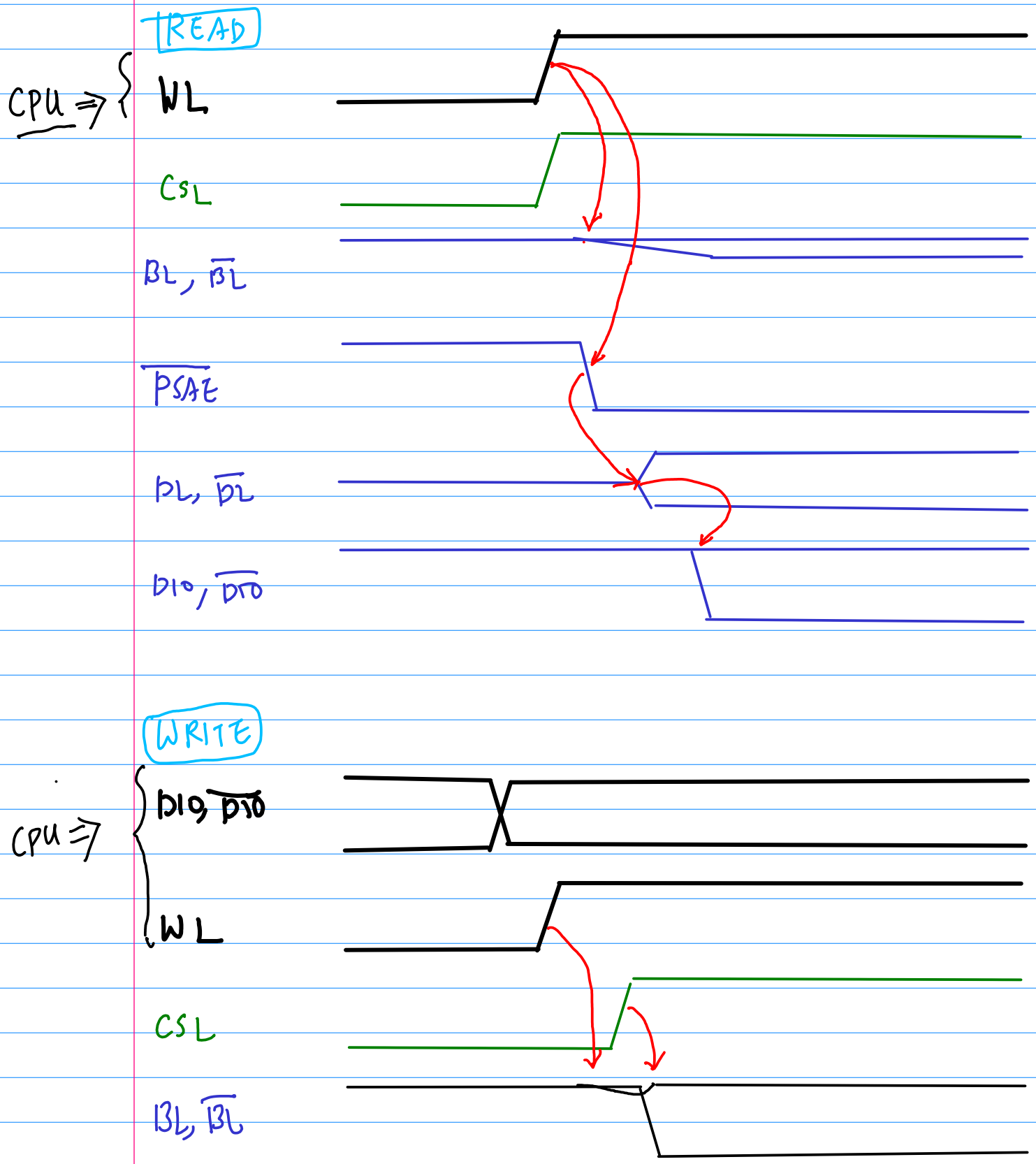
controlled by CSL (Column Selection Line)



Sense amp is shared by multiple bit lines (e.g. 32)

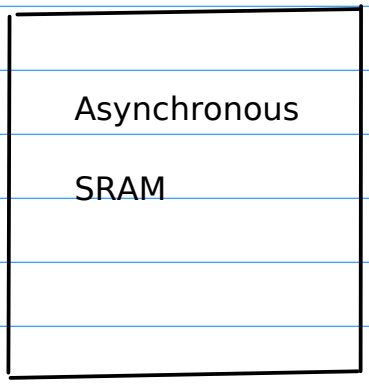
Asynchronous SRAM

triggered asynchronously



triggered asynchronously

Asynchronous SRAM



Synchronous SRAM