Transistor Level Design Example (3A)

Please send corrections (or suggestions) to youngwlim@hotmail.com.

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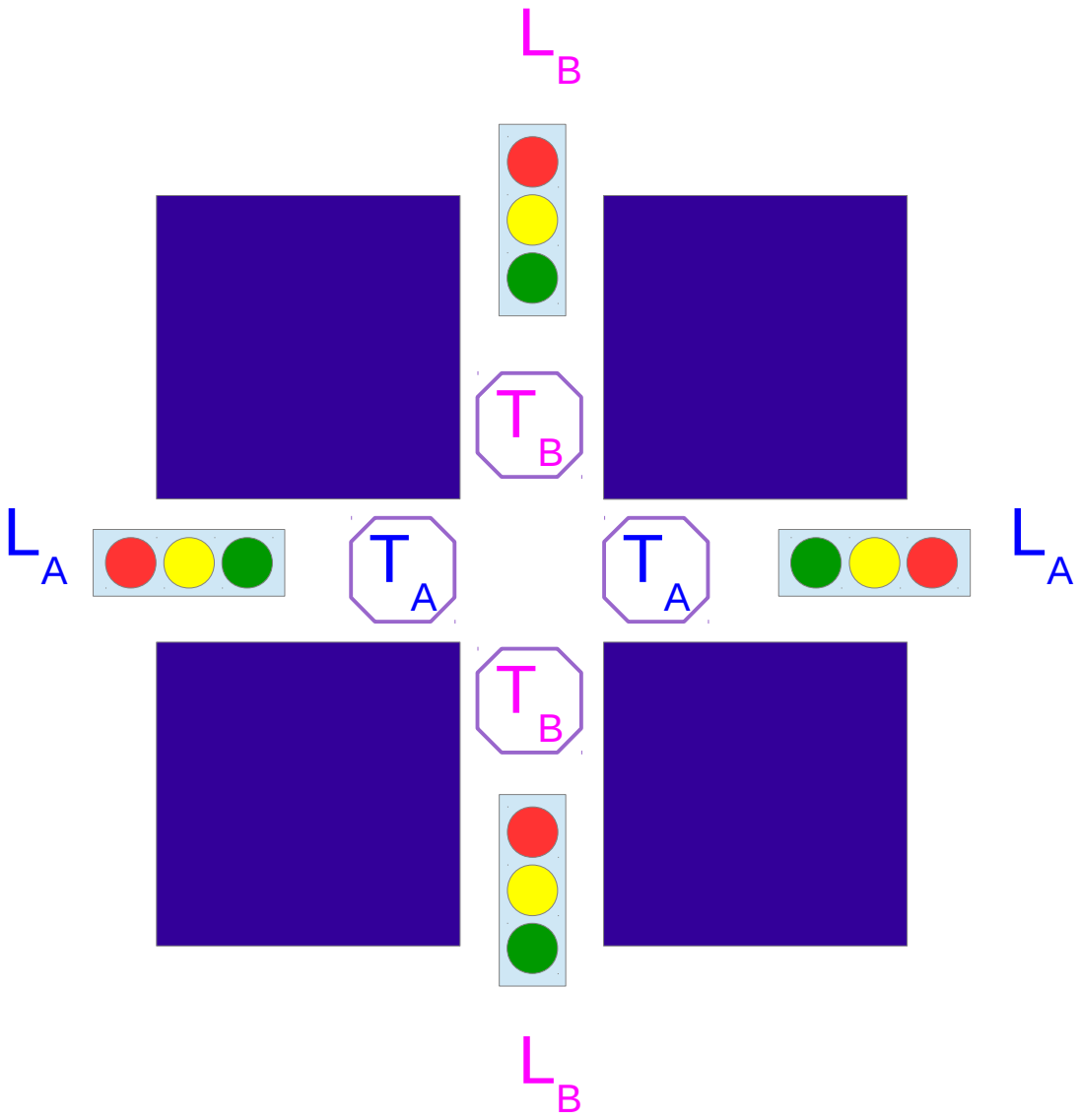
FSM Inputs and Outputs



Traffic Lights - Outputs

L_A L_B

Sensor - Inputs

T_A T_B

Moore FSM State Transition Table

S_1	S_0	T_A	T_B	S'_1	S'_0
0	0	0	X	0	1
0	0	1	X	0	0
0	1	X	X	1	0
1	0	X	0	1	1
1	0	X	1	1	0
1	1	X	X	0	0

	S_1	S_0	T_A	T_B	S'_1
	0	0	0	X	0
	0	0	1	X	0
$\overline{S_1}S_0$	0	1	X	X	1
$S_1\overline{S_0}\overline{T_B}$	1	0	X	0	1
$S_1\overline{S_0}T_B$	1	0	X	1	1
	1	1	X	X	0

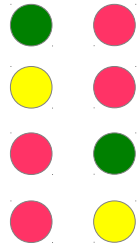
$$S'_1 = \overline{S_1}S_0 + S_1\overline{S_0}$$
$$= S_1 \oplus S_0$$

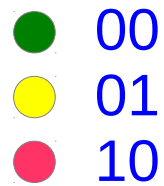
	S_1	S_0	T_A	T_B	S'_0
$\overline{S_1}\overline{S_0}\overline{T_A}$	0	0	0	X	1
	0	0	1	X	0
	0	1	X	X	0
$S_1\overline{S_0}\overline{T_B}$	1	0	X	0	1
	1	0	X	1	0
	1	1	X	X	0

$$S'_0 = \overline{S_1}\overline{S_0}\overline{T_A} + S_1\overline{S_0}\overline{T_B}$$

States and Outputs

S_1	S_0	L_{A1}	L_{A0}	L_{B1}	L_{B0}
0	0	0	0	1	0
0	1	0	1	1	0
1	0	1	0	0	0
1	1	1	0	0	1





S_1	S_0	L_{A1}
0	0	0
0	1	0
1	0	1
1	1	1

$$L_{A1} = S_1$$

S_1	S_0	L_{A0}
0	0	0
0	1	1
1	0	0
1	1	0

$$L_{A0} = \overline{S_1} S_0$$

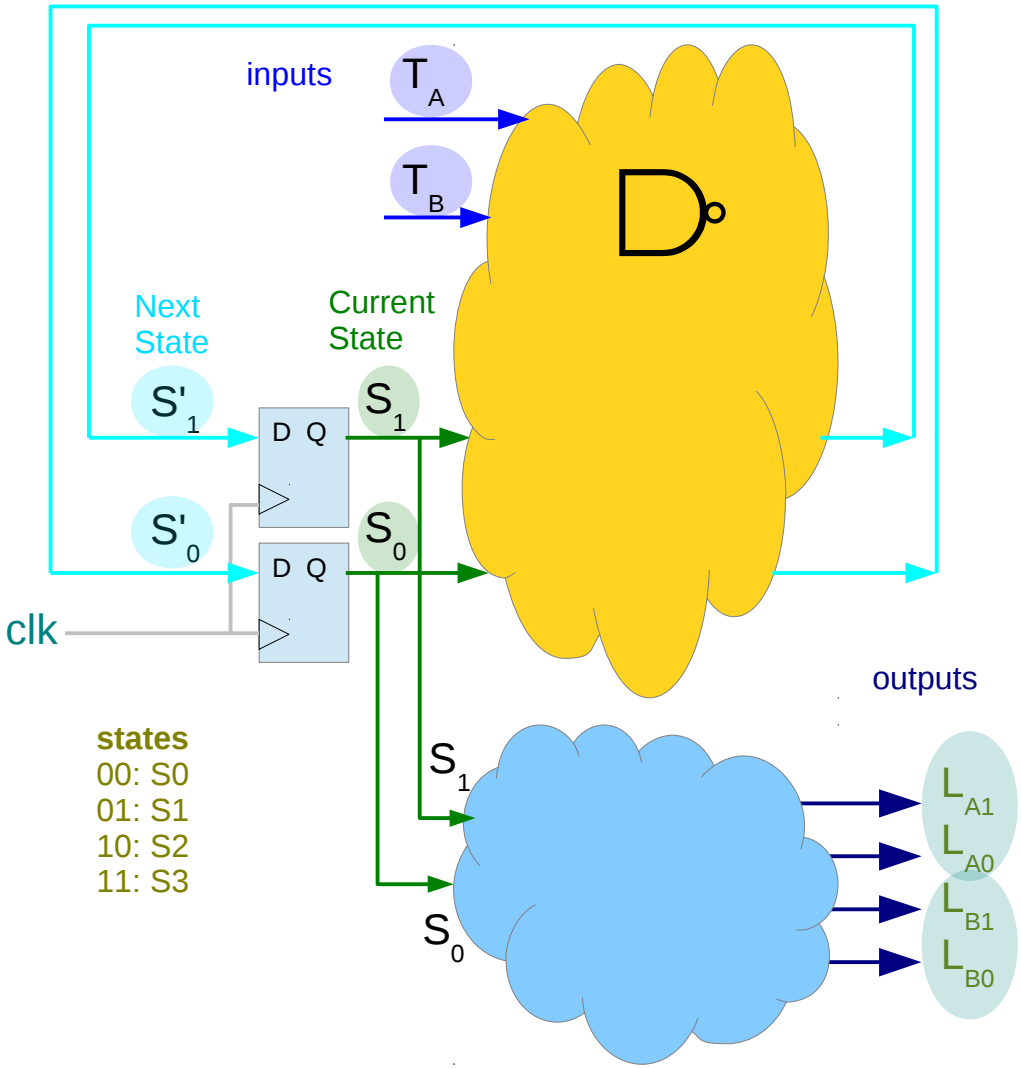
S_1	S_0	L_{B1}
0	0	1
0	1	1
1	0	0
1	1	0

$$L_{B1} = \overline{S_1}$$

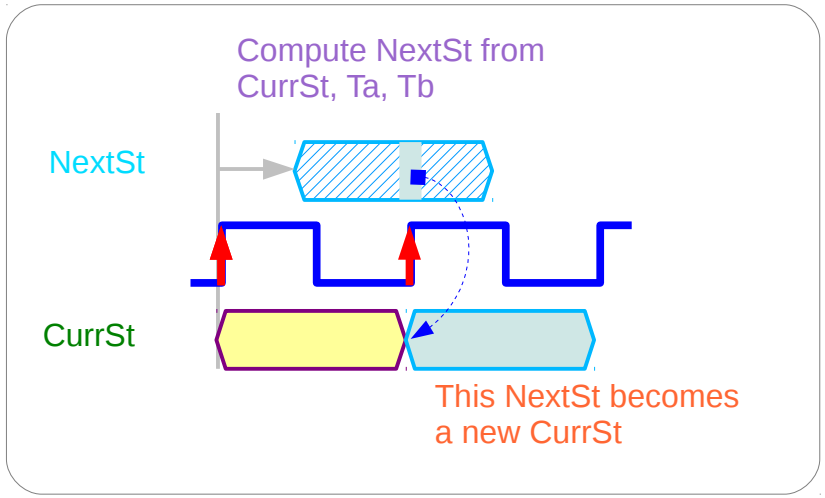
S_1	S_0	L_{B0}
0	0	0
0	1	0
1	0	0
1	1	1

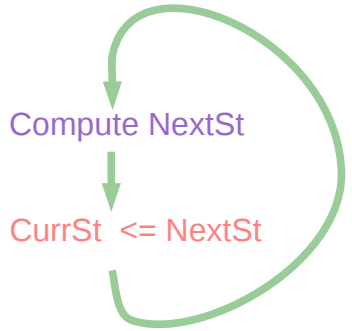
$$L_{B0} = S_1 S_0$$

Moore FSM (1)



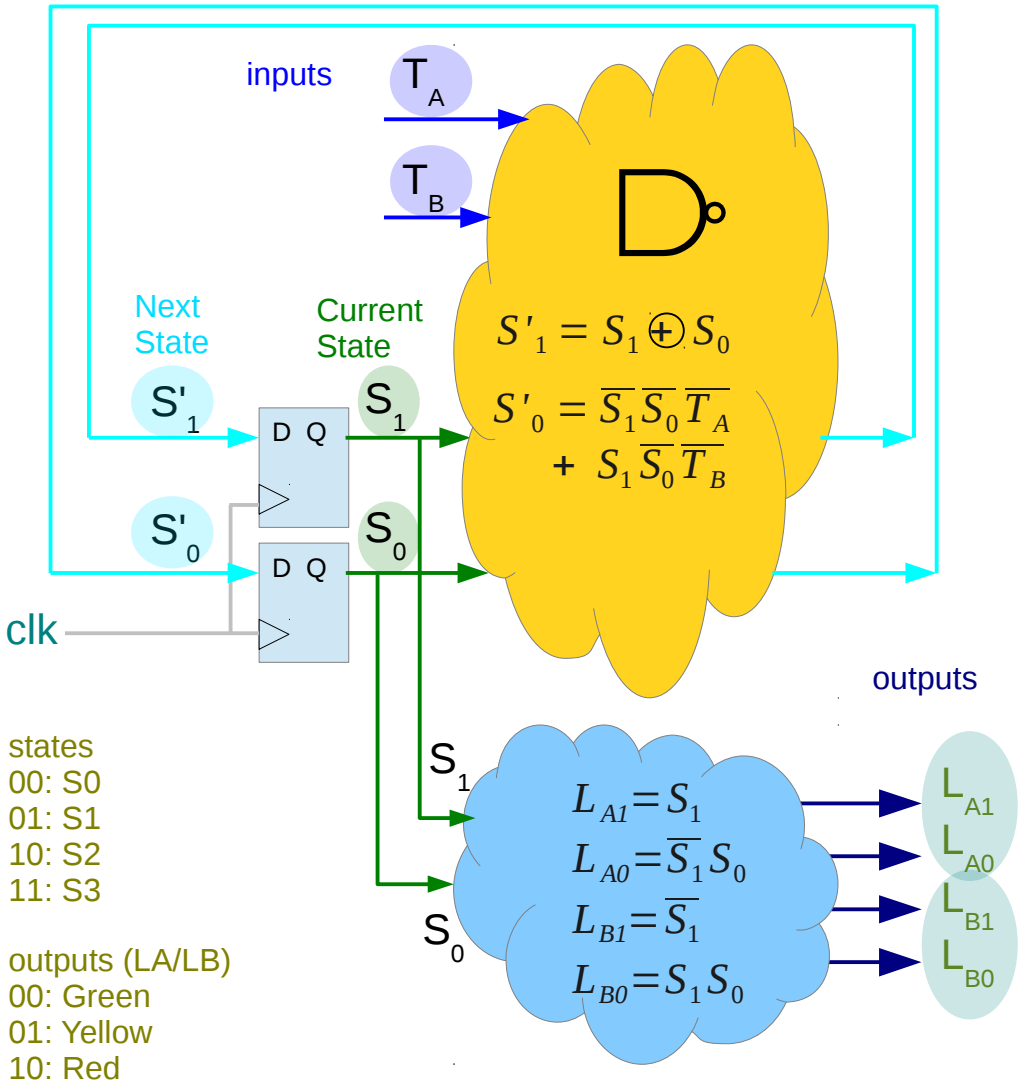
states
00: S0
01: S1
10: S2
11: S3





outputs (LA/LB)
00: Green
01: Yellow
10: Red
11: X

Moore FSM



Inputs T_A T_B

Current State S_1 S_0

Next States

$S'_1 = S_1 \oplus S_0$

$S'_0 = \overline{S_1}\,\overline{S_0}\,\overline{T_A} + S_1\,\overline{S_0}\,\overline{T_B}$

Current State S_1 S_0

Outputs

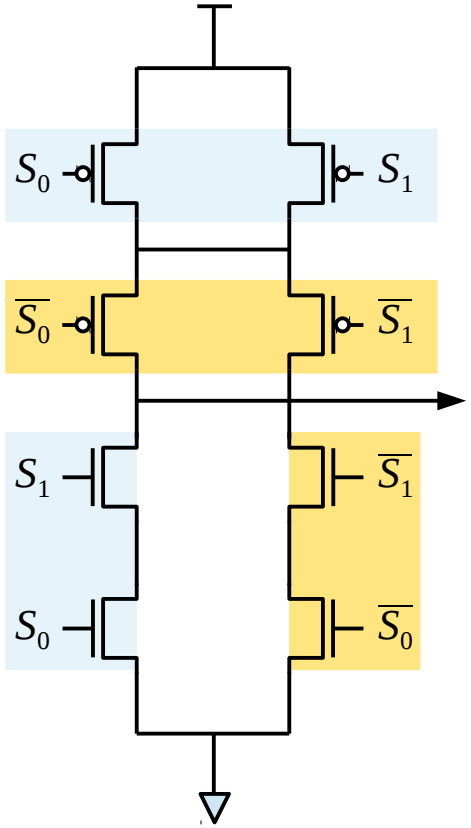
$L_{A1} = S_1$ $L_{B1} = \overline{S_1}$

$L_{A0} = \overline{S_1}\,S_0$ $L_{B0} = S_1 S_0$

Function S'1

$$S'_1 = \overline{S_1} S_0 + S_1 \overline{S_0}$$
$$= S_1 \oplus S_0$$

$$\overline{S'_1} = \overline{S_1}\,\overline{S_0} + S_1 S_0$$



$$S'_1 = \overline{S_1} S_0 + S_1 \overline{S_0}$$

$$(S_0 + S_1) \cdot (\overline{S_0} + \overline{S_1})$$
$$= ((S_0 + S_1) \cdot \overline{S_0}) + ((S_0 + S_1) \cdot \overline{S_1})$$
$$= \overline{S_0} S_1 + S_0 \overline{S_1}$$
$$= S_1 \oplus S_0$$

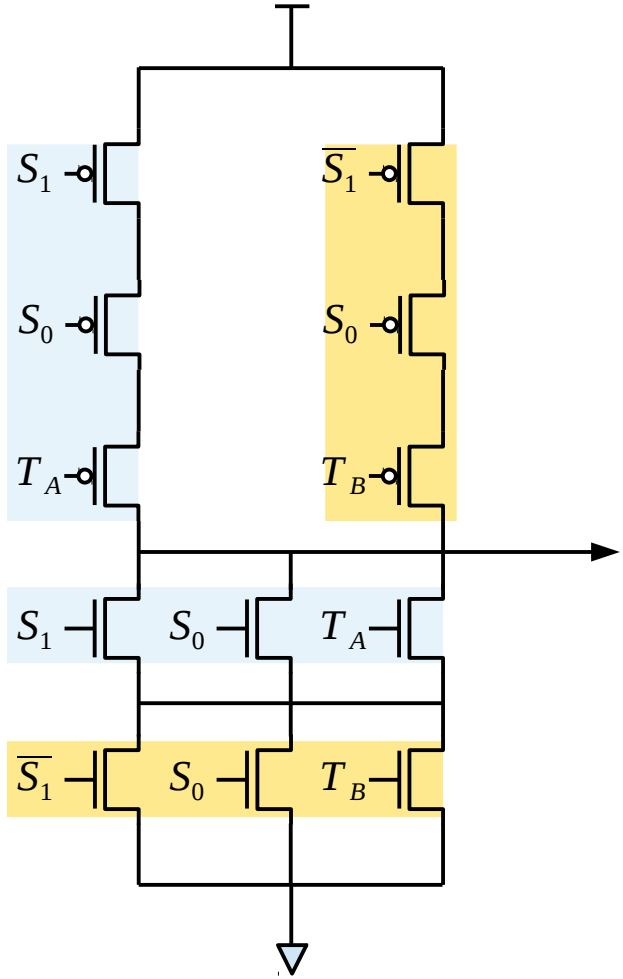
$$\overline{S_1}\,\overline{S_0} + S_1 S_0$$
$$= \overline{S_1 \oplus S_0}$$

Function S'2

$$S'_0 = \overline{S_1}\,\overline{S_0}\,\overline{T_A} + S_1\,\overline{S_0}\,\overline{T_B}$$

$$\overline{S'_0} = \overline{\overline{S_1}\,\overline{S_0}\,\overline{T_A}} \cdot \overline{S_1\,\overline{S_0}\,\overline{T_B}}$$

$$= (S_1 + S_0 + T_A) \cdot (\overline{S_1} + S_0 + T_B)$$



$$S'_0 = \overline{S_1}\,\overline{S_0}\,\overline{T_A} + S_1\,\overline{S_0}\,\overline{T_B}$$

Outputs L_{A0} & L_{B0}

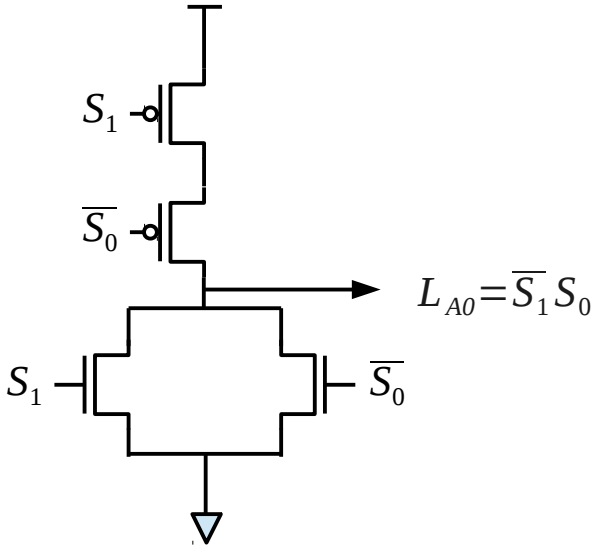
$$L_{A0} = \overline{S_1} S_0$$

$$\overline{L_{A0}} = \overline{\overline{S_1} S_0} = S_1 + \overline{S_0}$$

nMOS PDN

$$L_{A0} = (\overline{S_1})(\overline{S_0})$$

pMOS PUN



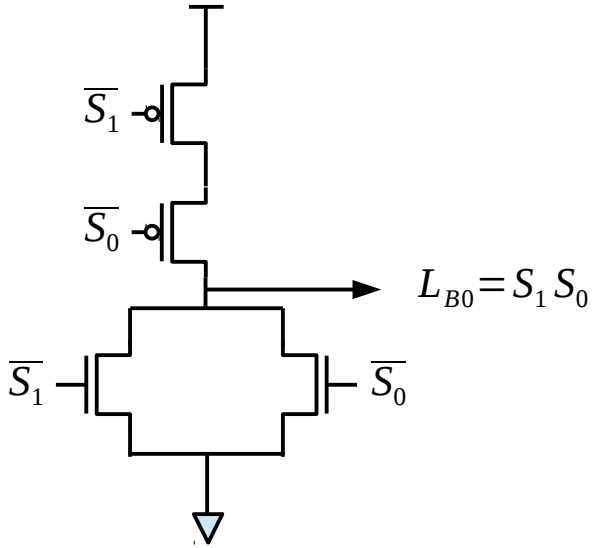
$$L_{B0} = S_1 S_0$$

$$\overline{L_{A0}} = \overline{S_1 S_0} = \overline{S_1} + \overline{S_0}$$

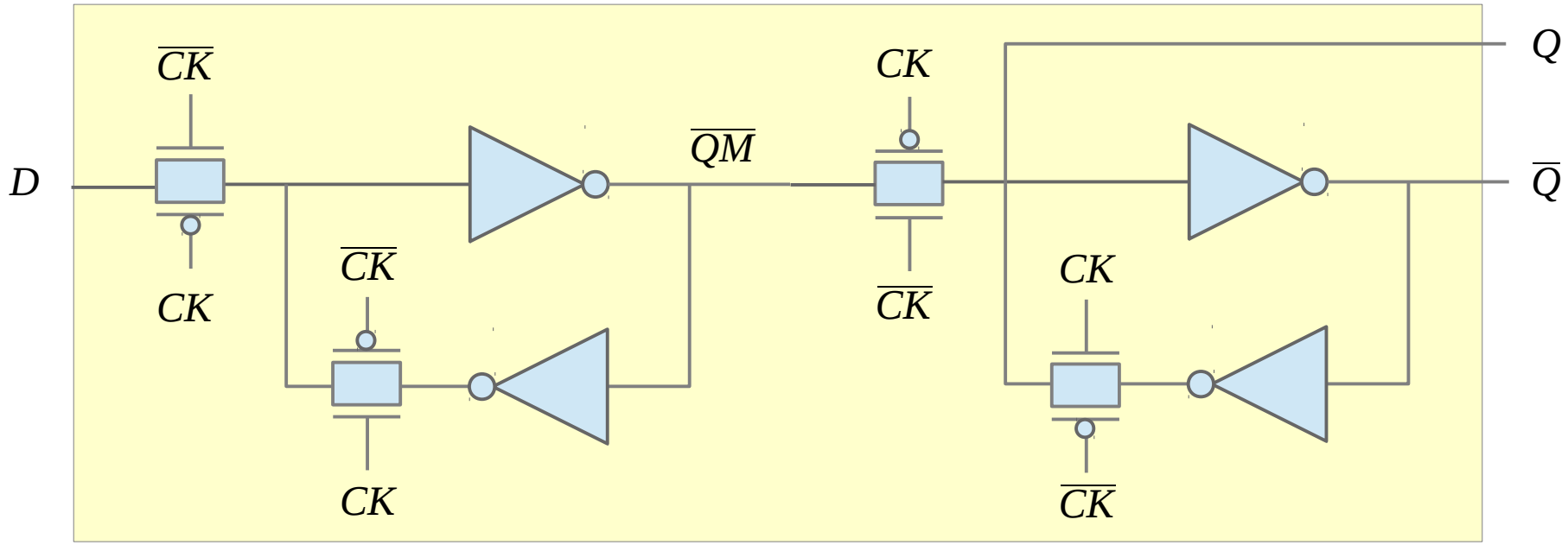
nMOS PDN

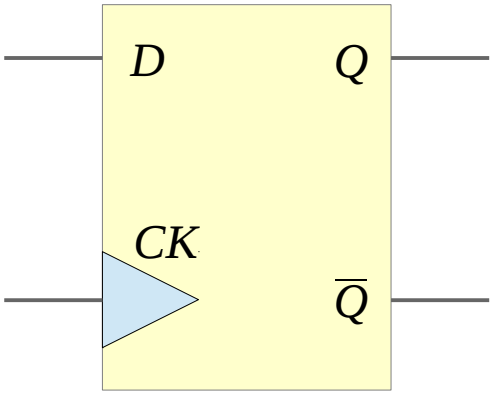
$$L_{B0} = (\overline{S_1})(\overline{S_0})$$

pMOS PUN



D Flip Flop with Pass Gate





References

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[10] https://en.wikiversity.org/wiki/The_necessities_in_Computer_Organization