

# Transistor Level Design Example (3A)

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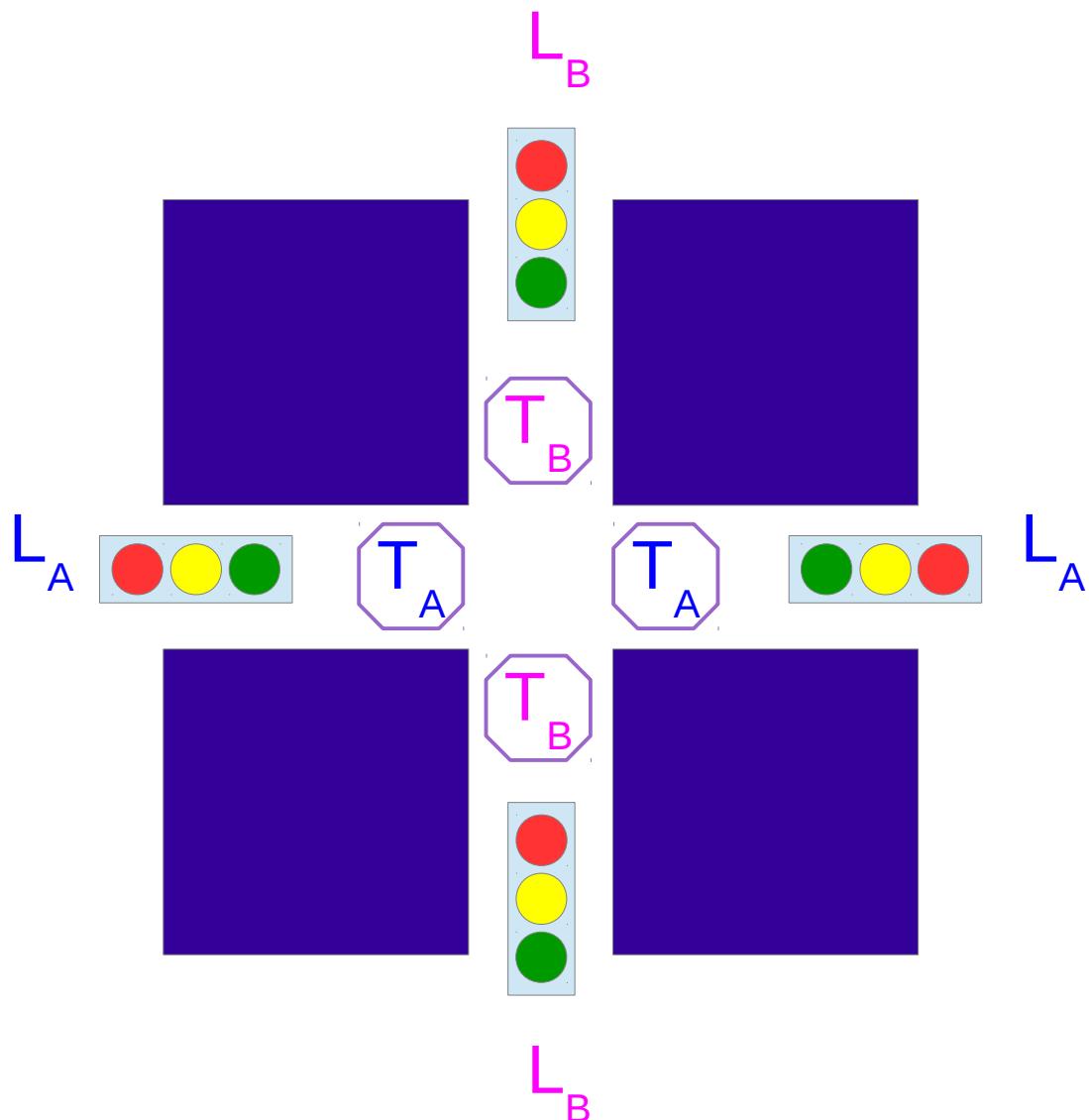
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# FSM Inputs and Outputs



Traffic Lights - Outputs

L<sub>A</sub> L<sub>B</sub>

Sensor - Inputs

T<sub>A</sub> T<sub>B</sub>

# Moore FSM State Transition Table

$S_1$	$S_0$	$T_A$	$T_B$	$S'_1$	$S'_0$
0	0	0	X	0	1
0	0	1	X	0	0
0	1	X	X	1	0
1	0	X	0	1	1
1	0	X	1	1	0
1	1	X	X	0	0

$S_1$	$S_0$	$T_A$	$T_B$	$S'_1$
0	0	0	X	0
0	0	1	X	0
0	1	X	X	1
1	0	X	0	1
1	0	X	1	1
1	1	X	X	0

$\overline{S}_1 S_0$

$S_1 \overline{S}_0 T_B$

$S_1 \overline{S}_0 T_B$

$S_1$	$S_0$	$T_A$	$T_B$	$S'_0$
0	0	0	X	1
0	0	1	X	0
0	1	X	X	0
1	0	X	0	1
1	0	X	1	0
1	1	X	X	0

$S_1 \overline{S}_0 \overline{T}_A$

$S_1 \overline{S}_0 \overline{T}_B$

$$\begin{aligned} S'_1 &= \overline{S}_1 S_0 + S_1 \overline{S}_0 \\ &= S_1 \oplus S_0 \end{aligned}$$

$$S'_0 = \overline{S}_1 \overline{S}_0 \overline{T}_A + S_1 \overline{S}_0 \overline{T}_B$$

# States and Outputs

$S_1$	$S_0$	$L_{A1}$	$L_{A0}$	$L_{B1}$	$L_{B0}$
0 0	0 0	1 0			
0 1	0 1	1 0			
1 0	1 0	0 0			
1 1	1 0	0 1			

- 00
- 01
- 10

$S_1$	$S_0$	$L_{A1}$
0 0	0	
0 1	0	
	1 0	1
	1 1	1

$$L_{A1} = S_1$$

$S_1$	$S_0$	$L_{A0}$
0 0	0	
	0 1	1
	1 0	0
	1 1	0

$$L_{A0} = \overline{S}_1 S_0$$

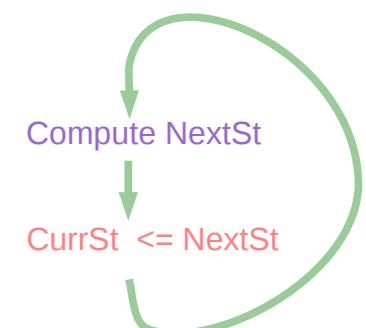
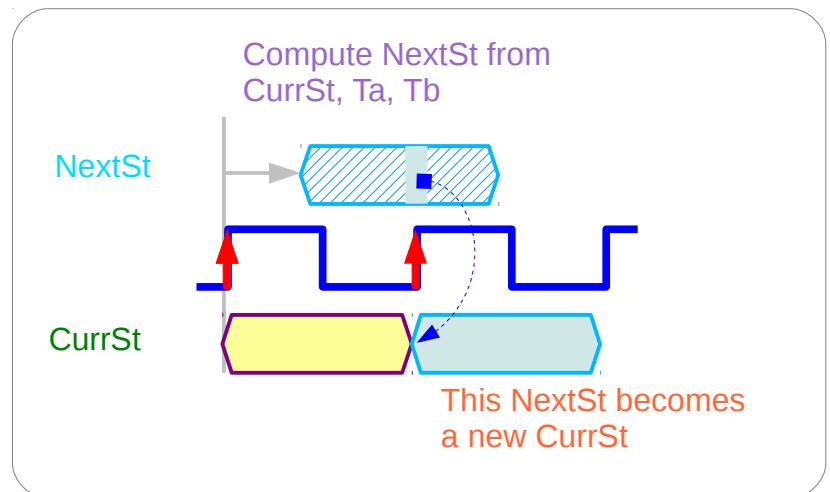
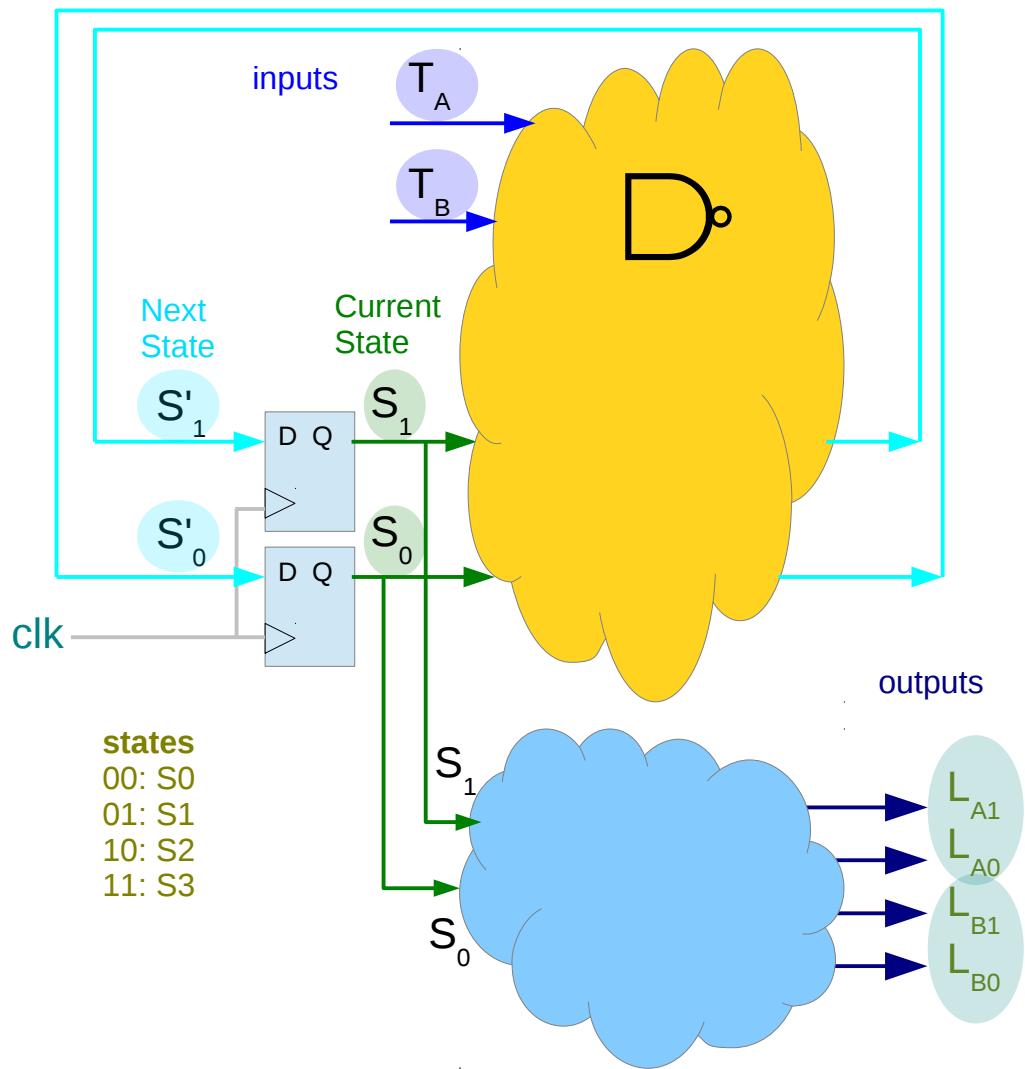
$S_1$	$S_0$	$L_{B1}$
	0 0	1
	0 1	1
	1 0	0
	1 1	0

$$L_{B1} = \overline{S}_1$$

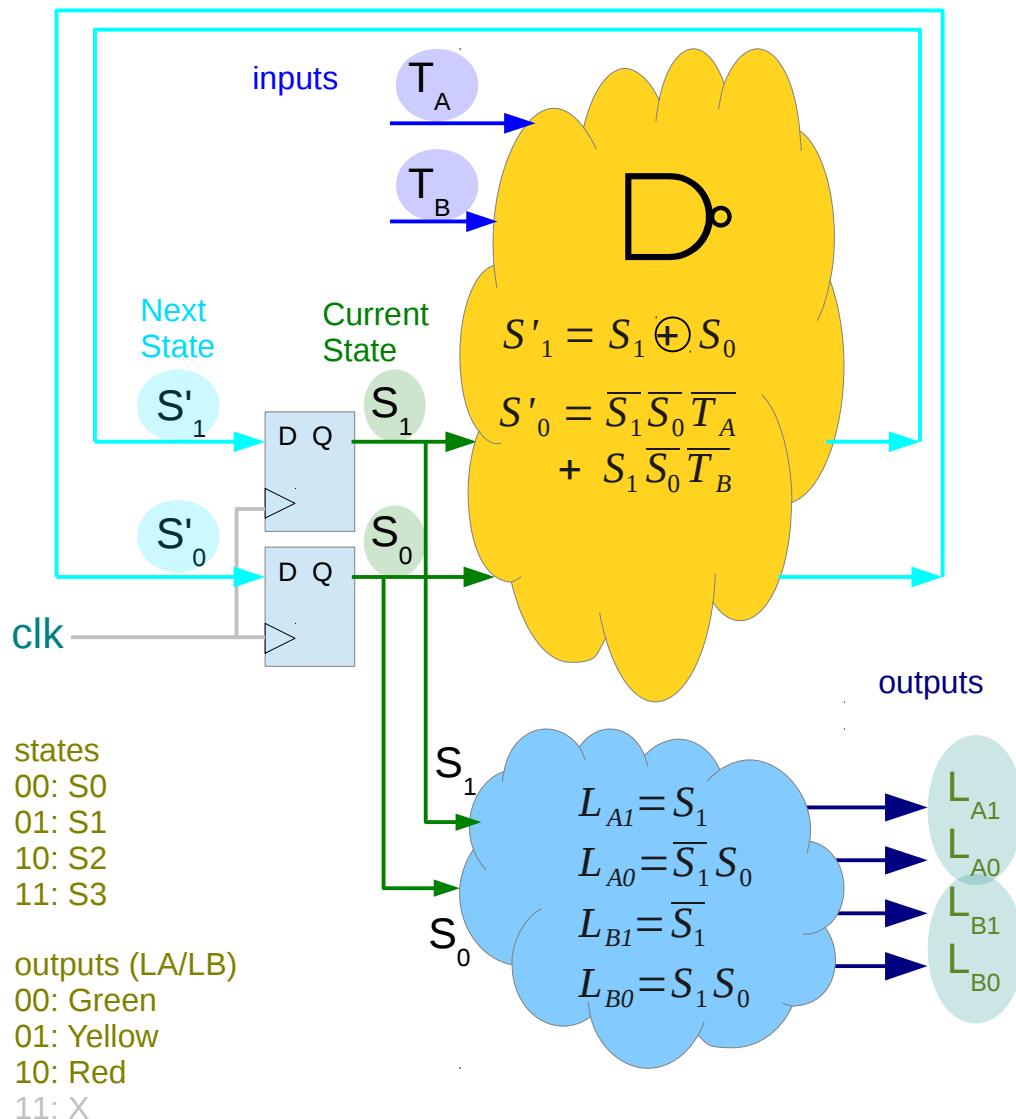
$S_1$	$S_0$	$L_{B0}$
0 0		0
0 1		0
1 0		0
	1 1	1

$$L_{B0} = S_1 S_0$$

# Moore FSM (1)



# Moore FSM



Inputs

$T_A$	$T_B$
$S_1$	$S_0$

Current State



Next States

$$S'_1 = S_1 \oplus S_0$$

$$S'_0 = \overline{S_1} \overline{S_0} \overline{T_A} + S_1 \overline{S_0} \overline{T_B}$$

Current State

$S_1$	$S_0$
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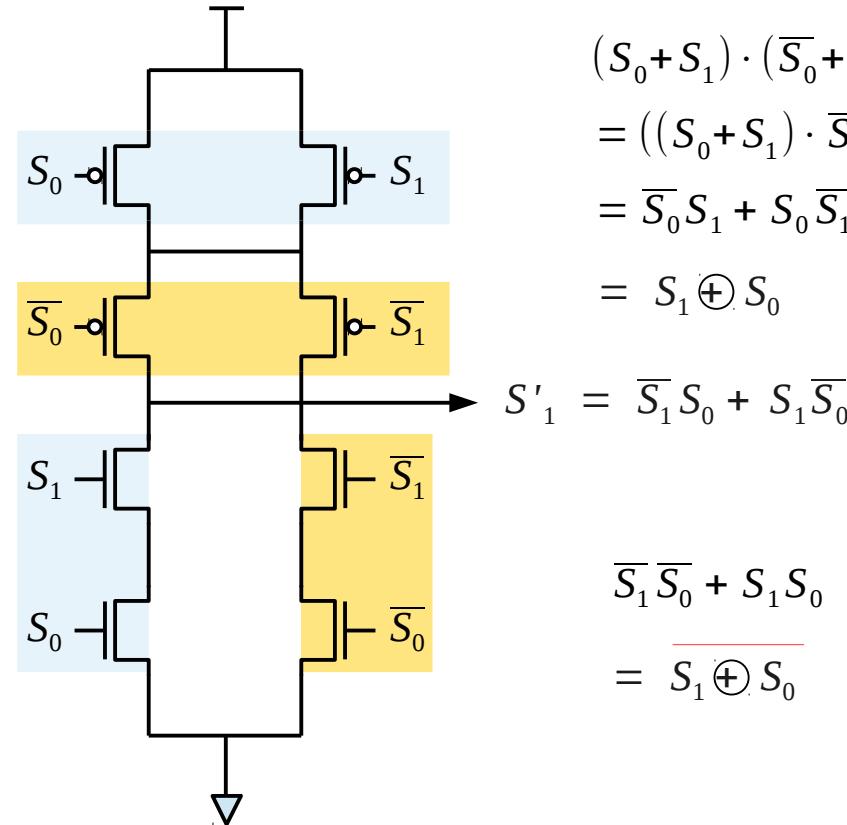
Outputs

$$\begin{array}{ll} L_{A1} = S_1 & L_{B1} = \overline{S_1} \\ L_{A0} = \overline{S_1} S_0 & L_{B0} = S_1 S_0 \end{array}$$

# Function S'1

$$\begin{aligned}S'_{11} &= \overline{S_1}S_0 + S_1\overline{S_0} \\&= S_1 \oplus S_0\end{aligned}$$

$$\overline{S'_{11}} = \overline{S_1}\overline{S_0} + S_1S_0$$



$$\begin{aligned}(S_0 + S_1) \cdot (\overline{S_0} + \overline{S_1}) \\&= ((S_0 + S_1) \cdot \overline{S_0}) + ((S_0 + S_1) \cdot \overline{S_1}) \\&= \overline{S_0}S_1 + S_0\overline{S_1} \\&= S_1 \oplus S_0\end{aligned}$$

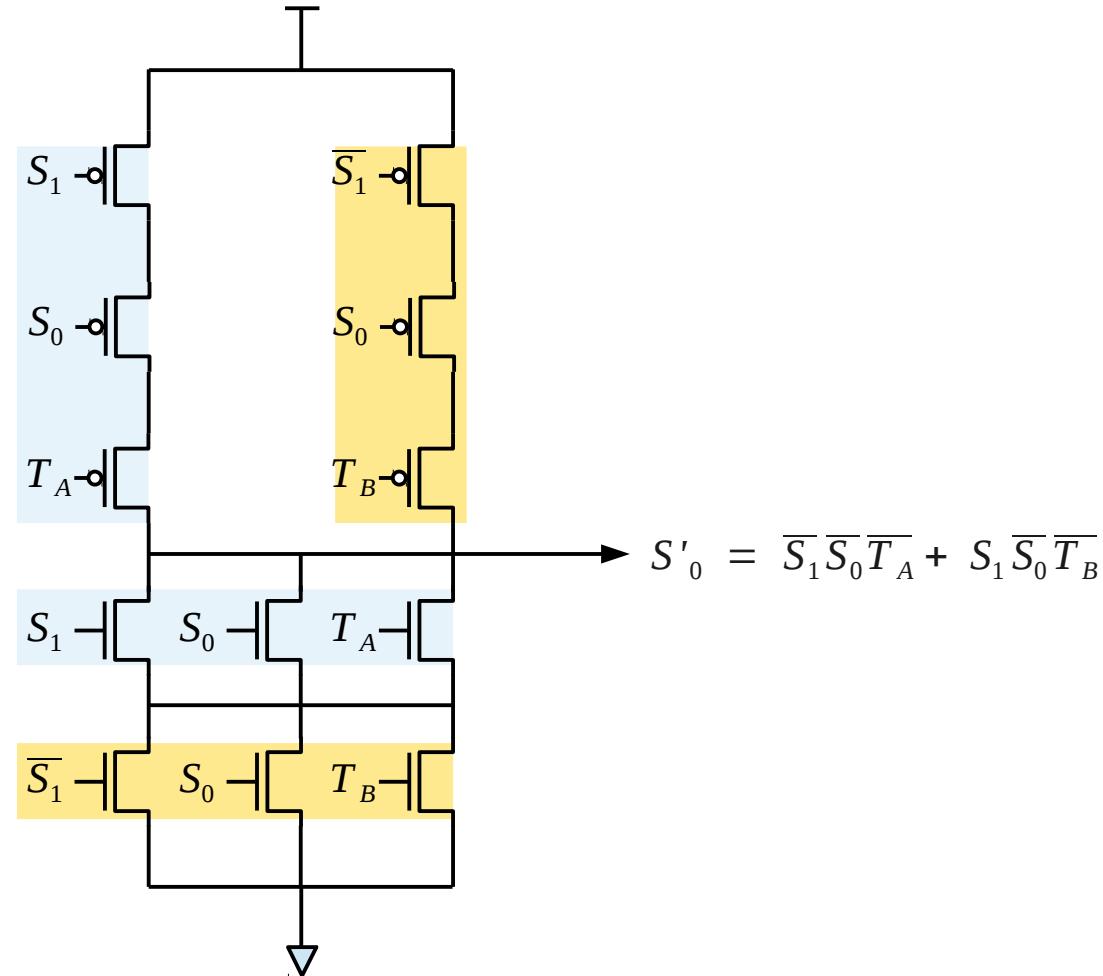
$$S'_{11} = \overline{S_1}S_0 + S_1\overline{S_0}$$

$$\overline{S_1}\overline{S_0} + S_1S_0 \\= \underline{\underline{S_1 \oplus S_0}}$$

# Function S'2

$$S'_0 = \overline{S_1} \overline{S_0} \overline{T_A} + S_1 \overline{S_0} \overline{T_B}$$

$$\begin{aligned} \overline{S'_0} &= \overline{\overline{S_1} \overline{S_0} \overline{T_A}} \cdot \overline{S_1 \overline{S_0} \overline{T_B}} \\ &= (S_1 + S_0 + T_A) \cdot (\overline{S_1} + S_0 + T_B) \end{aligned}$$



# Outputs $L_{A0}$ & $L_{B0}$

$$L_{A0} = \overline{S_1} S_0$$

$$L_{B0} = S_1 S_0$$

$$\begin{aligned}\overline{L_{A0}} &= \overline{\overline{S_1} S_0} \\ &= S_1 + \overline{S_0}\end{aligned}$$

**nMOS PDN**

$$L_{A0} = \overline{(S_1)} \overline{(\overline{S_0})}$$

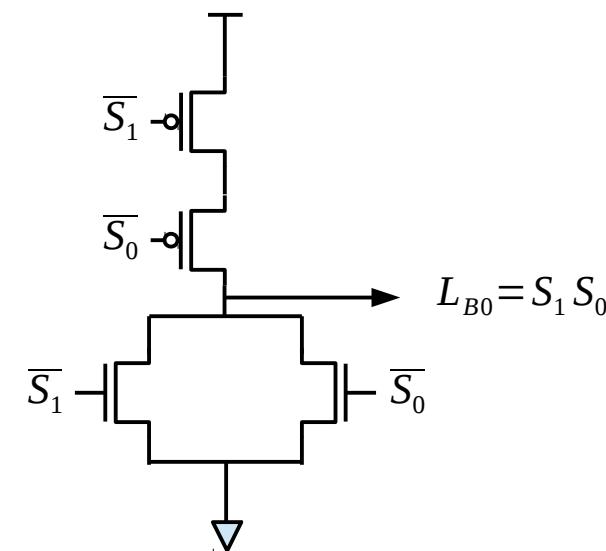
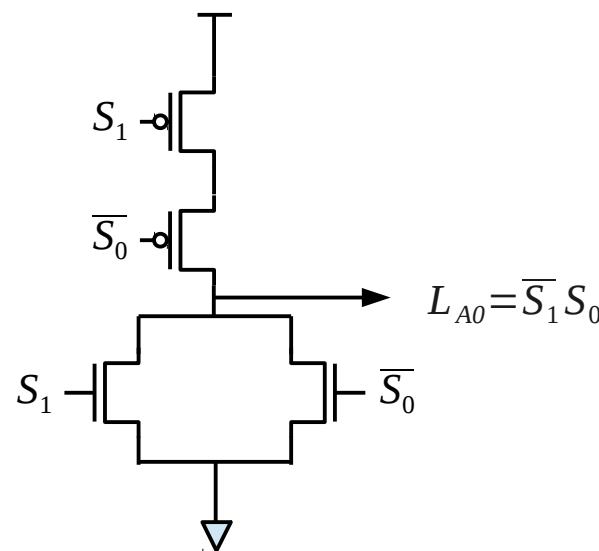
**pMOS PUN**

$$\begin{aligned}\overline{L_{A0}} &= \overline{S_1} \overline{S_0} \\ &= \overline{S_1} + \overline{S_0}\end{aligned}$$

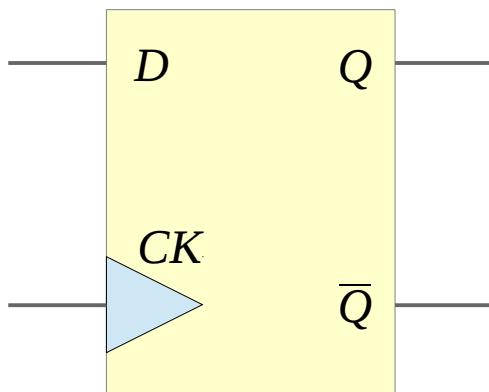
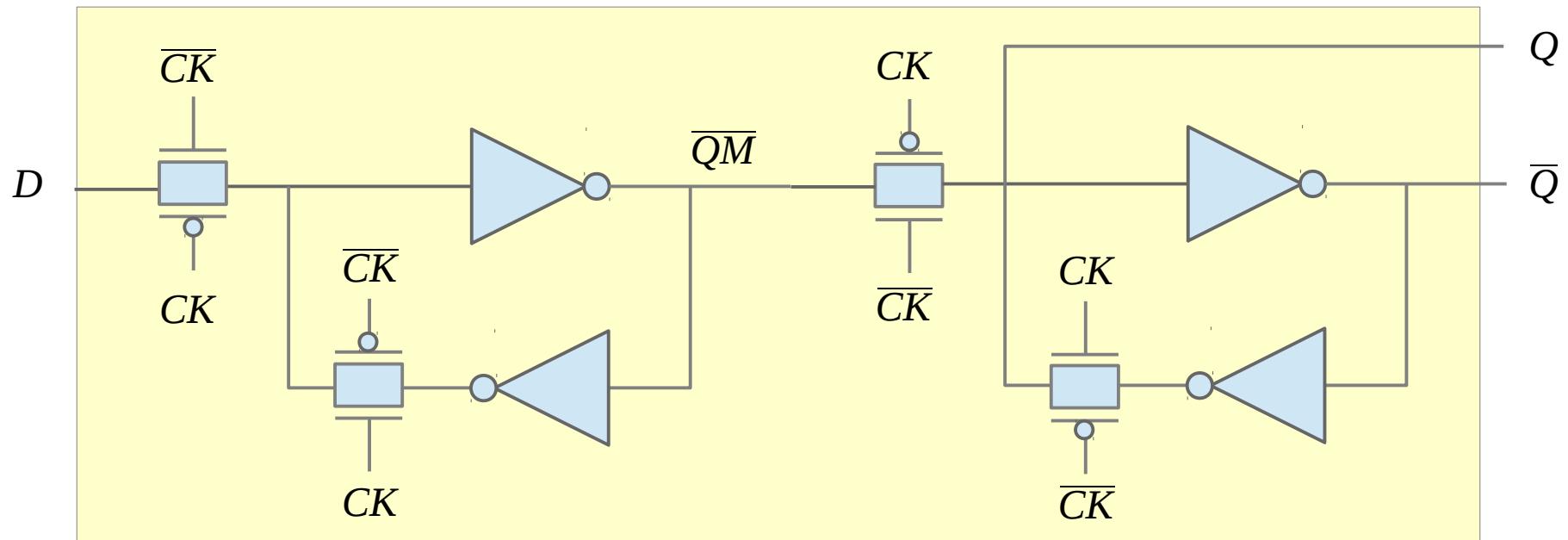
**nMOS PDN**

$$L_{B0} = \overline{(\overline{S_1})} \overline{(\overline{S_0})}$$

**pMOS PUN**



# D Flip Flop with Pass Gate



## References

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- [6] [https://en.wikiversity.org/wiki/The\\_necessities\\_in\\_SOC\\_Design](https://en.wikiversity.org/wiki/The_necessities_in_SOC_Design)
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- [10] [https://en.wikiversity.org/wiki/The\\_necessities\\_in\\_Computer\\_Organization](https://en.wikiversity.org/wiki/The_necessities_in_Computer_Organization)