Wafer Testing (1D)

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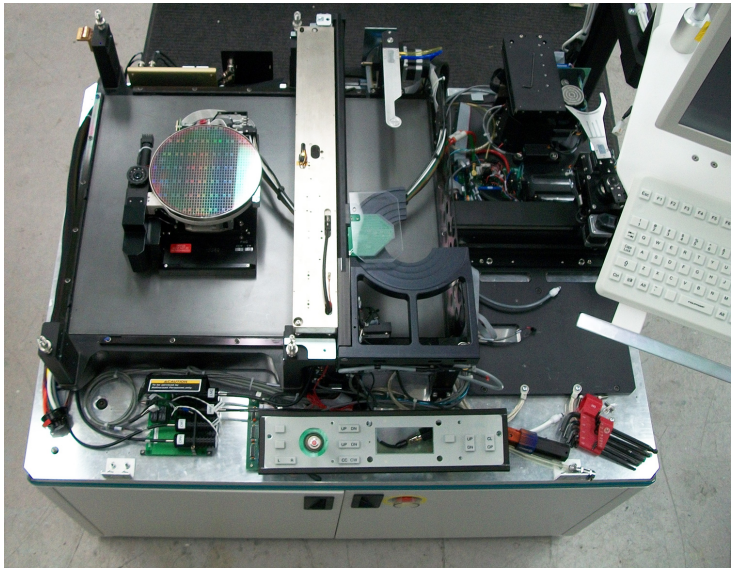
Wafer Testing

Wafer testing is a step performed during semiconductor device fabrication. During this step, performed before a wafer is sent to die preparation, all individual integrated circuits that are present on the wafer are tested for functional defects by applying special test patterns to them. The wafer testing is performed by a piece of test equipment called a wafer prober. The process of wafer testing can be referred to in several ways: Wafer Sort (WS), Wafer Final Test (WFT), Electronic Die Sort (EDS) and Circuit Probe (CP) are probably the most common.

Wafer Prober

A wafer prober is a machine used to test integrated circuits. For electrical testing a set of microscopic contacts or probes called a probe card are held in place whilst the wafer, vacuum-mounted on a wafer chuck, is moved into electrical contact. When a die (or array of dice) have been electrically tested the prober moves the wafer to the next die (or array) and the next test can start. The wafer prober is usually responsible for loading and unloading the wafers from their carrier (or cassette) and is equipped with automatic pattern recognition optics capable of aligning the wafer with sufficient accuracy to ensure accurate registration between the contact pads on the wafer and the tips of the probes.



Yield

Once the front-end process has been completed, the semiconductor devices are subjected to a variety of electrical tests to determine if they function properly. The proportion of devices on the wafer found to perform properly is referred to as the **yield**. Manufacturers are typically secretive about their yields, but it can be as low as 30%.

The fab tests the chips on the wafer with an electronic tester that presses tiny probes against the chip. The machine marks each bad chip with a drop of dye.

Chips are also tested again after packaging, as the bond wires may be missing, or analog performance may be altered by the package. This is referred to as "final test".

Test Software

Usually, the fab charges for test time, with prices in the order of cents per second. Test times vary from a few milliseconds to a couple of seconds, and the test software is optimized for reduced test time. Multiple chip (multi-site) testing is also possible, since many testers have the resources to perform most or all of the tests in parallel.

Chips are often designed with "**testability features**" such as scan chains and "built-in self-test" to speed testing, and reduce test costs. In certain designs that use specialized **analog** fab processes, wafers are also laser-trimmed during test, to achieve tightly-distributed resistance values as specified by the design.

Good designs try to test and statistically manage **corners**: extremes of silicon behavior caused by operating temperature combined with the extremes of fab processing steps. Most designs cope with more than 64 corners.

References

[1] http://en.wikipedia.org/