

Some Useful Links

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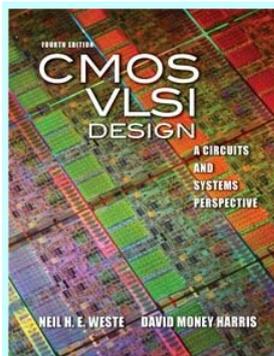
Some useful links in VLSI designs

Weste <http://pages.hmc.edu/harris/cmosvlsi/4e/index.html>
Rabaey <http://bwrcs.eecs.berkeley.edu/Classes/IcBook/instructors.html>
Mason <http://www.egr.msu.edu/classes/ece410/mason/>
Baker <http://cmosedu.com/cmos1/book.htm>

Electric Layout Tool

<http://www.staticfreesoft.com/index.html>
<http://cmosedu.com/cmos1/electric/electric.htm>

Weste <http://pages.hmc.edu/harris/cmosvlsi/4e/index.html>



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Lectures

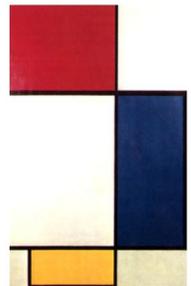
Lecture	Topic	PowerPoint	PDF
0	Introduction	ppt	pdf
1	Circuits & Layout	ppt	pdf
2	Design Flow	ppt	pdf
3	Transistor Theory	ppt	pdf
4	Nonideal Transistors	ppt	pdf
5	DC & Transient Response	ppt	pdf
6	Logical Effort	ppt	pdf
7	Power	ppt	pdf
8	Simulation	ppt	pdf
9	Combinational Circuit Design	ppt	pdf
10	Circuit Families	ppt	pdf
11	Sequential Circuit Design	ppt	pdf
12	Design for Testability	ppt	pdf
14	Wires	ppt	pdf
15	Scaling	ppt	pdf
16	Pitfalls & Reliability	ppt	pdf
17	Adders	ppt	pdf
18	Datapaths	ppt	pdf
19	SRAM	ppt	pdf
20	ROMs, CAMs, & PLAs	ppt	pdf
21	Packaging, Power, & Clock	ppt	pdf
22	PLLs & DLLs	ppt	pdf
23	I/O	ppt	pdf
24	Microprocessor Hall of Fame	ppt	pdf

Rabaey <http://bwracs.eecs.berkeley.edu/Classes/lcBook/instructors.html>

Click on the corresponding header to download the slide-sets covering the different chapters.

- **Design rules** - [PPT](#) or [PDF \(151 kB\)](#)
- **SCMOS Design rules** - [pdf](#)
- **Chapter 1: Introduction** - [PPT](#) or [PDF \(1,259 kB\)](#)
- **Chapter 2: Devices** - [PPT](#) or [PDF \(2,292 kB\)](#)
- **Chapter 3: Inverter** [PPT](#) or [PDF \(2,096 kB\)](#)
- **Chapter 4 (1): Combinational Logic in CMOS** - [PPT](#) or [PDF \(1,154 kB\)](#)
- **Chapter 4 (2): Low Power Design** - [PPT](#) or [PDF \(365 kB\)](#)
- **Chapter 5: High Performance Design** - [PPT](#) or [PDF \(268 kB\)](#)
- **Chapter 6: Sequential Logic** - [PPT](#) or [PDF \(1,451 kB\)](#)
- **Chapter 7: Arithmetic** - [PPT](#) or [PDF \(1,611 kB\)](#)
- **Chapter 8: Interconnect** - [PPT](#) or [PDF \(1,784 kB\)](#)
- **Chapter 9: Timing** - [PPT](#) or [PDF \(1,387 kB\)](#)
- **Chapter 10: Semiconductor memory** - [PPT](#) or [PDF \(1,975 kB\)](#)
- **Chapter 11: Design methodologies** - [PPT](#) or [PDF \(1,967 kB\)](#)

Design Methodologies



Digital Integrated Circuits

Design Methodologies

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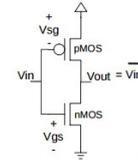
MSU <http://www.egr.msu.edu/classes/ece410/mason/>

Lecture Notes

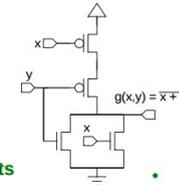
- © Power Point Slide: <[Introduction](#)> <[Ch.2 switch logic](#)> <[Ch.3-5 technology](#)> <[Ch.6 physics/modeling](#)> <[Ch.7 performance analysis](#)> <[Ch.11 CMOS digital functions](#)> <[Ch.12 arithmetic circuits](#)> <[Ch.13 memory](#)> <[Advanced Digital](#)> <[MEMS Overview](#)>
- © Extras: [LOCOS Slide Show](#) (for viewing, not printing).

Review: CMOS Logic Gates

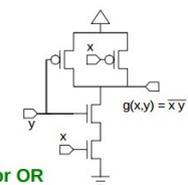
- INV Schematic
- NOR Schematic
- NAND Schematic



- CMOS inverts functions

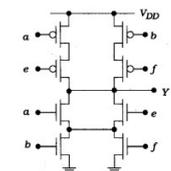
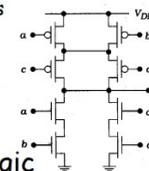


- parallel for OR
- series for AND



- CMOS Combinational Logic

- use DeMorgan relations to reduce functions
 - remove all NAND/NOR operations
- implement nMOS network
- create pMOS by complementing operations



- AOI/OAI Structured Logic

- XOR/XNOR using structured logic



Patel <http://www.csee.umbc.edu/~cpatel2/links/640/>

▶ Syllabus: [Fall 2015 syllabus](#)

▶ Lecture 1: [Introduction](#)

▶ Lecture 2: [CMOS Basics I](#)

▶ Lecture 3: [CMOS Basics II](#)

▶ Lecture 4: [Quality Metrics I](#)

▶ Lecture 5: [Quality Metrics II](#)

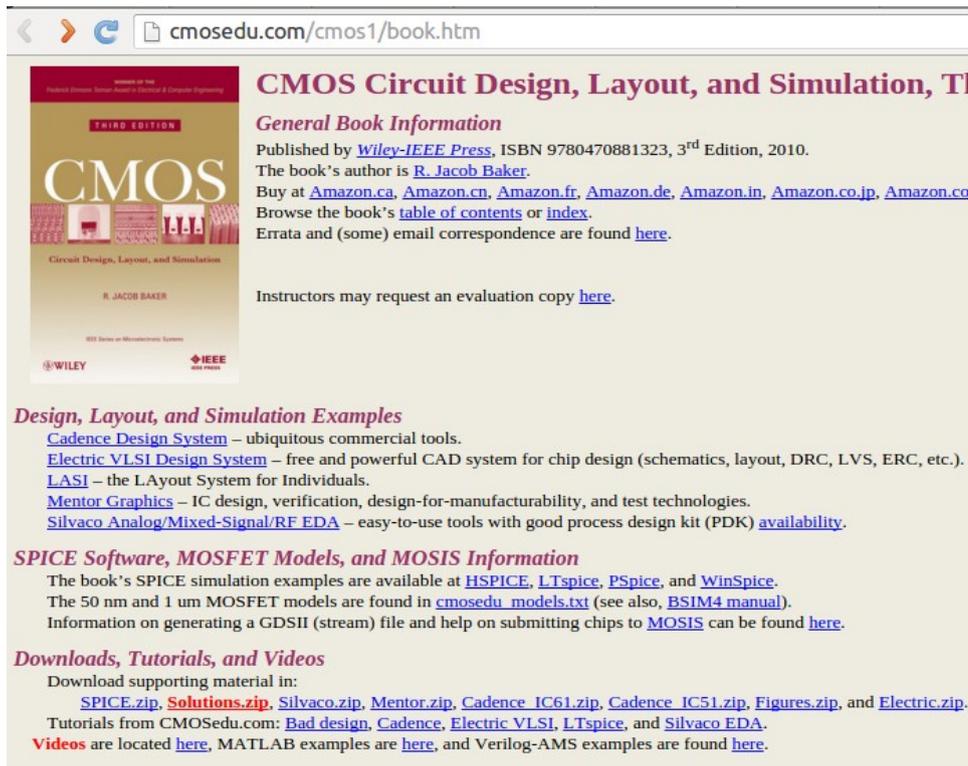
▶ Lecture 6: [Diode Details](#)

▶ Lecture 7: [MOS Transistor Details](#)

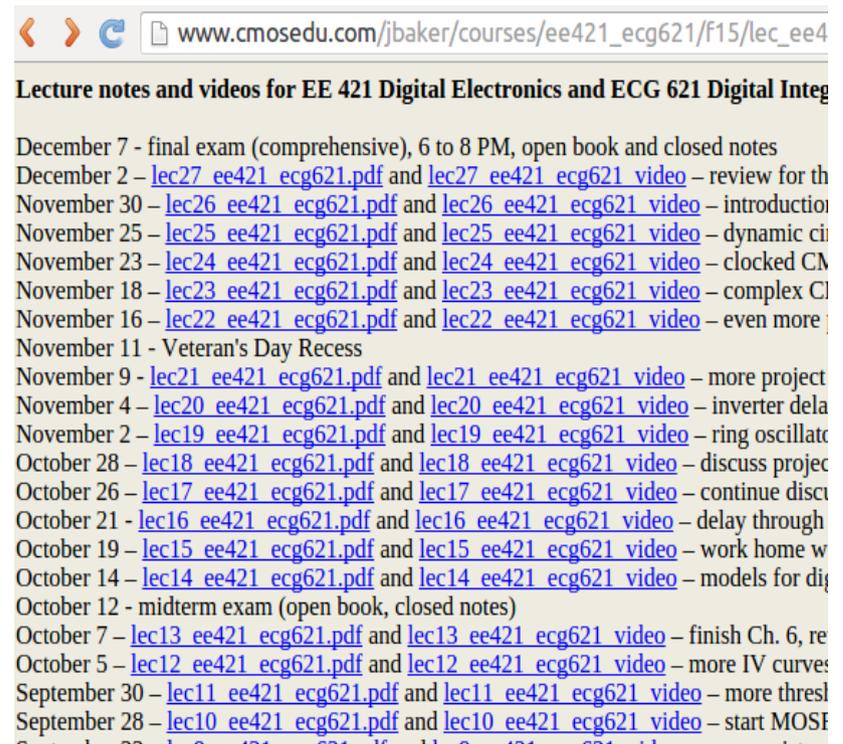
Advanced VLSI Design	CMOS Processing Technology	CMPE 640
CMOS Processing Technology		
<p>Silicon: a semiconductor with resistance between that of conductor and an insulator.</p> <p>Conductivity of silicon can be changed several orders of magnitude by introducing impurity atoms in silicon crystal lattice.</p> <ul style="list-style-type: none">○ Impurities that use electrons: acceptors (p-type), e.g., Boron.○ Impurities that provide electrons: donors (n-type), e.g., Phosphorous. <p>Wafer: 10 cm to 30 cm (~4 to ~12 inches) and 1 mm thick.</p> <p>Wafers are cut from ingots of single-crystal silicon, that have been pulled from a crucible melt of pure molten silicon at 1425 degrees C (Czochralski method).</p> <p>Controlled amounts of impurities are added to the melt to enable the proper electrical properties.</p>		

Baker <http://cmosedu.com/cmos1/book.htm>

http://www.cmosedu.com/jbaker/courses/ee421_ecg621/f15/lec_ee421_ecg621.htm



The screenshot shows a web browser window with the URL cmosedu.com/cmos1/book.htm. The page features the book cover for 'CMOS Circuit Design, Layout, and Simulation, Third Edition' by R. Jacob Baker, published by Wiley-IEEE Press. The cover is yellow and red with the title 'CMOS' in large letters. To the right of the cover, the text reads: 'CMOS Circuit Design, Layout, and Simulation, Third Edition', 'General Book Information', 'Published by Wiley-IEEE Press, ISBN 9780470881323, 3rd Edition, 2010.', 'The book's author is R. Jacob Baker.', 'Buy at Amazon.ca, Amazon.cn, Amazon.fr, Amazon.de, Amazon.in, Amazon.co.jp, Amazon.com.', 'Browse the book's table of contents or index.', 'Errata and (some) email correspondence are found here.', and 'Instructors may request an evaluation copy here.' Below this, there are sections for 'Design, Layout, and Simulation Examples' (listing Cadence Design System, Electric VLSI Design System, LASI, Mentor Graphics, and Silvaco Analog/Mixed-Signal/RF EDA), 'SPICE Software, MOSFET Models, and MOSIS Information' (listing HSPICE, LTspice, PSpice, WinSpice, and cmosedu_models.txt), and 'Downloads, Tutorials, and Videos' (listing SPICE.zip, Solutions.zip, Silvaco.zip, Mentor.zip, Cadence IC61.zip, Cadence IC51.zip, Figures.zip, and Electric.zip).



The screenshot shows a web browser window with the URL www.cmosedu.com/jbaker/courses/ee421_ecg621/f15/lec_ee421_ecg621.htm. The page is titled 'Lecture notes and videos for EE 421 Digital Electronics and ECG 621 Digital Integration'. It contains a list of dates and links to lecture notes and videos. The dates range from December 7 to September 28. The links are in the format [lecXX ee421 ecg621.pdf](#) and [lecXX ee421 ecg621 video](#). The dates and links are: December 7 - final exam (comprehensive), 6 to 8 PM, open book and closed notes; December 2 - [lec27 ee421 ecg621.pdf](#) and [lec27 ee421 ecg621 video](#) - review for the final; November 30 - [lec26 ee421 ecg621.pdf](#) and [lec26 ee421 ecg621 video](#) - introduction to digital logic; November 25 - [lec25 ee421 ecg621.pdf](#) and [lec25 ee421 ecg621 video](#) - dynamic CMOS; November 23 - [lec24 ee421 ecg621.pdf](#) and [lec24 ee421 ecg621 video](#) - clocked CMOS; November 18 - [lec23 ee421 ecg621.pdf](#) and [lec23 ee421 ecg621 video](#) - complex CMOS; November 16 - [lec22 ee421 ecg621.pdf](#) and [lec22 ee421 ecg621 video](#) - even more CMOS; November 11 - Veteran's Day Recess; November 9 - [lec21 ee421 ecg621.pdf](#) and [lec21 ee421 ecg621 video](#) - more project; November 4 - [lec20 ee421 ecg621.pdf](#) and [lec20 ee421 ecg621 video](#) - inverter delay; November 2 - [lec19 ee421 ecg621.pdf](#) and [lec19 ee421 ecg621 video](#) - ring oscillator; October 28 - [lec18 ee421 ecg621.pdf](#) and [lec18 ee421 ecg621 video](#) - discuss project; October 26 - [lec17 ee421 ecg621.pdf](#) and [lec17 ee421 ecg621 video](#) - continue discussion; October 21 - [lec16 ee421 ecg621.pdf](#) and [lec16 ee421 ecg621 video](#) - delay through CMOS; October 19 - [lec15 ee421 ecg621.pdf](#) and [lec15 ee421 ecg621 video](#) - work home with CMOS; October 14 - [lec14 ee421 ecg621.pdf](#) and [lec14 ee421 ecg621 video](#) - models for digital logic; October 12 - midterm exam (open book, closed notes); October 7 - [lec13 ee421 ecg621.pdf](#) and [lec13 ee421 ecg621 video](#) - finish Ch. 6, review; October 5 - [lec12 ee421 ecg621.pdf](#) and [lec12 ee421 ecg621 video](#) - more IV curves; September 30 - [lec11 ee421 ecg621.pdf](#) and [lec11 ee421 ecg621 video](#) - more threshold voltage; September 28 - [lec10 ee421 ecg621.pdf](#) and [lec10 ee421 ecg621 video](#) - start MOSFET.

Electric Layout Tool

<http://www.staticfreesoft.com/index.html>

The image shows a screenshot of a web browser displaying the Static Free Software website. The website has a navigation menu with links for Home, About, Products, Documentation, and Contact Us. The main content area features the Static Free Software logo and the text "Home of the Electric VLSI Design System". Below this, there is a question: "Can Your CAD System Do This? Is it Free?".

Below the website screenshot is a screenshot of the Electric VLSI Design System software interface. The interface is titled "Electric" and has a menu bar with File, Edit, Cell, Export, View, Window, Tool, and Help. The main workspace is divided into several panes:

- txPadAmp[sch]:** A schematic diagram of a circuit with components labeled X=0.5, X=1, X=4, and outputs in[1], out[1], and out[1].
- 3D View: nmosGate[lay]:** A 3D perspective view of a multi-layer printed circuit board (PCB) layout.
- half_toggle_6x[lay]:** A 2D layout view showing a grid of components.
- Record(doc):** A text window showing a change record for a document.

Harris' Computer Architecture Book

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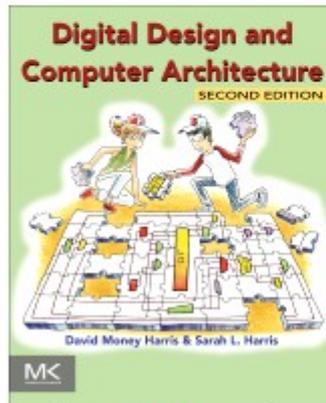


COMPANION MATERIALS

Harris, Harris: Digital Design and Computer Architecture, 2

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Digital Design and Computer Architecture About this Companion Site

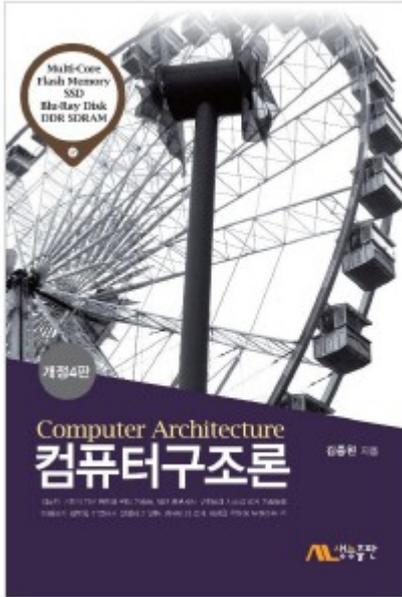
This companion site hosts Solutions to Odd-Numbered Exercises, HDL Files, Lecture Slides, Links to CAD Tools, and
Solutions to Odd-Numbered Exercises

Solutions to odd-numbered exercises are available to instructors for an electronic computing system (www.euroarms.net · 2006.)
textbooks.elsevier.com/9780123944245)

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Architecture		Instructions Registers
Micro-architecture		Datapaths Controllers
Logic		Adders Memories
Digital Circuits		AND Gates NOT Gates
Analog Circuits		Amplifiers Filters
Devices		Transistors Diodes
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Computer Architecture



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컴퓨터구조론

개정판 4판 | 양장본

김종현 지음 | 생능출판사 | 2014년 01월 10일 출간

이 책의 개정정보 : 2015년 출간 ▼

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References

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- [2] <http://www.allaboutcircuits.com/>
- [3] W. Wolf, "Modern VLSI Design : Systems on Silicon"
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- [5] J. P. Uyemura, "Introduction to VLSI Circuits and Systems"
- [6] https://en.wikiversity.org/wiki/The_necessities_in_SOC_Design
- [7] https://en.wikiversity.org/wiki/The_necessities_in_Digital_Design
- [8] https://en.wikiversity.org/wiki/The_necessities_in_Computer_Design
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