CMOS Pass Transistor (H.1)

20151219

Common Gate Mode (Pass Transistor)

References

Some Figures from the following sites

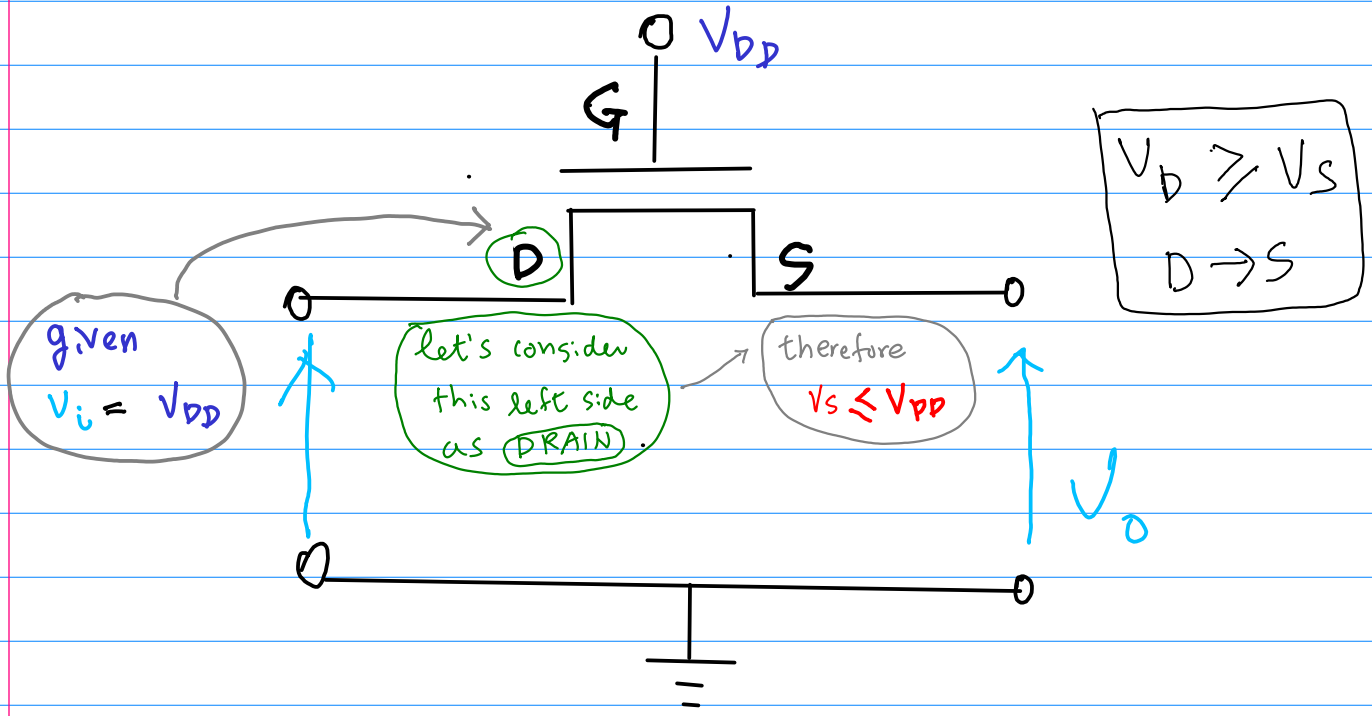
[1] http://pages.hmc.edu/harris/cmosvlsi/4e/index.html
Weste & Harris Book Site

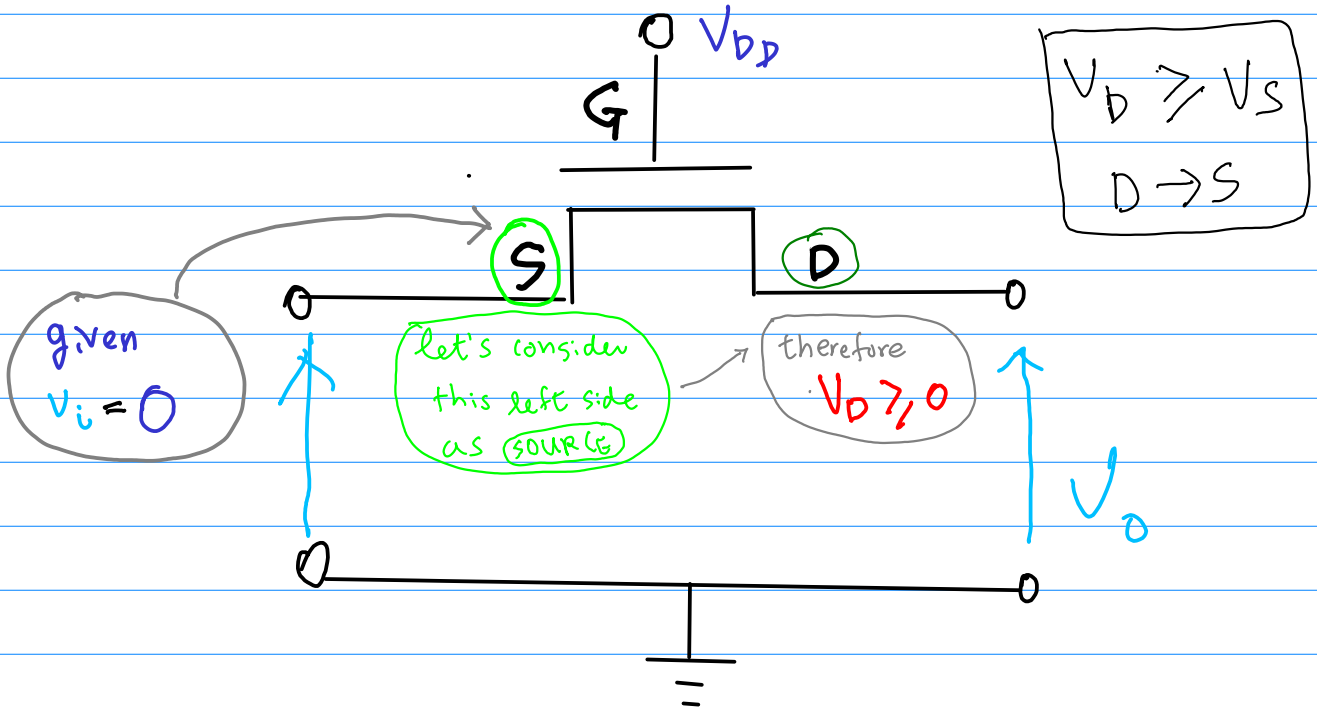
[2] en.wikipedia.org

Pass Transistor Configuration

Symmetric (S)ource & (D)rain

nMOS I_{DS} (+) D → S $V_D > V_S$

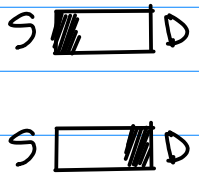




① Cut off

$$V_{GS} < V_t$$

② Linear



$$0 < V_t < V_{GS}$$
$$0 < V_t < V_{GD}$$

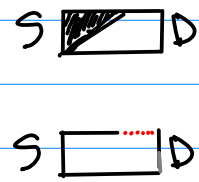
$\equiv$

$$0 < V_t < V_{GS}$$
$$V_{DS} < V_{GS} - V_t$$

$V_{GD} = V_{GS} - V$

$V_{GS} -$

③ Saturation

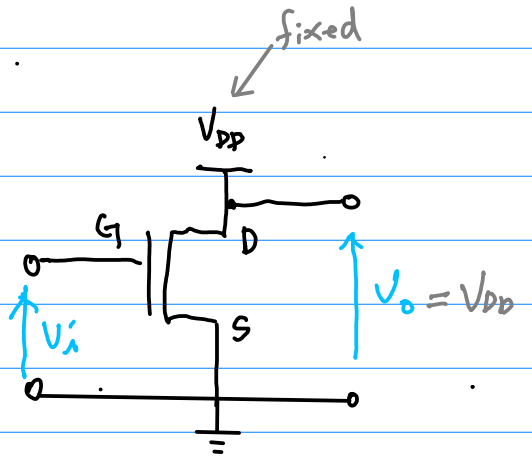


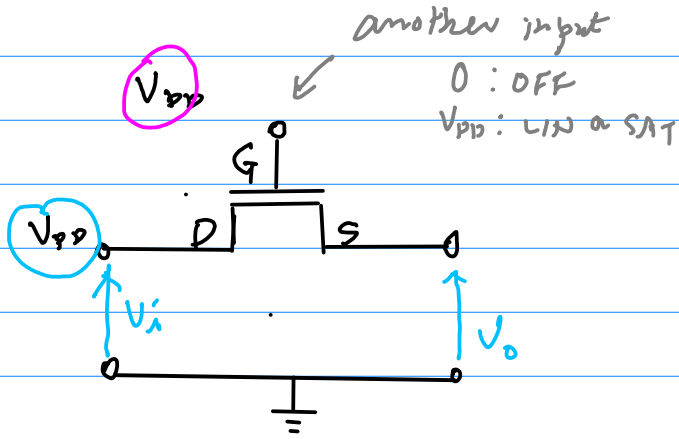
$$0 < V_t < V_{GS}$$
$$V_{GD} < V_t$$

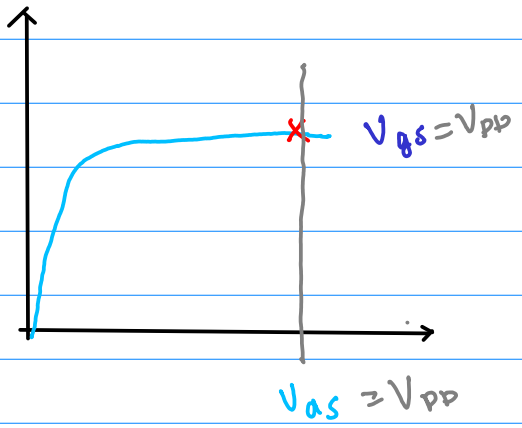
$\equiv$

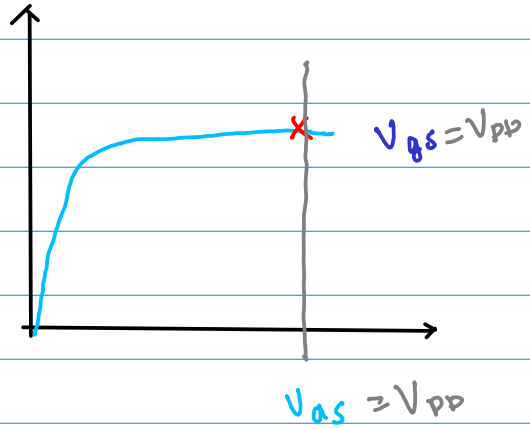
$$0 < V_t < V_{GS}$$
$$V_{GS} - V_t < V_{DS}$$

(*) also nMOS pass transistor must be in either SAT or LIN to "pass" v_i to v_o



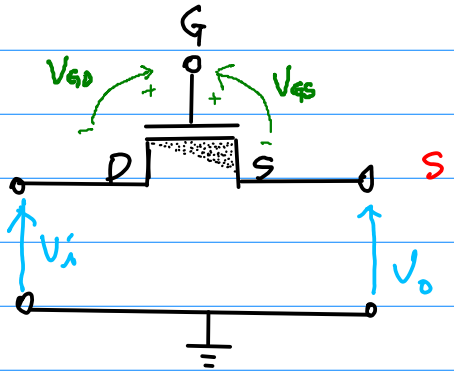






$V_{DS} = V_D - V_S$

$= V_{DD} - V_S > V_t$



$V_{GS} > V_t$ $\quad$ $V_{GS} > V_t$

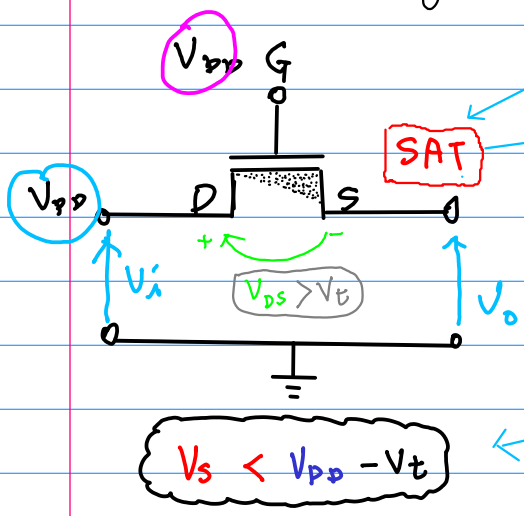
$V_{GD} > V_t$ $\quad$ $V_{GD} < V_t$

LIN $\quad$ SAT

$V_{GD} = V_G - V_D$

$= V_{DD} - V_{DD} = 0$

$0 = V_{GD} < V_t$



$V_{GS} > V_t$

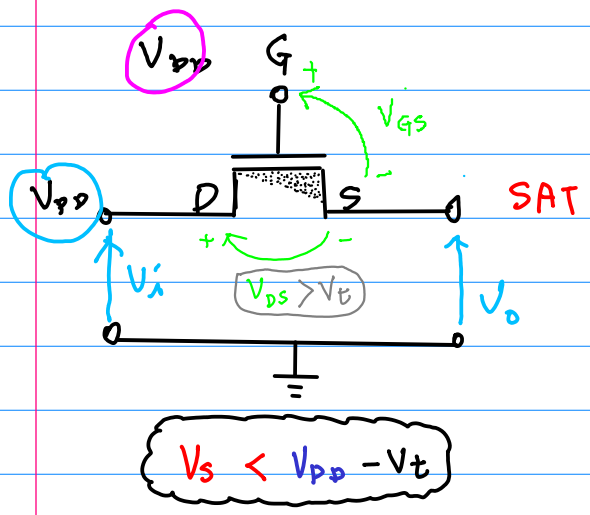
$V_{GS} = V_G - V_S > V_t$

$V_{DD} - V_S > V_t$

$V_{DD} - V_t > V_S$

$V_S < V_{DD} - V_t$

Condition: must not turn off



$V_S < V_{DD} - V_t$

SAT $\begin{cases} V_{GS} > V_t \\ V_{DS} > V_{GS} - V_t \end{cases}$

$$V_{GS} = V_G - V_S = V_{DD} - V_S > V_t$$

$$V_{DS} = V_D - V_S = V_{DD} - V_S > V_t$$

$V_{S,min} = 0$

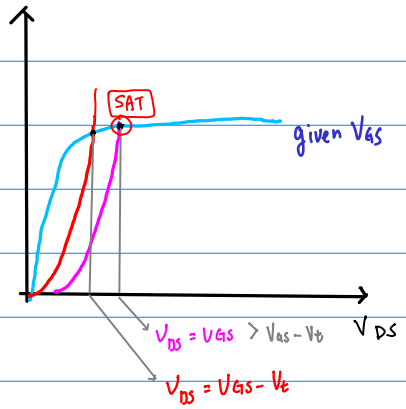
$V_{S,max} = V_{DD} - V_t$

$V_S \in [0,\ V_{DD} - V_t]$

$V_{DS,max} = V_{GS,max} = V_{DD}$

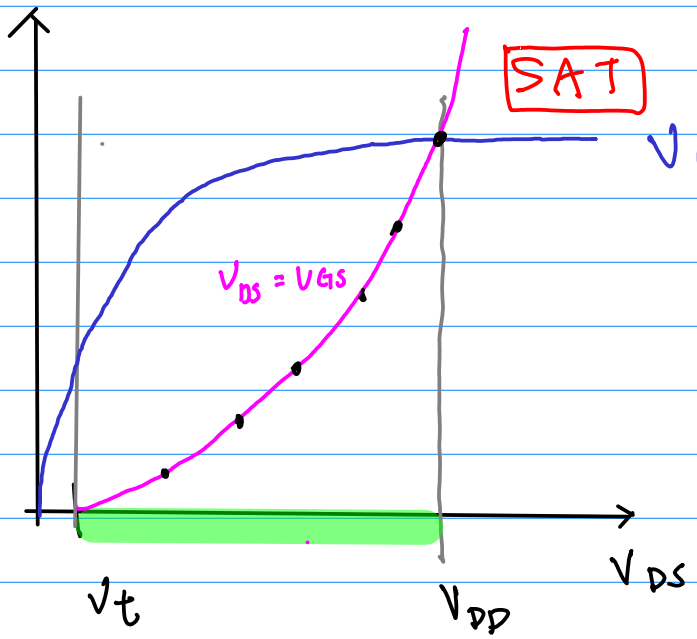
$V_{DS,min} = V_{GS,min} = V_t$

$V_{DS} = V_{GS} \in [V_t,\ V_{DD}]$



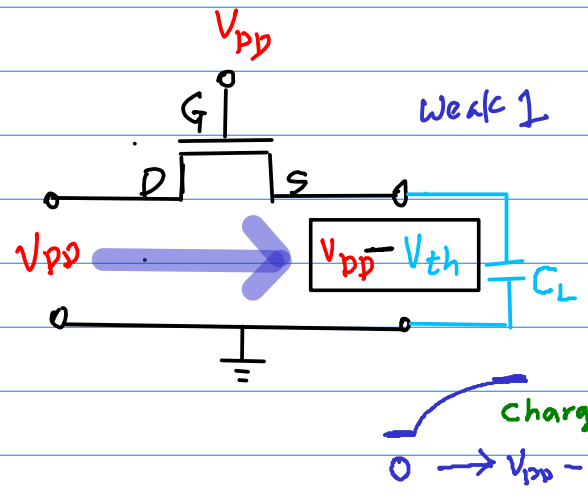
$V_{DS} = V_{GS} > V_{GS} - V_t \Leftarrow (V_{DS} = V_{GS})$

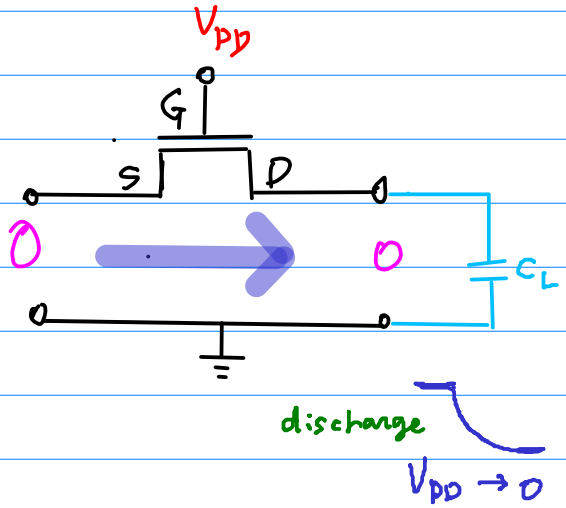
$V_{DS} = V_{GS} - V_t \Leftarrow V_{DS} \geq V_{GS} - V_t$

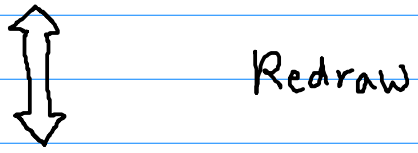


$V_S \in [0,\ V_{DD} - V_t]$

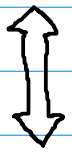
$V_{DS} = V_{GS} \in [V_t,\ V_{DD}]$

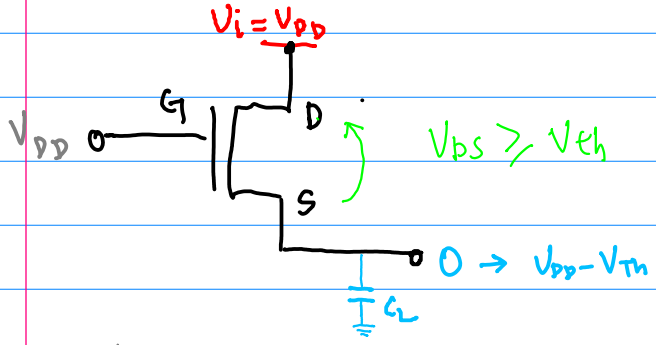




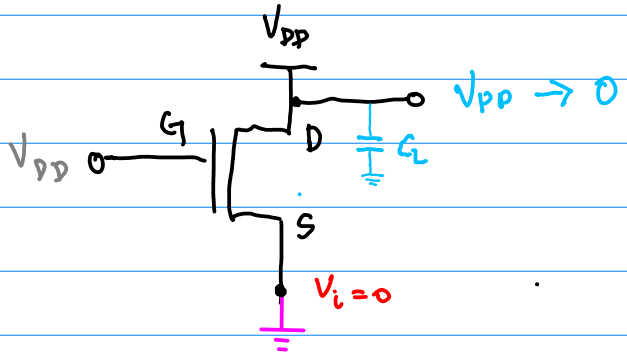


Redraw



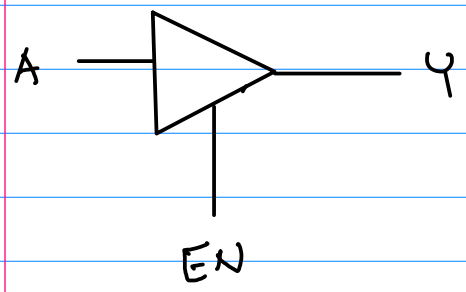


Charging Load Capacitor

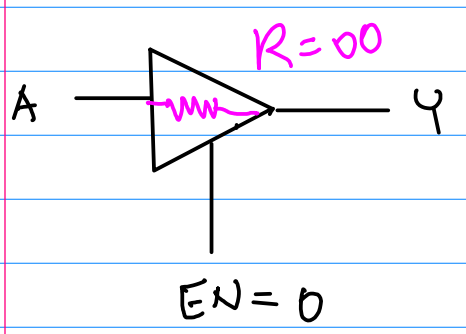


discharging Load capacitor

Tristate Buffer

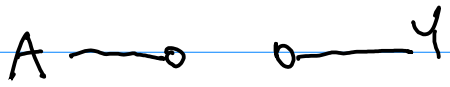


A	EN	Y	
0	0	Z	) state
1	0	Z	) state
0	1	0	) state
1	1	1	) state

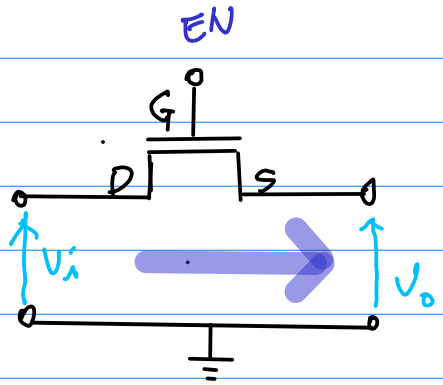


≅

High Impedence Z



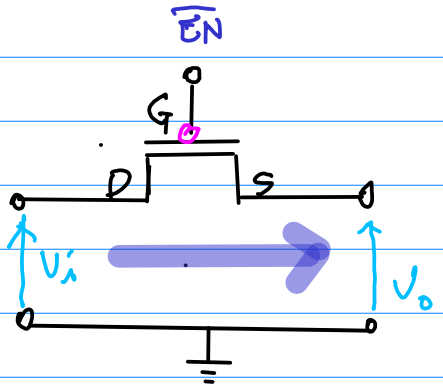
open circuit
disconnect
electrically



nMOS

0 → strong 0

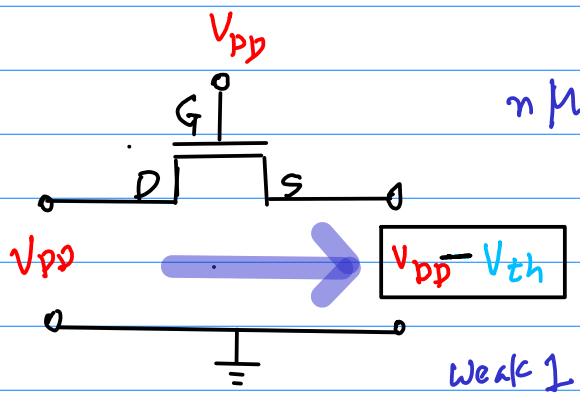
1 → weak 1



pMOS

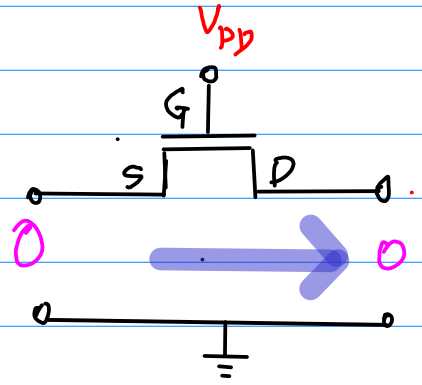
0 → weak 0

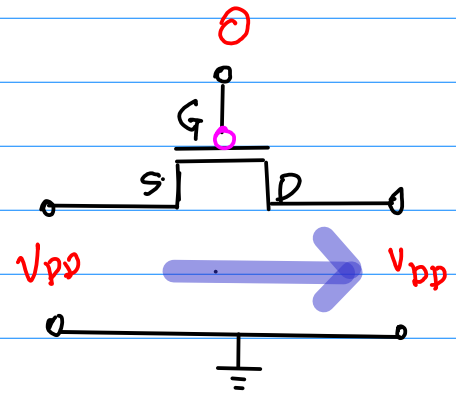
1 → strong 1



nMOS

Weak 1





pMOS