MOSFET Theory (H.3)

20160407

Various nMOS Capacitance

(I) Oxide related Cap.

* Voltage dependent components

depends on inversion channel.
affected by mode (OFF, LIN, SAT)

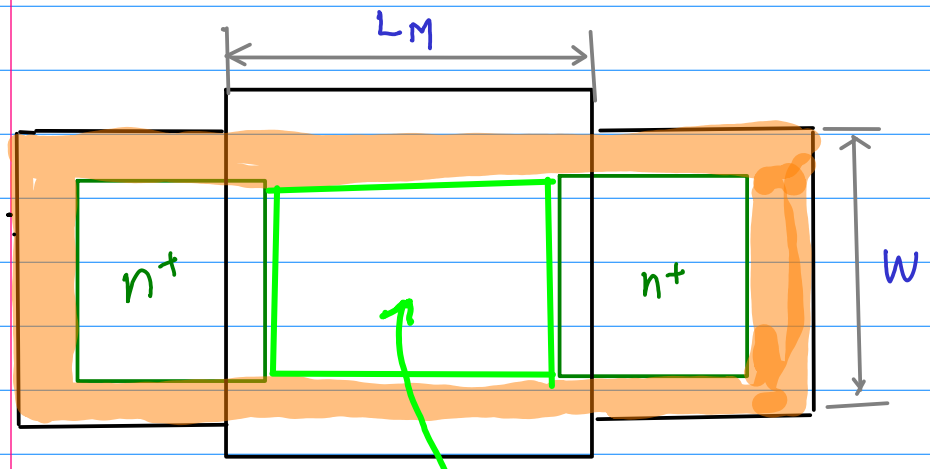
* Voltage independent components

overlap capacitance

(II) Diffusion Area Cap.

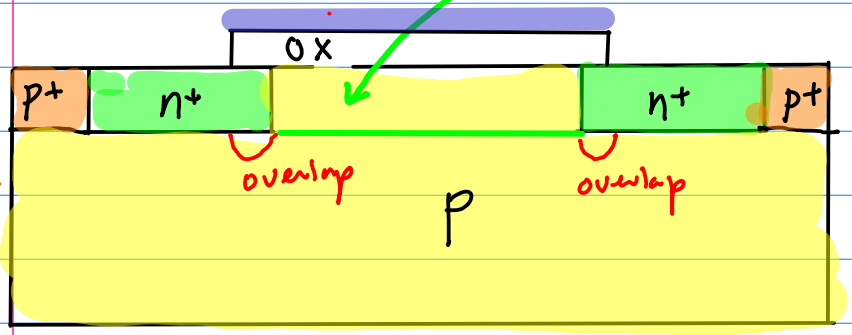
Junction Capacitance

Channel Stop Implant



Top View

inversion channel can exist in this region



cross section view

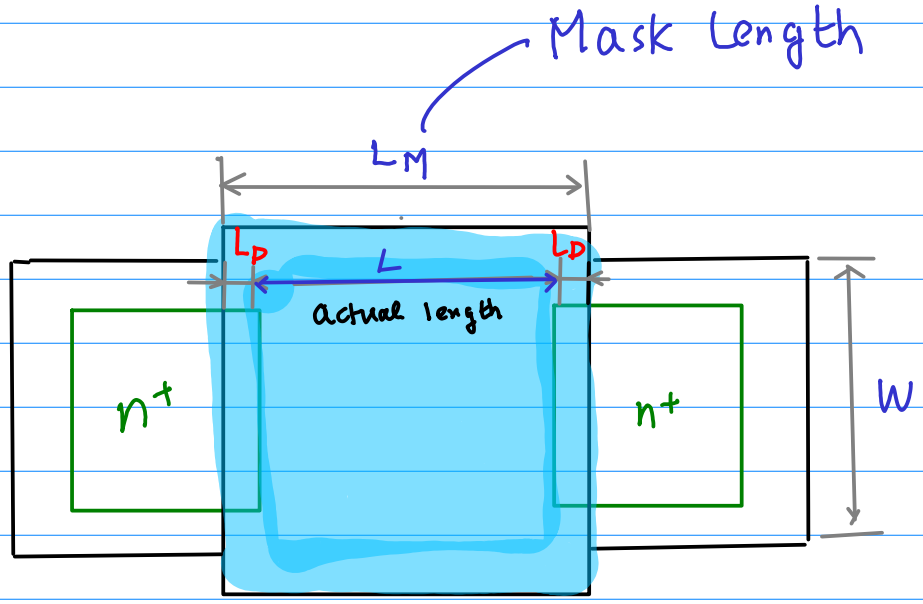
To prevent unwanted parasitic channel

① P^+ doped region (heavily doped)

② FOX: Field Oxide (SiO_2)

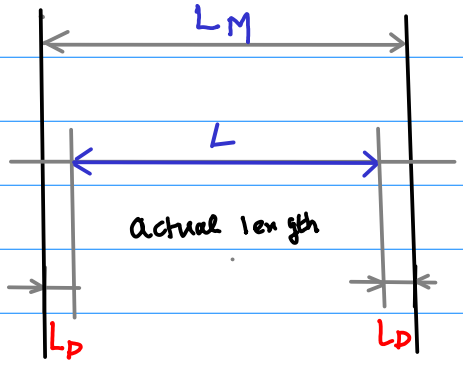
* Channel stopper

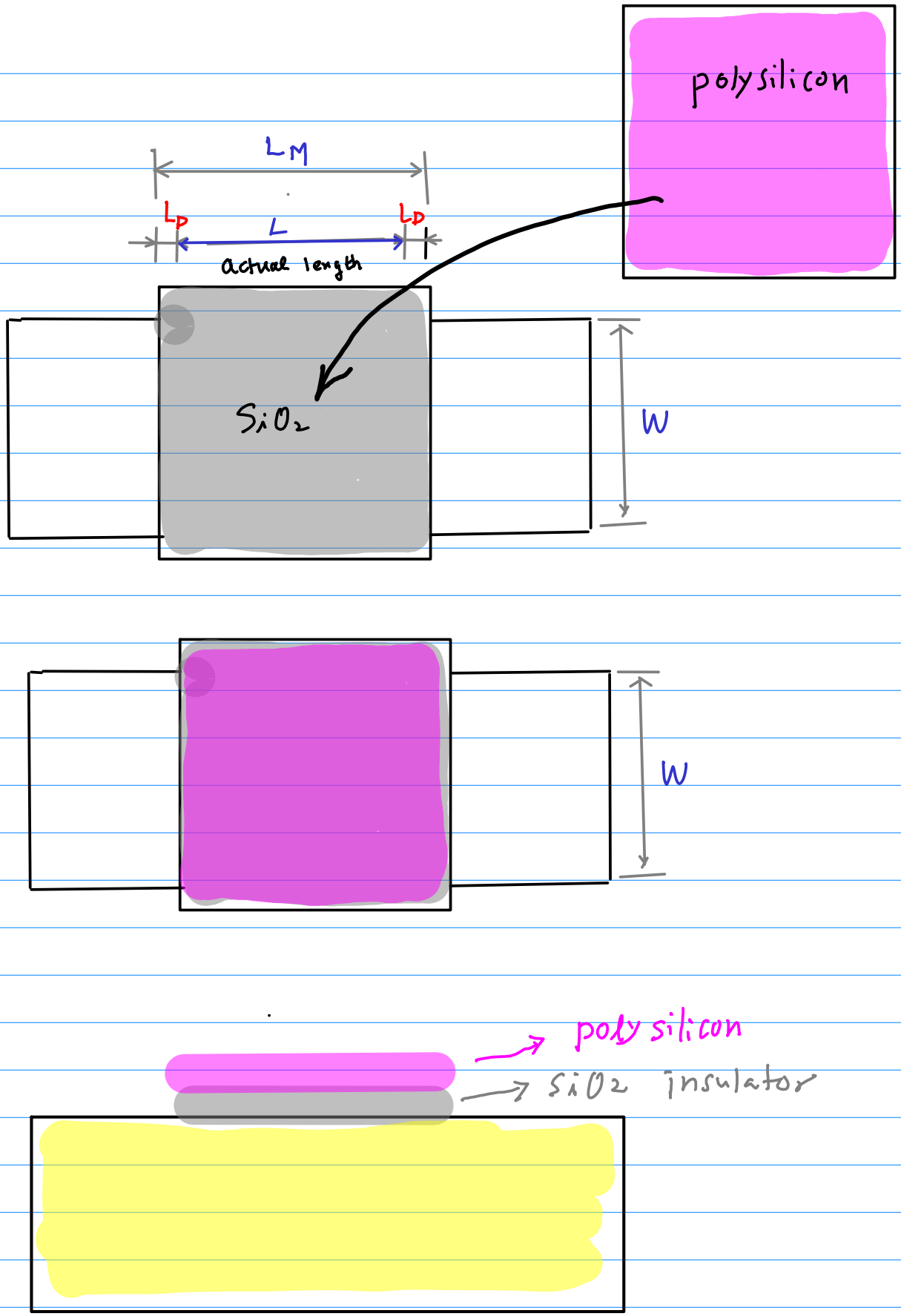
Channel Length

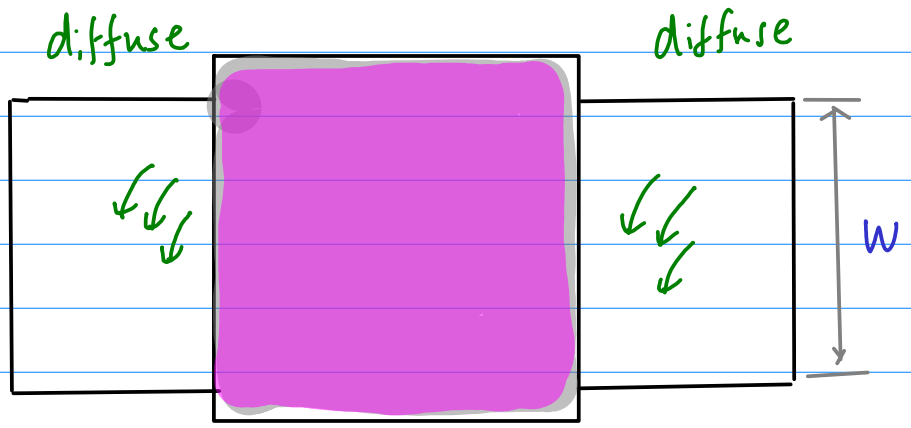


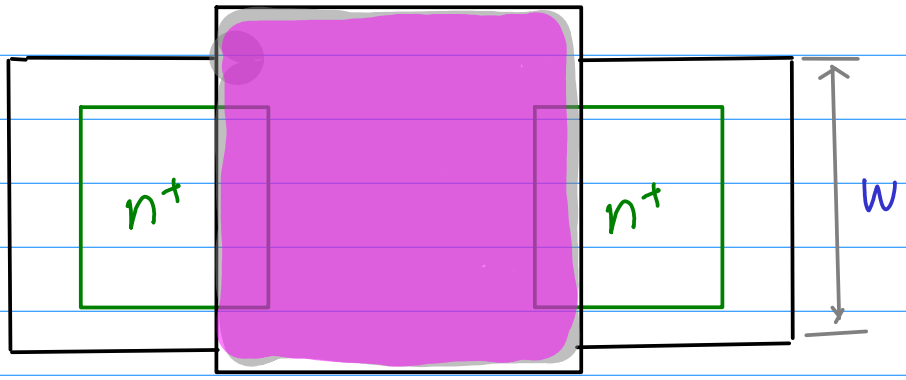
$$L = L_M - 2L_D$$

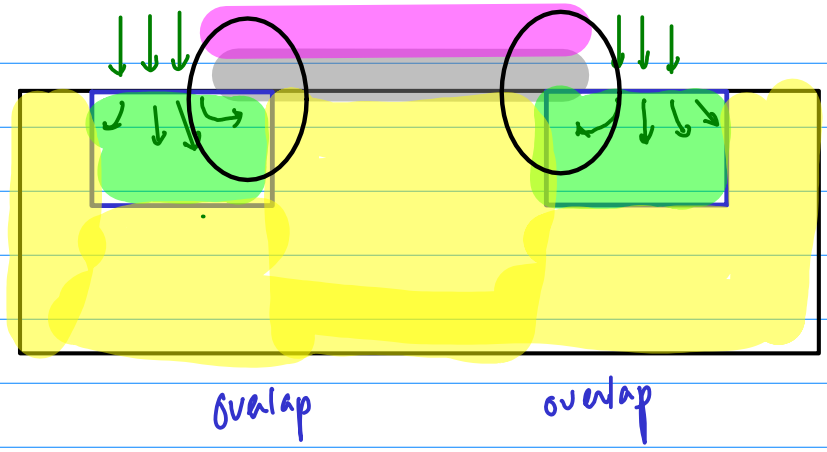
- L_M : Mask Length
- L : Channel Length.
- L_D : Overlapped Length

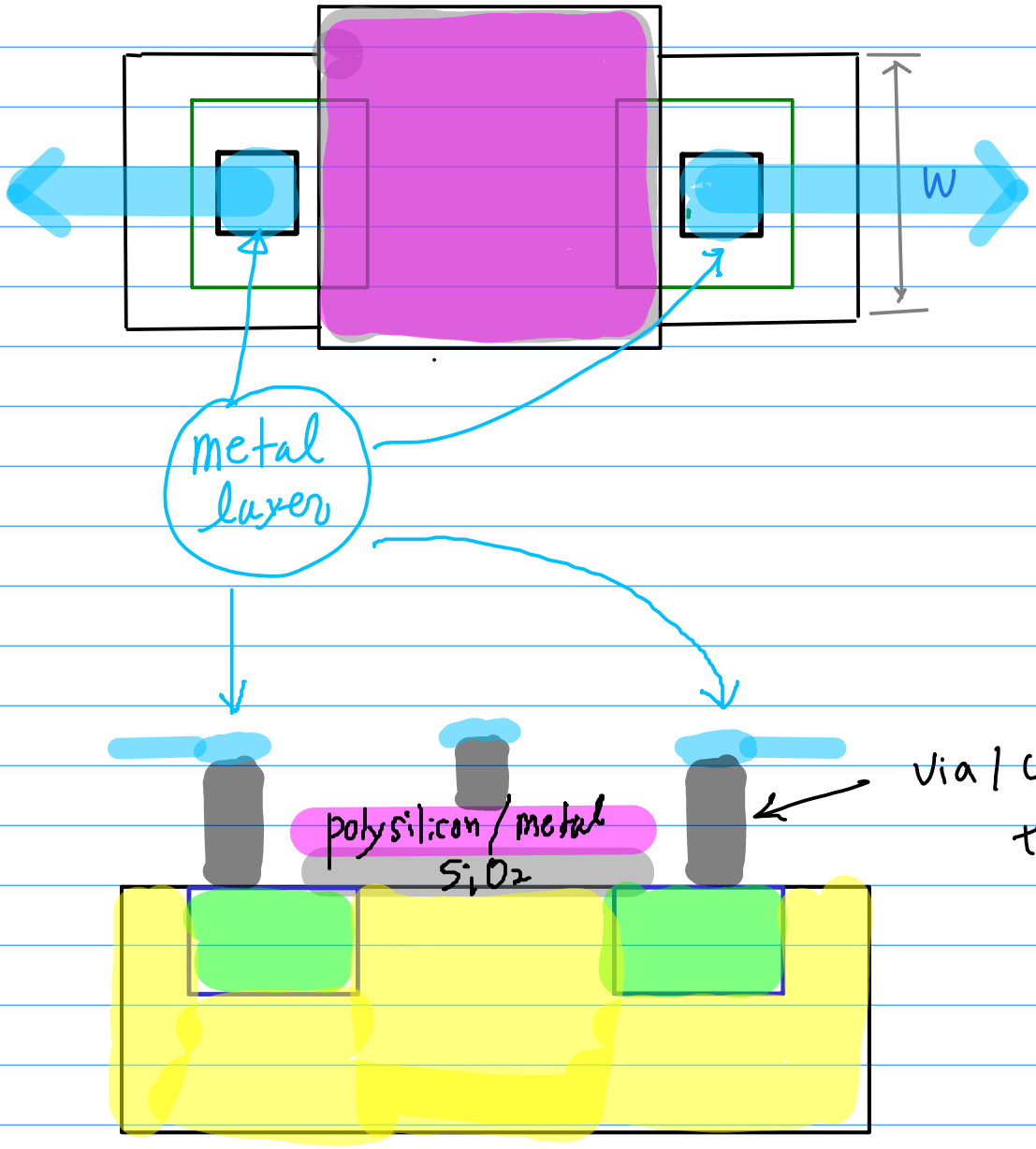


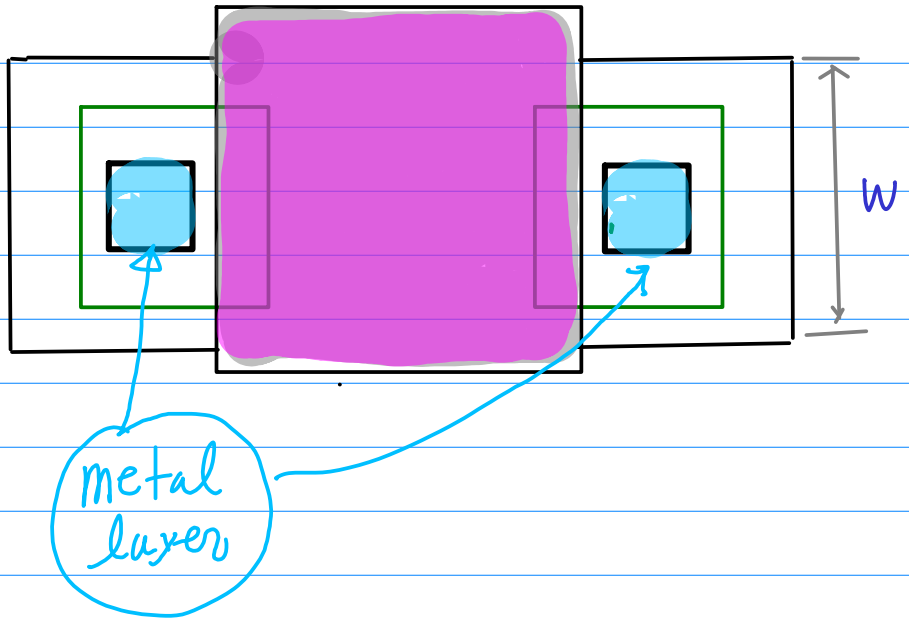

polysilicon
L_M
L_D
L_D
L
actual length
SiO_2
W
W
polysilicon
SiO_2 insulator


diffuse
diffuse
W

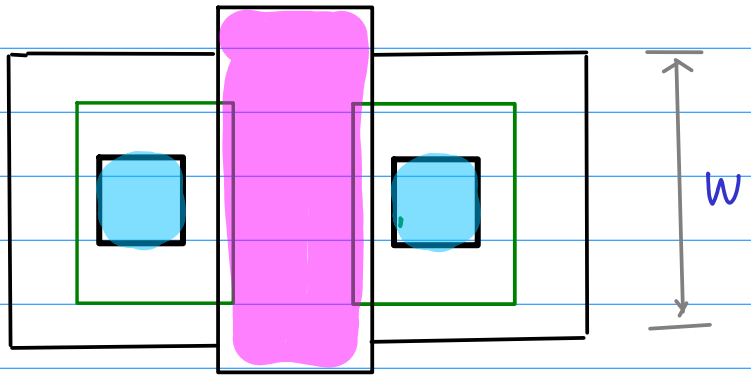

n+
n+
W


overlap
overlap


W
metal layer
polysilicon / metal
SiO_2
Via / contact
tungsten



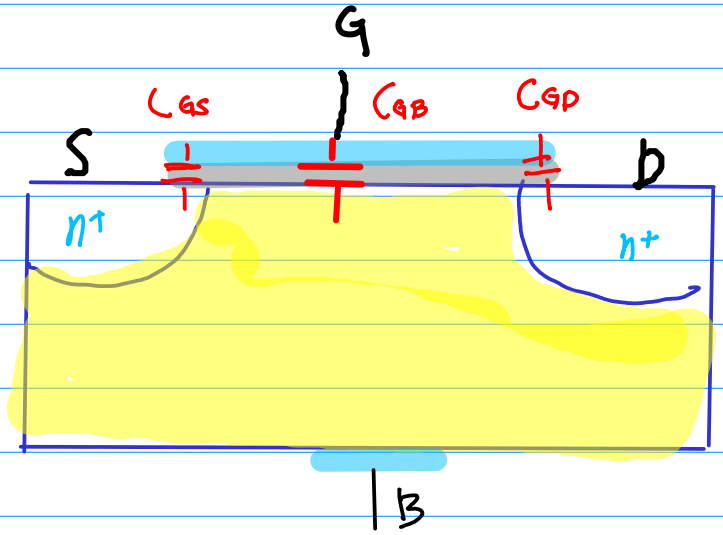
More actual Geometry

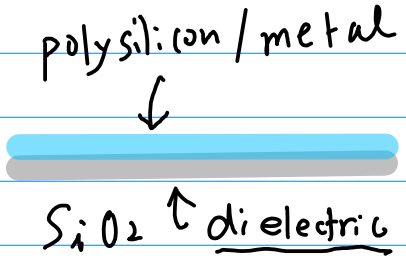


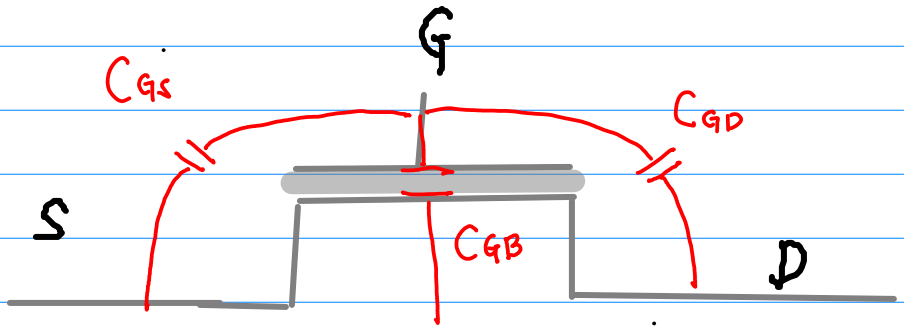
Short
channel

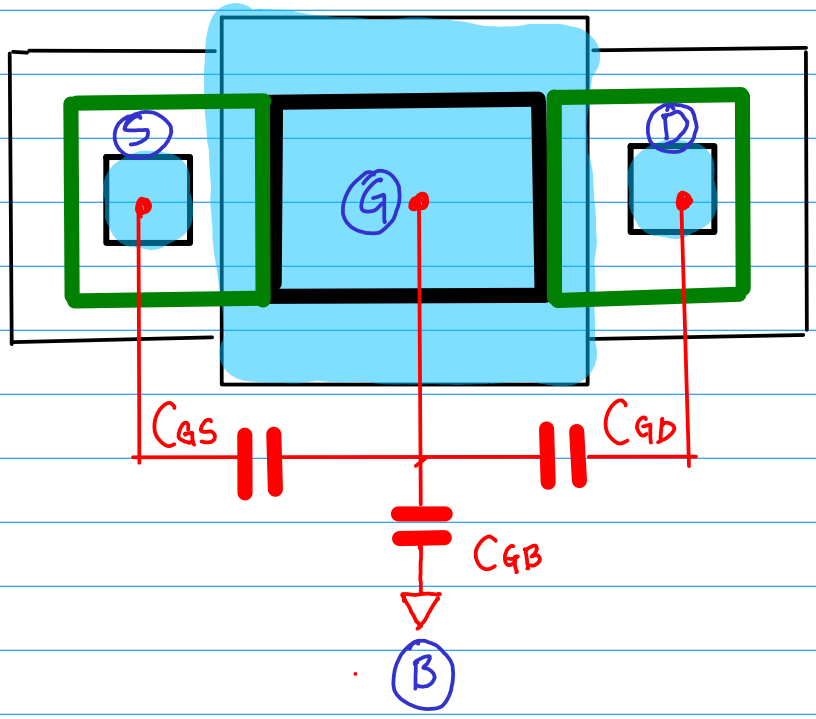
Oxide related Cap.

- Voltage dependent component









Oxide related Cap.

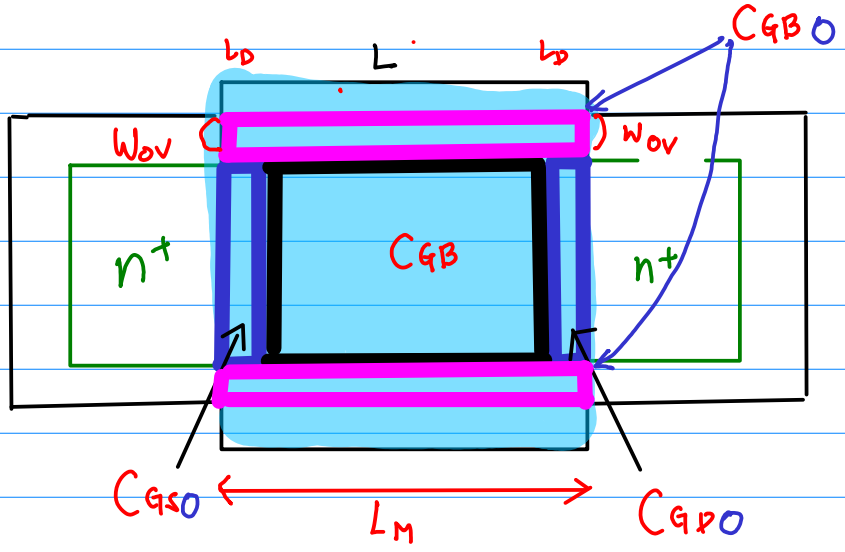
— Voltage independent component

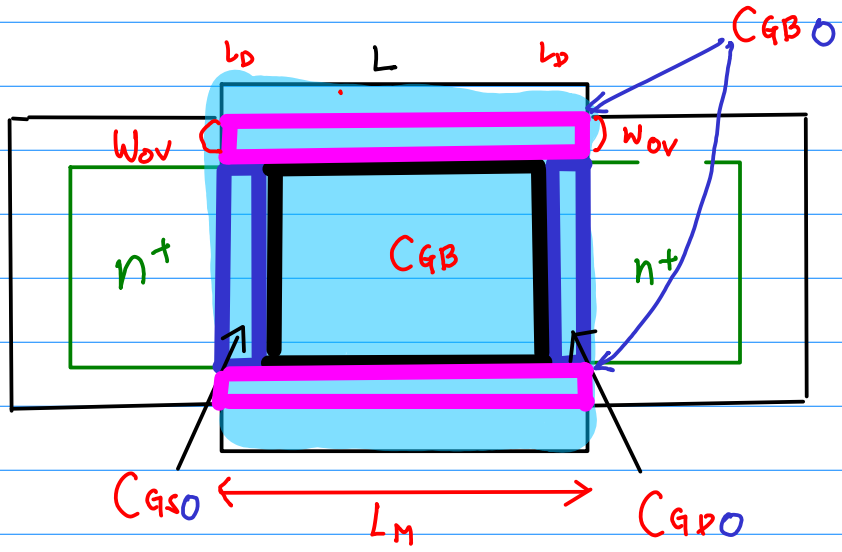
Overlap Capacitance

$$\left.\begin{aligned} C_{GSO} &= C_{ox} \cdot W \cdot L_D \\ C_{GDO} &= C_{ox} \cdot W \cdot L_D \\ C_{GBO} &= C_{ox} \cdot W_{ov} \cdot L_M \end{aligned}\right\} \text{voltage independent}$$

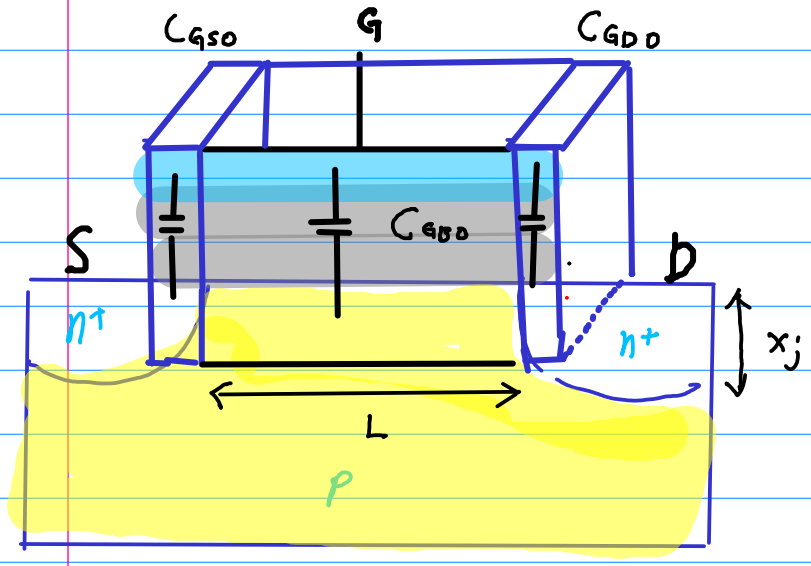
$$C_{GB} = C_{ox} \cdot W \cdot L \quad \} \text{ voltage dependent}$$

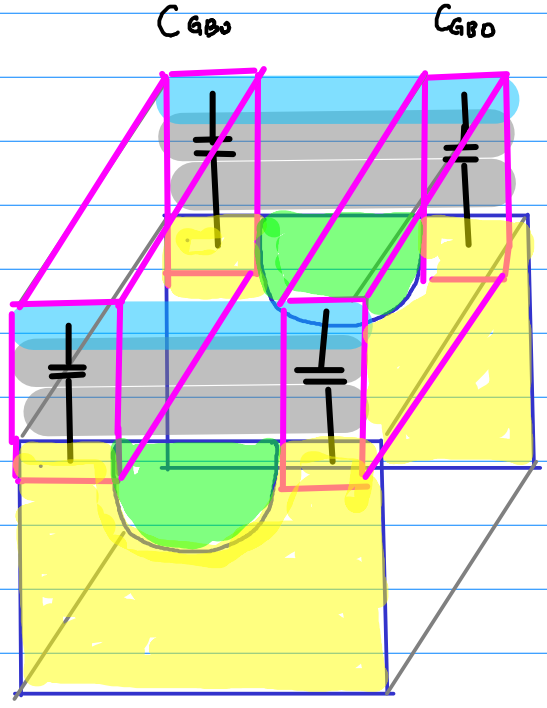
C_{GB} non zero only in CUT OFF mode





$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

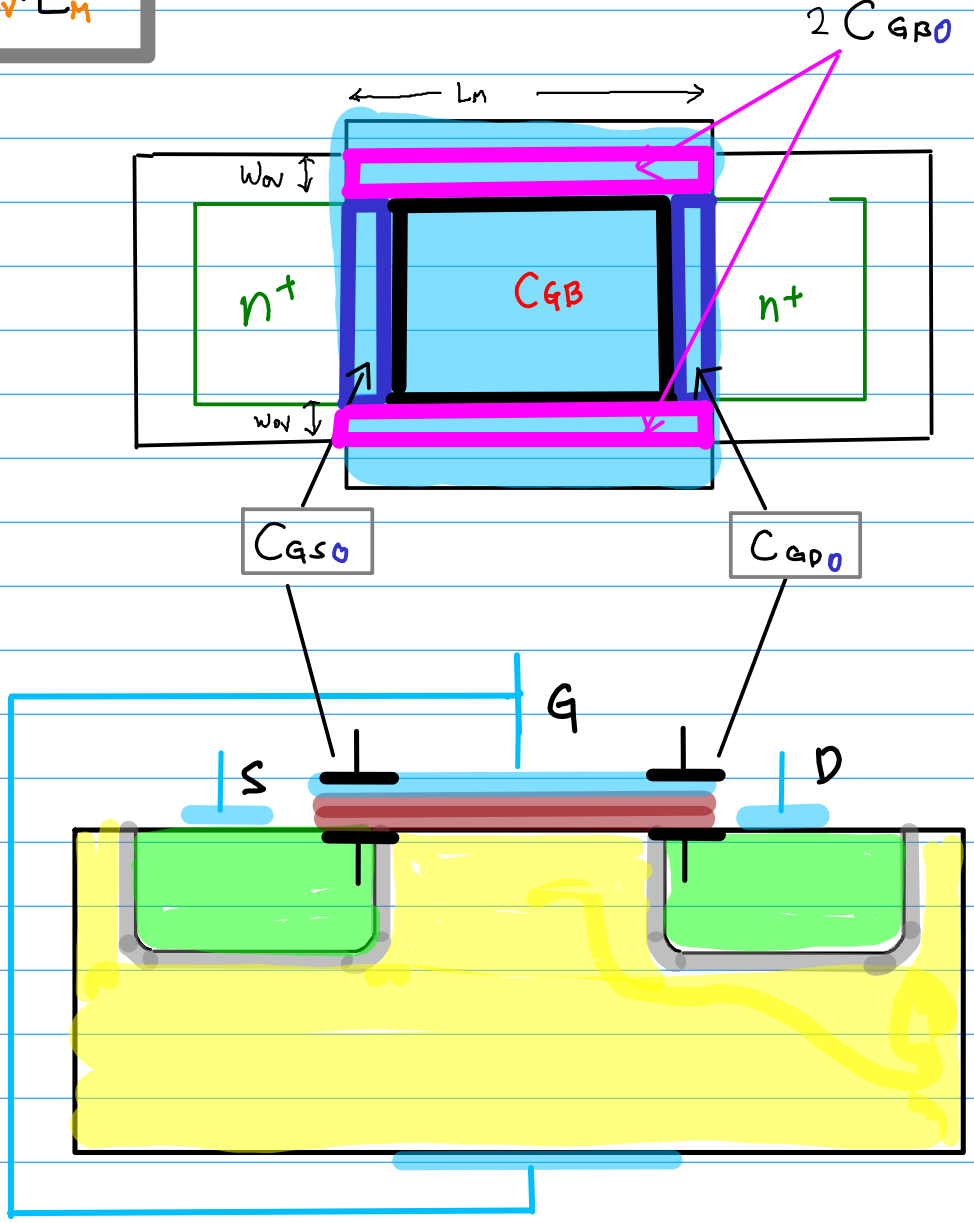




Overlap Capacitance

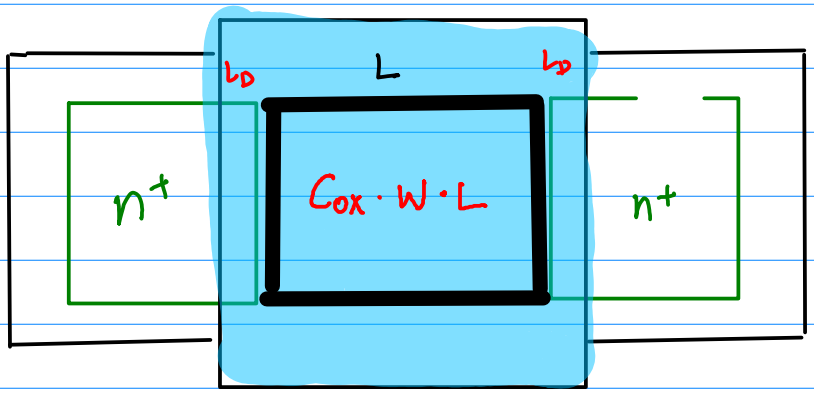
* voltage independent component
  - not related to inversion channel
  - constant under different operating mode
    cut off, linear, saturation

$$C_{GSO} = C_{ox} \cdot W \cdot L_D$$
$$C_{GDO} = C_{ox} \cdot W \cdot L_D$$
$$2C_{GBO} = 2C_{ox} \cdot W_{ov} \cdot L_M$$



Oxide related Cap.

— Voltage dependent component



Voltage dependent

① cut off

$$C_{GS} = 0$$

$$C_{GD} = 0$$

$$C_{GB} = C_{ox} \cdot W \cdot L$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

② Linear

$$C_{GS} = \frac{1}{2} C_{ox} \cdot W \cdot L$$

$$C_{GD} = \frac{1}{2} C_{ox} \cdot W \cdot L$$

$$C_{GB} = 0$$

③ Saturation

$$C_{GS} = \frac{2}{3} C_{ox} \cdot W \cdot L$$

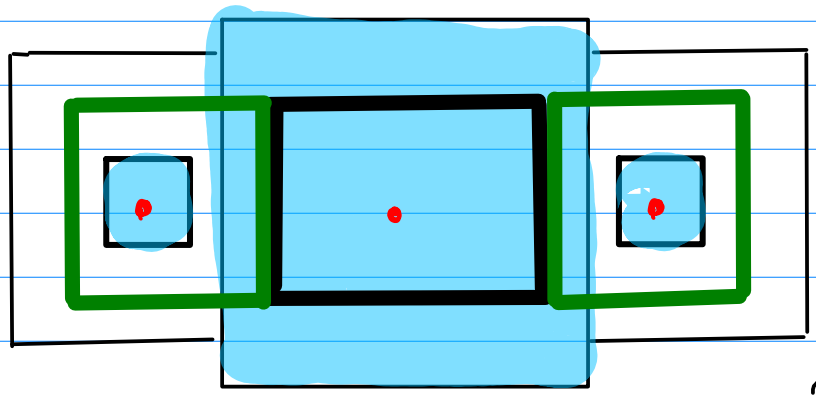
$$C_{GD} = 0$$

$$C_{GB} = 0$$

Oxide related Cap.

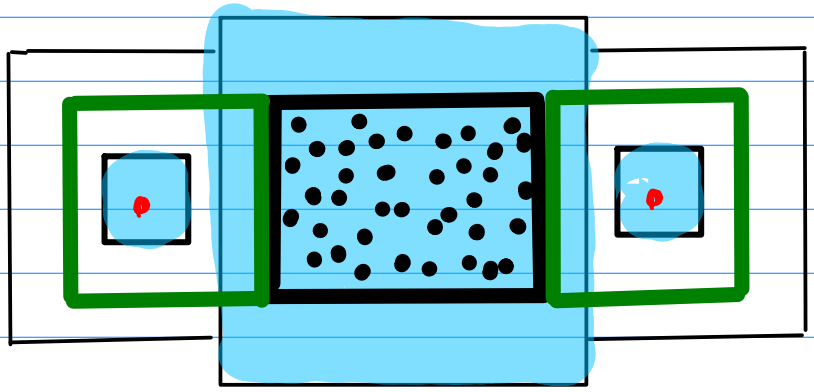
- Voltage dependent component

OFF



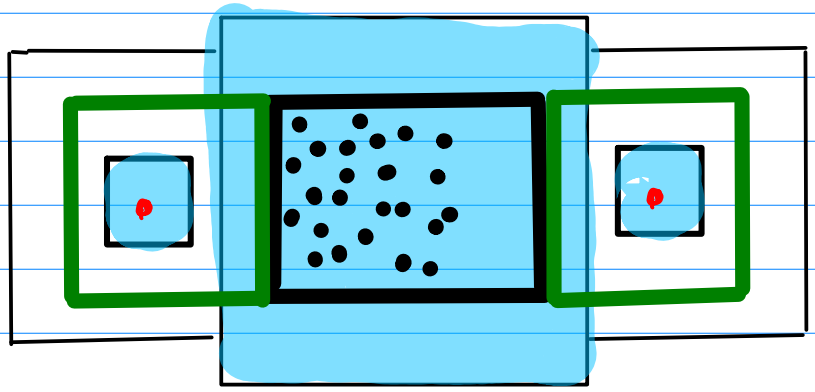
no channel

LIN



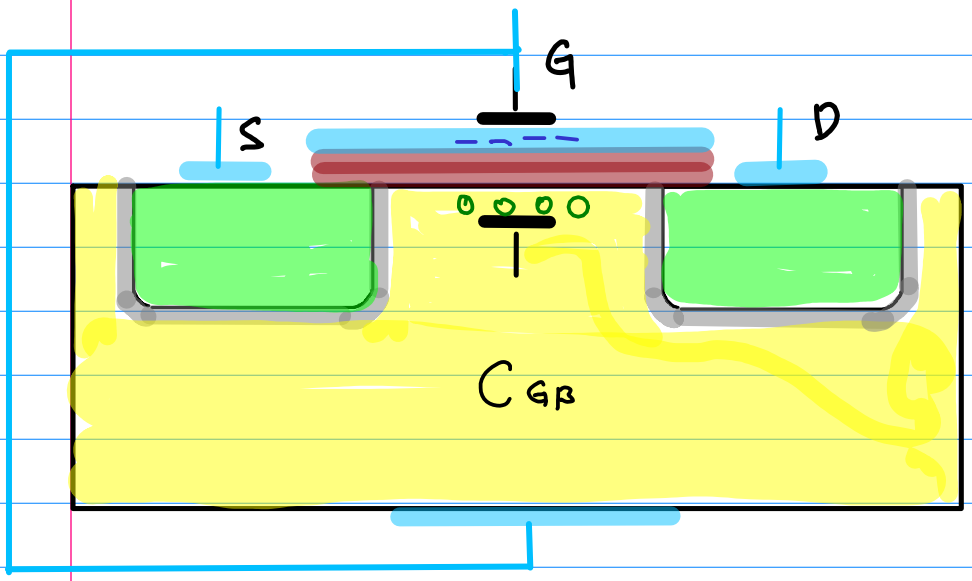
full channel

SAT



reduced channel

Oxide-related Capacitance – Cut Off



OFF

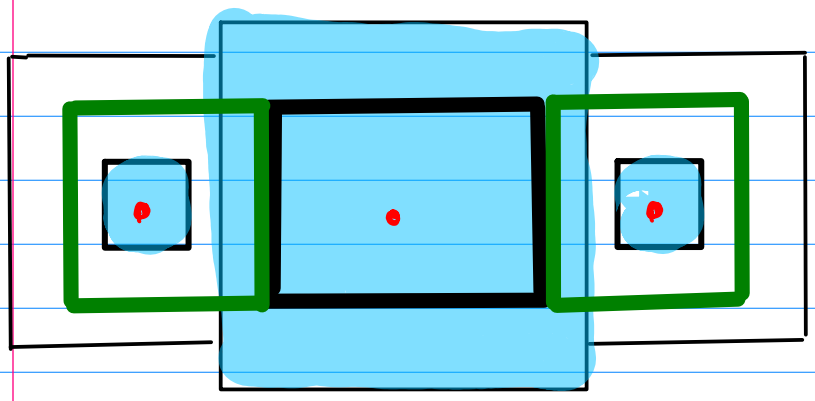
$V_{GS} < V_t$

* Voltage dependent component

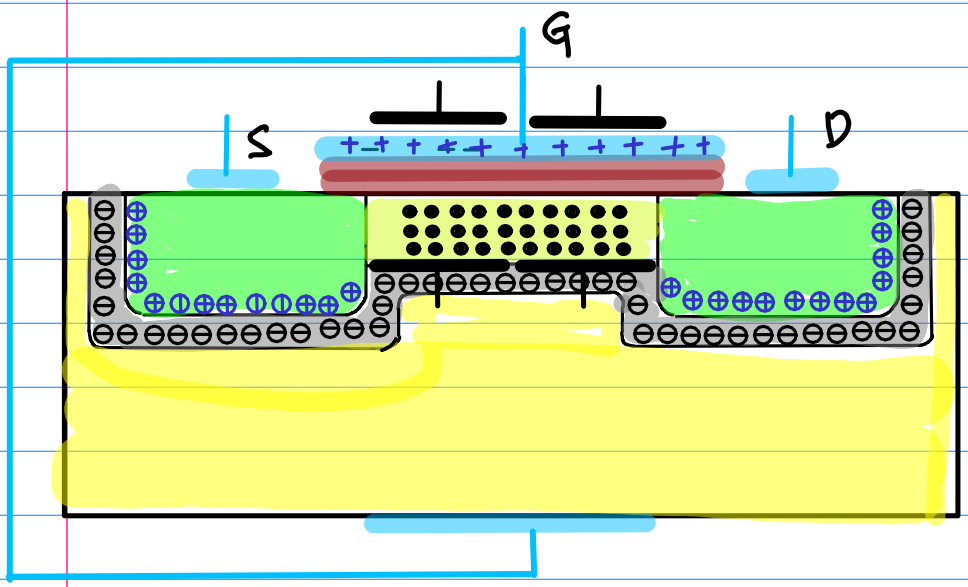
$C_{GS} = 0$

$C_{GD} = 0$

$C_{GB} = C_{ox} \cdot W \cdot L$



Oxide-related Capacitance – Linear



LIN

$V_t < V_{GS}$

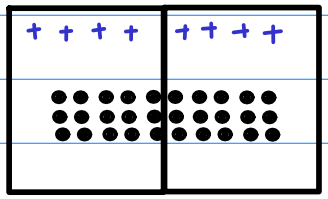
$V_{DS} < V_{GS} - V_t$

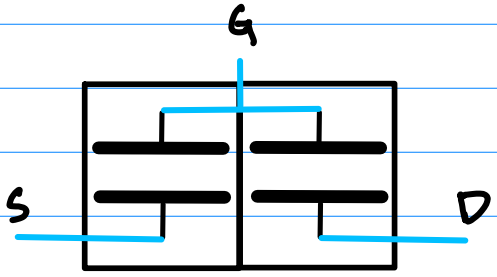
* Voltage dependent component

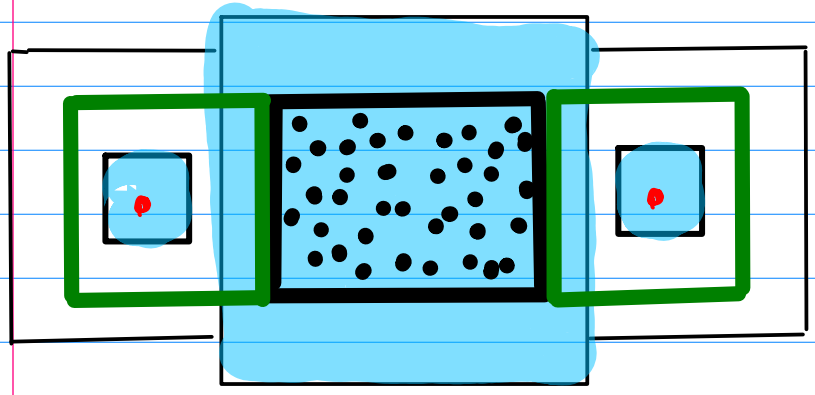
$$C_{GS} = \frac{1}{2} C_{ox} \cdot W \cdot L$$

$$C_{GD} = \frac{1}{2} C_{ox} \cdot W \cdot L$$

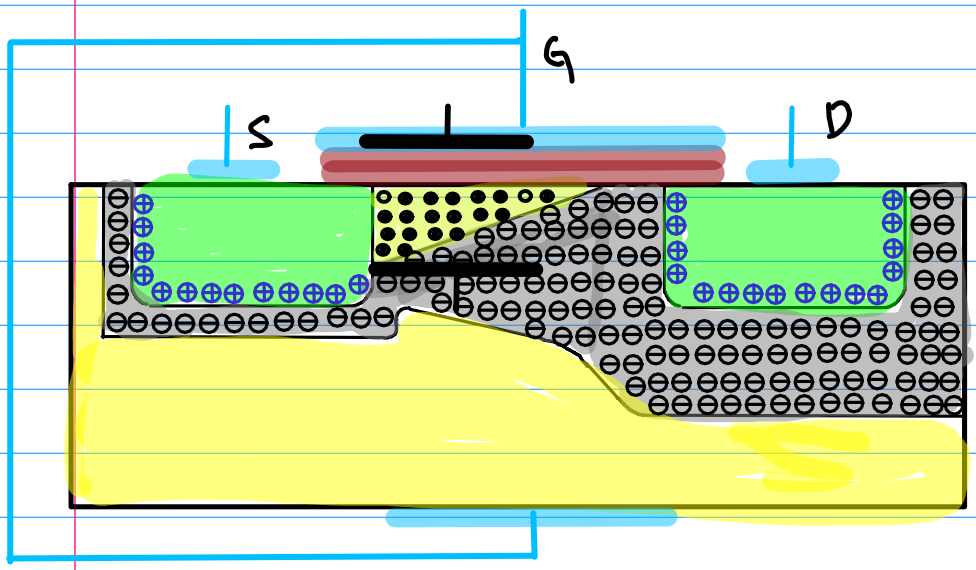
$$C_{GB} = 0$$







Oxide-related Capacitance – Saturation



SAT

$V_t < V_{GS}$

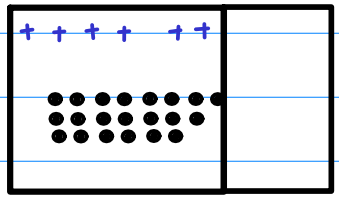
$V_{DS} > V_{GS} - V_t$

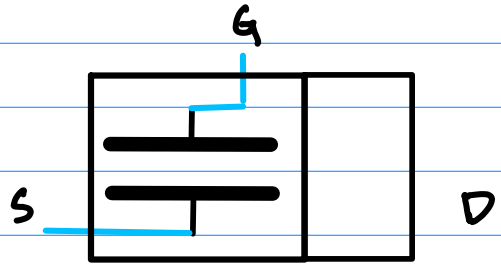
* Voltage dependent component

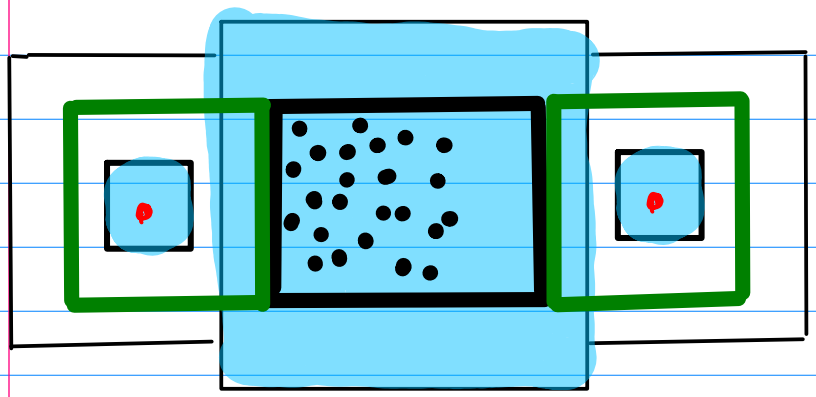
$$C_{GS} = \frac{2}{3} C_{ox} \cdot W \cdot L$$

$$C_{GD} = 0$$

$$C_{GB} = 0$$







① Cut off

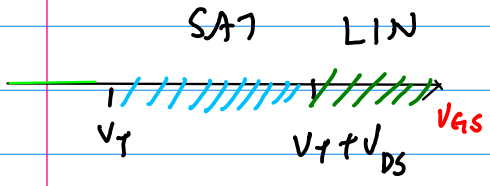
$C_{GS} = 0$	
$C_{GD} = 0$	
$C_{GB} = C_{ox} \cdot W \cdot L$	

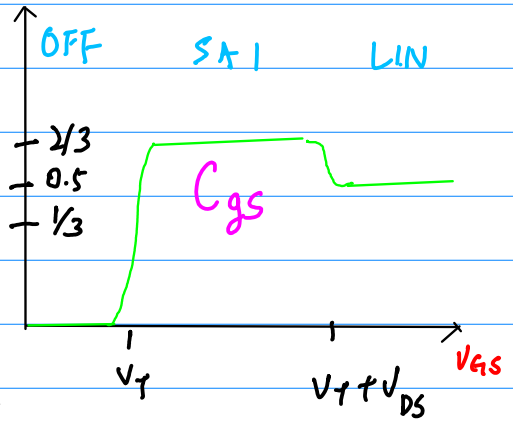
② Linear

$C_{GS} = \frac{1}{2} C_{ox} \cdot W \cdot L$	
$C_{GD} = \frac{1}{2} C_{ox} \cdot W \cdot L$	
$C_{GB} = 0$	

③ saturation

$C_{GS} = \frac{2}{3} C_{ox} \cdot W \cdot L$	
$C_{GD} = 0$	
$C_{GB} = 0$	





$V_T < V_{GS} < V_T + V_{DS}$

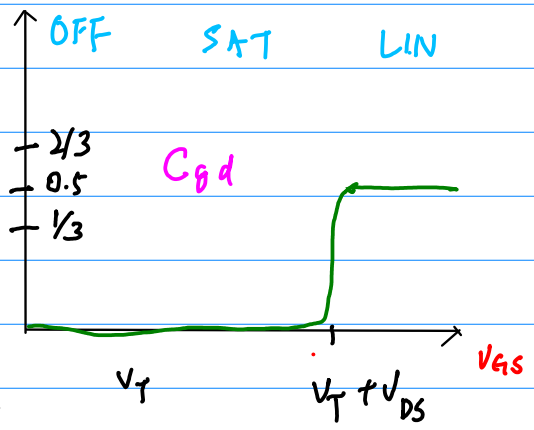
$V_{DS} > V_{GS} - V_T$

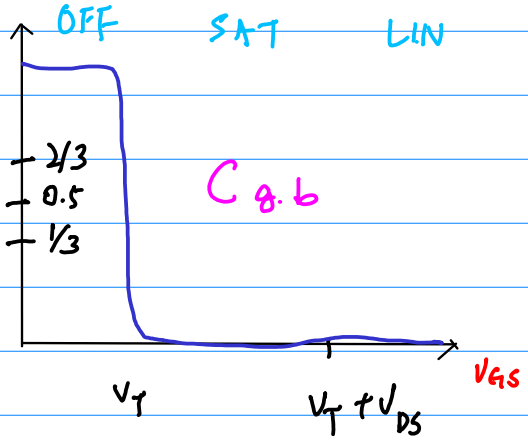
SAT

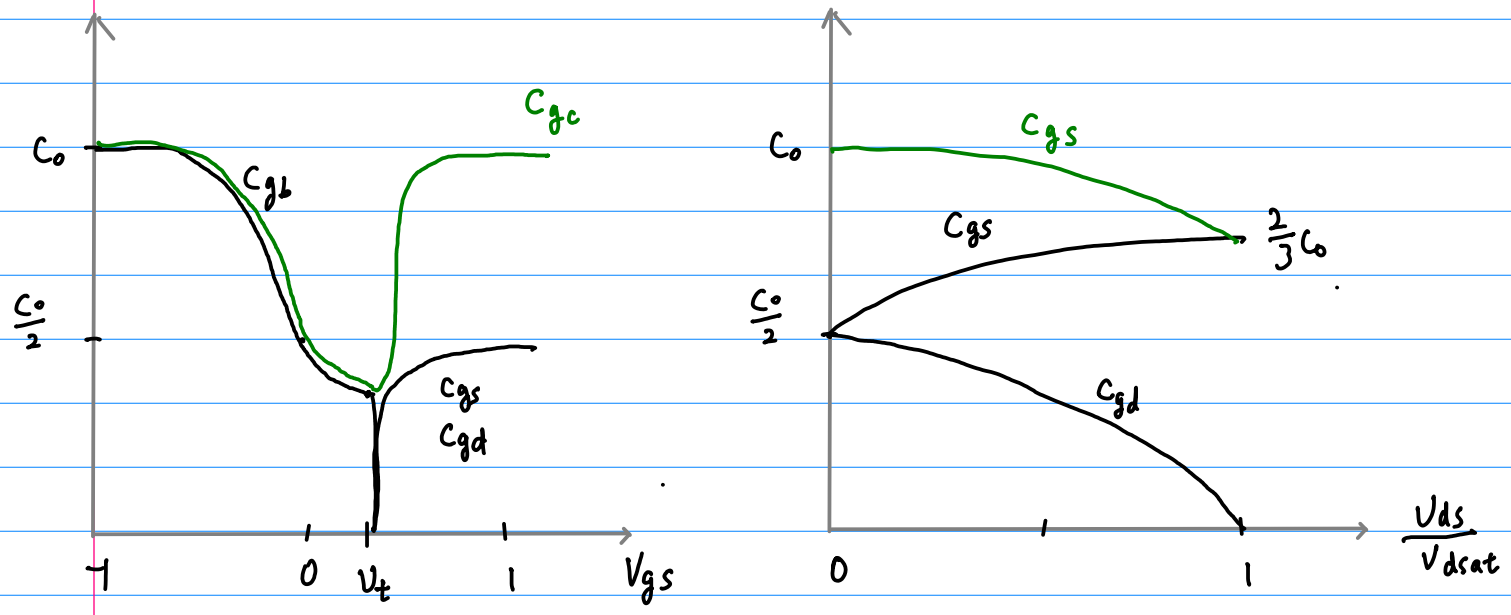
$V_T + V_{DS} < V_{GS}$

$V_{DS} < V_{GS} - V_T$

LIN







① OFF $V_{gs} < V_t$

no inversion channel

Gate-Body Capacitance C_{gb}

inc V_{gs} $(0 < V_{gs} < V_t)$

: depletion region ↑ d ↑ C_{gb} ↓

② LIN $V_{gs} > V_t$ $V_{ds} < V_{gs} - V_t$

inversion channel — connected to S & D

$C_{gs} = C_o/2 = C_{gd}$

V_{ds} ↑ $C_{gs} > C_o/2 > C_{gd}$ $Q_{gs} \leftarrow Q_{gd}$

③ SAT $V_{gs} > V_t$ $V_{ds} > V_{gs} - V_t$

pinch off the channel

only $C_{gs} = \frac{2}{3} C_o$

* Ox - Related Capacitance

① Voltage dependent component

	① Cut off	② Linear	③ saturation
GS	$C_{GS} = 0$	$C_{GS} = \frac{1}{2} C_{ox} \cdot W \cdot L$	$C_{GS} = \frac{2}{3} C_{ox} \cdot W \cdot L$
GD	$C_{GD} = 0$	$C_{GD} = \frac{1}{2} C_{ox} \cdot W \cdot L$	$C_{GD} = 0$
GB	$C_{GB} = C_{ox} \cdot W \cdot L$	$C_{GB} = 0$	$C_{GB} = 0$

② Voltage independent component (Overlap Capacitance)

	① Cut off	② Linear	③ saturation
GSO	$C_{GSO} = C_{ox} \cdot W \cdot L_D$		
GDO	$C_{GDO} = C_{ox} \cdot W \cdot L_D$		
GBO	$2 \cdot C_{GBO} = 2 C_{ox} \cdot W_{ov} \cdot L_M$		

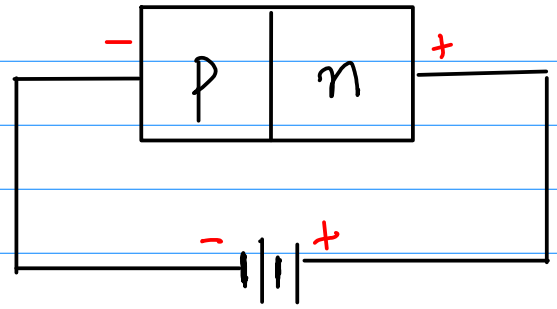
* Total Capacitance & Gate Capacitance

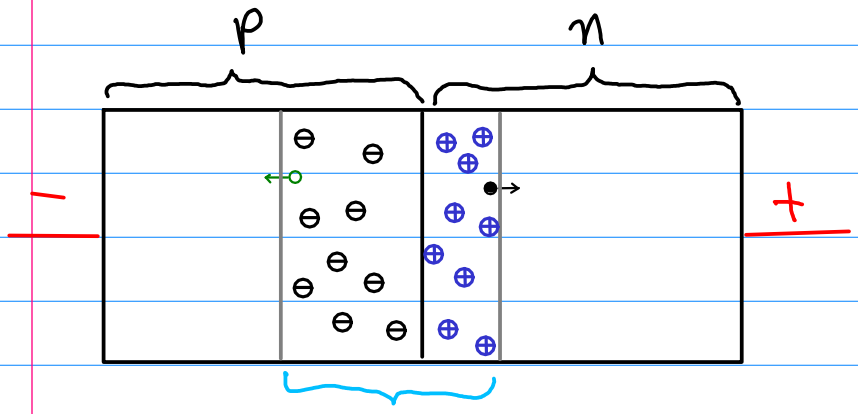
	① Cut off	② Linear	③ saturation
Total C_{GS}	$0 + C_{GSO}$	$\frac{1}{2} C_{ox} \cdot W \cdot L + C_{GSO}$	$\frac{2}{3} C_{ox} \cdot W \cdot L + C_{GSO}$
Total C_{GD}	$0 + C_{GDO}$	$\frac{1}{2} C_{ox} \cdot W \cdot L + C_{GDO}$	$0 + C_{GDO}$
Total C_{GB}	$C_{ox} \cdot W \cdot L + 2C_{GBO}$	$0 + 2 \cdot C_{GBO}$	$0 + 2 \cdot C_{GBO}$

C_g

① Cut off	② Linear	③ saturation
$C_{ox} \cdot W \cdot L$	$C_{ox} \cdot W \cdot L$	$\frac{2}{3} C_{ox} \cdot W \cdot L$
$+ C_{GSO}$	$+ C_{GSO}$	$+ C_{GSO}$
$+ C_{GDO}$	$+ C_{GDO}$	$+ C_{GDO}$
$+ 2 C_{GBO}$	$+ 2 C_{GBO}$	$+ 2 C_{GBO}$

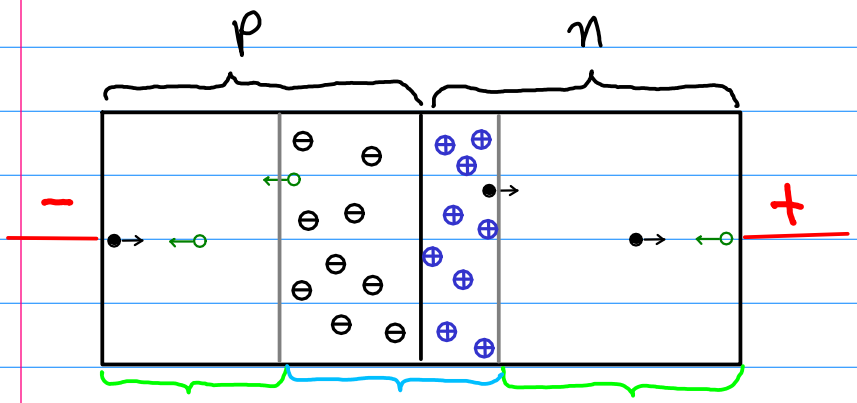
P-N Junction Capacitance

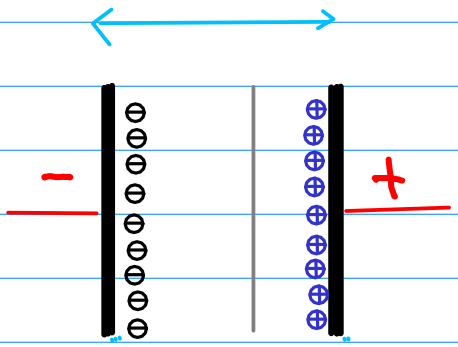


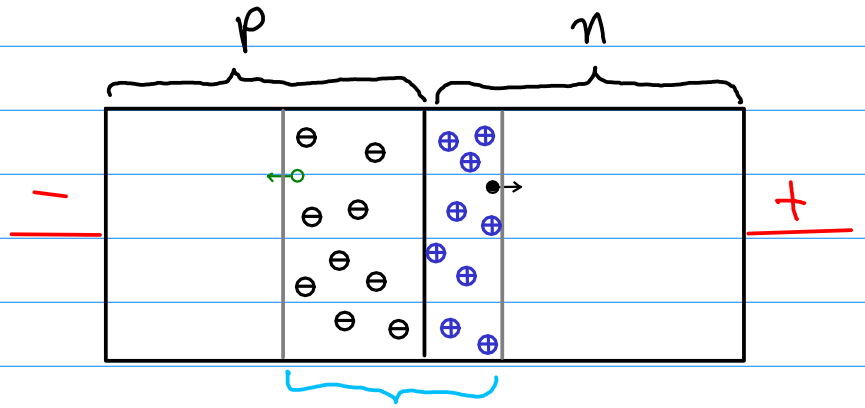


reverse bias

increasing reverse bias
increasing depletion region



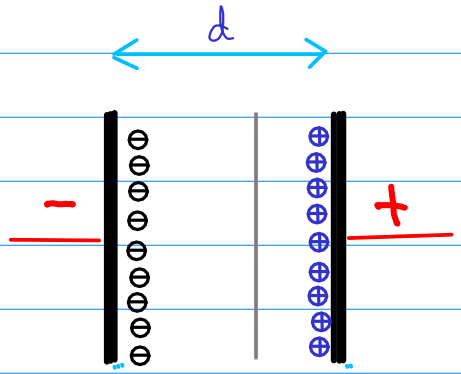




reverse bias

depletion region

acts as dielectric

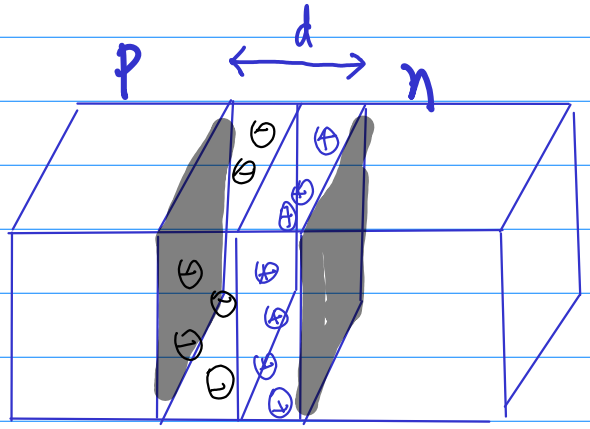


reverse bias ↑ (d) ↑ C_d ↓

$$C_d = \frac{\varepsilon_0 \varepsilon_s S}{d}$$

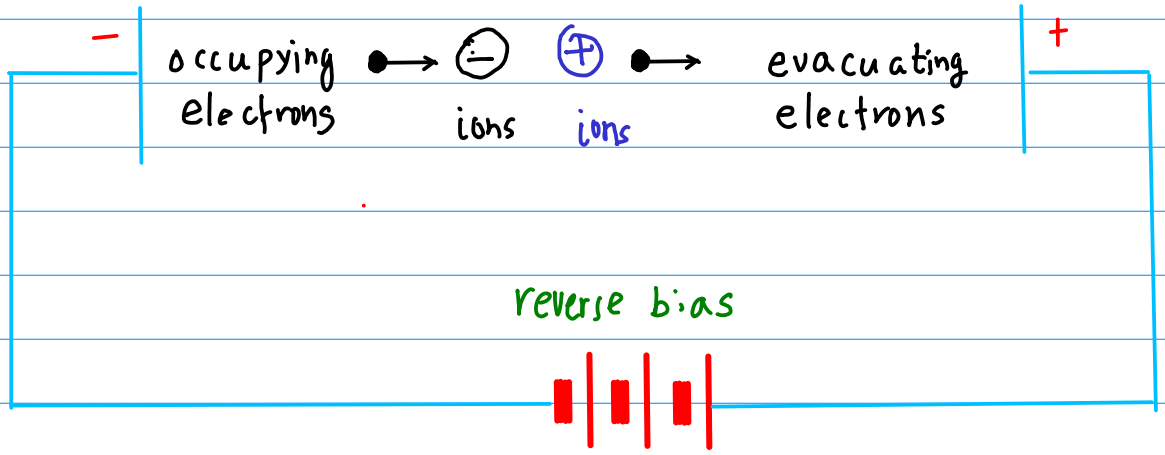
S: cross section area

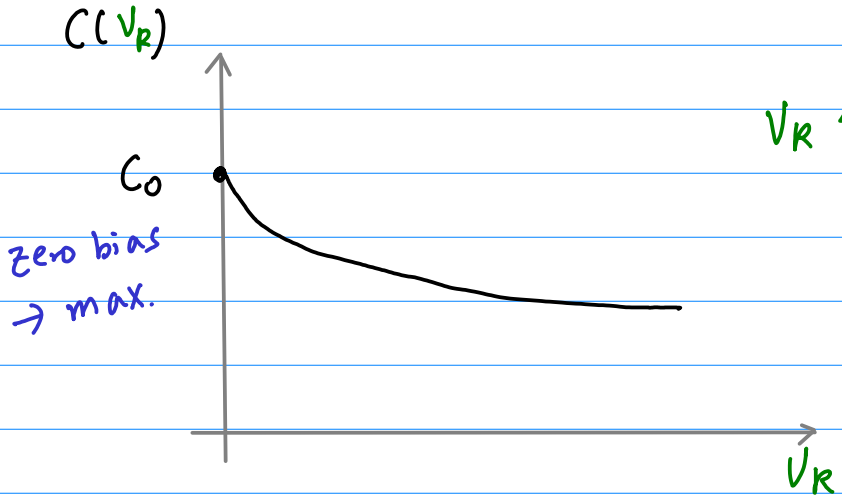
d: distance



Space charge

fixed, immobile





$V_R \uparrow \quad d \uparrow \quad C(V_R) \downarrow$

$$C_j = \frac{dQ}{dV}$$

incremental charge-storage capacitance

$$C_j = \frac{dq}{dv}$$ incremental charg-storage capacitance

defined as a small signal quantity

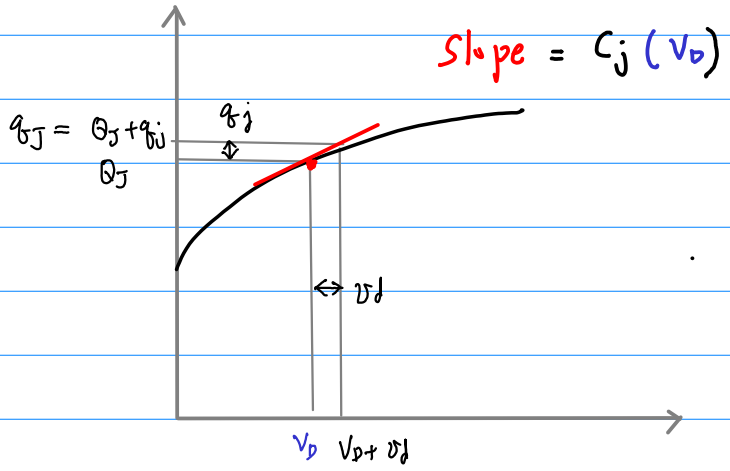
$$q_J = \boxed{Q_J} + \boxed{q_j}$$

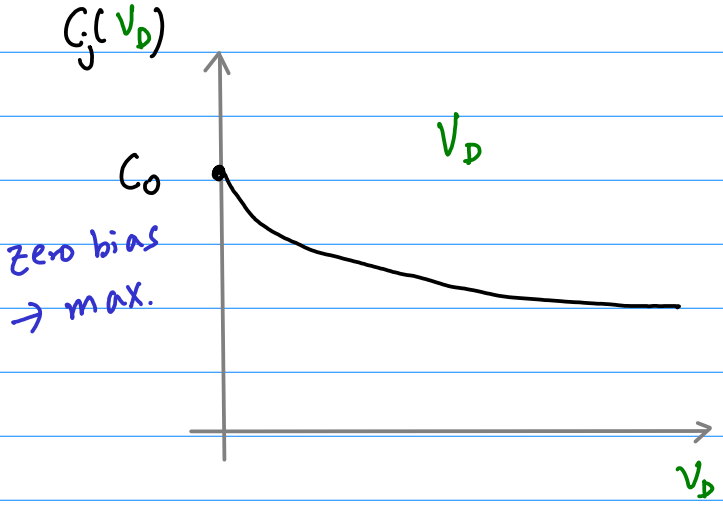
$$v_D = \boxed{V_D} + \boxed{v_d}$$

DC voltage

small-signal voltage

junction capacitance $$C_j = \frac{q_j}{v_d} = \frac{\Delta q_J}{\Delta v_D}$$





V_D : reverse bias

think flipped graph

$-V_D$

Junction Capacitance

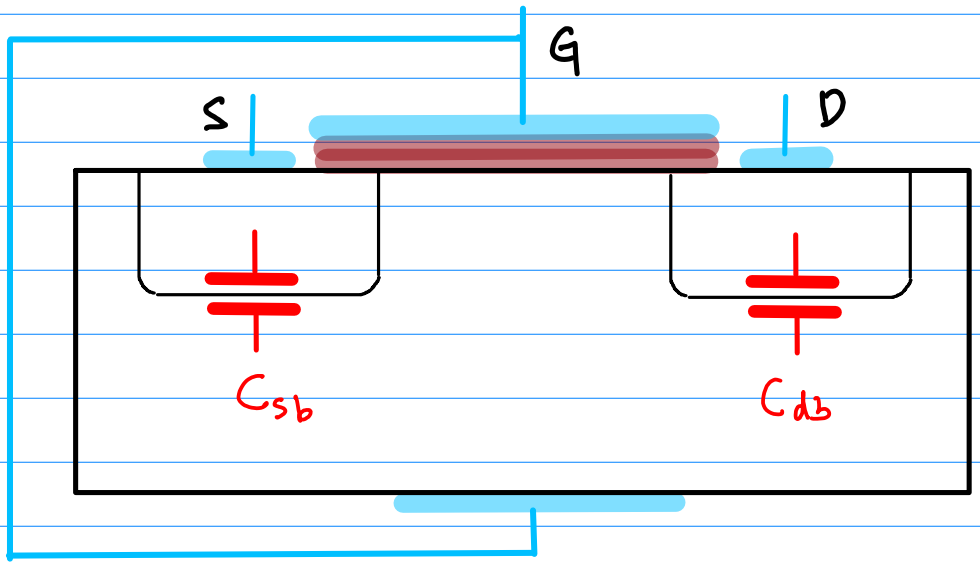
- Junction → location

  (n+) diffusion area — S & D of nMOS
  (p+) diffusion area — S & D of pMOS

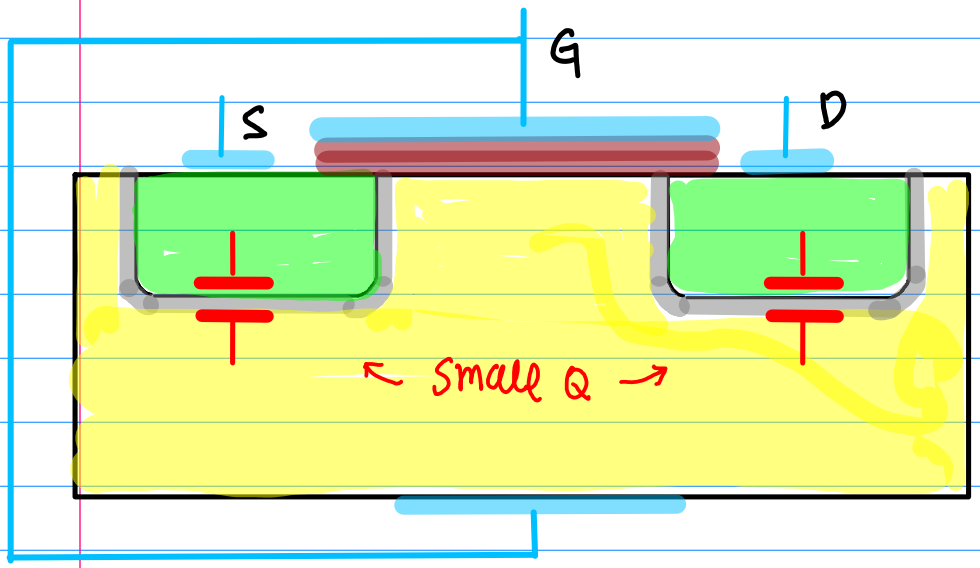
- Junction → reverse biased under normal operating conditions (OFF, LIN, SAT)

depletion capacitance — function (reverse bias voltage)

space charge

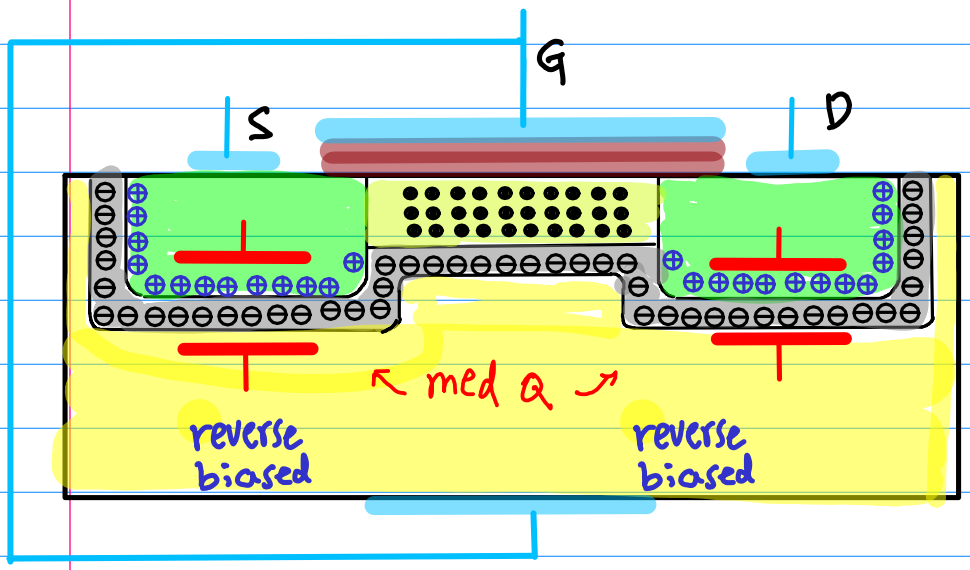


Junction Capacitance



OFF

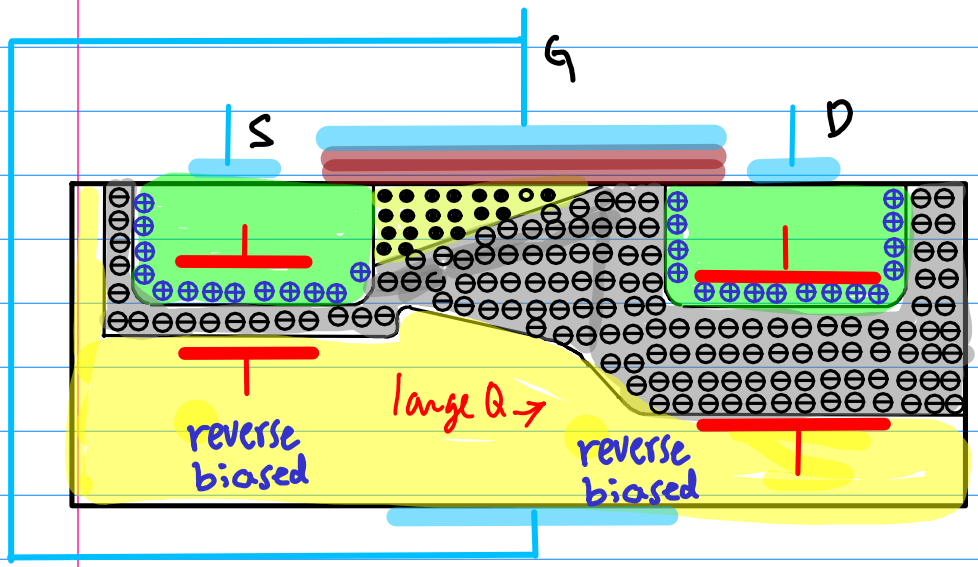
$V_{GS} < V_t$



LIN

$V_t < V_{GS}$

$V_{DS} < V_{GS} - V_t$

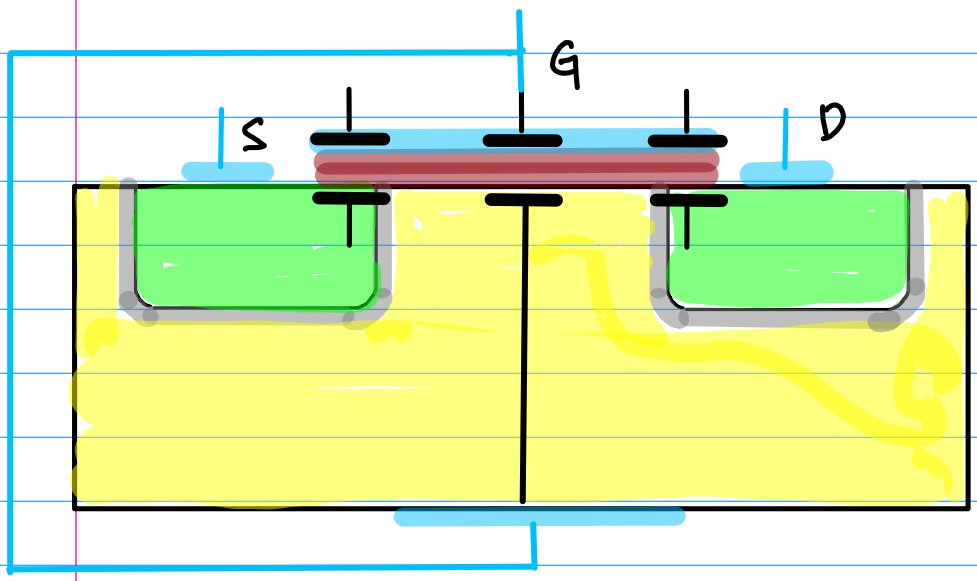


SAT

$V_t < V_{GS}$

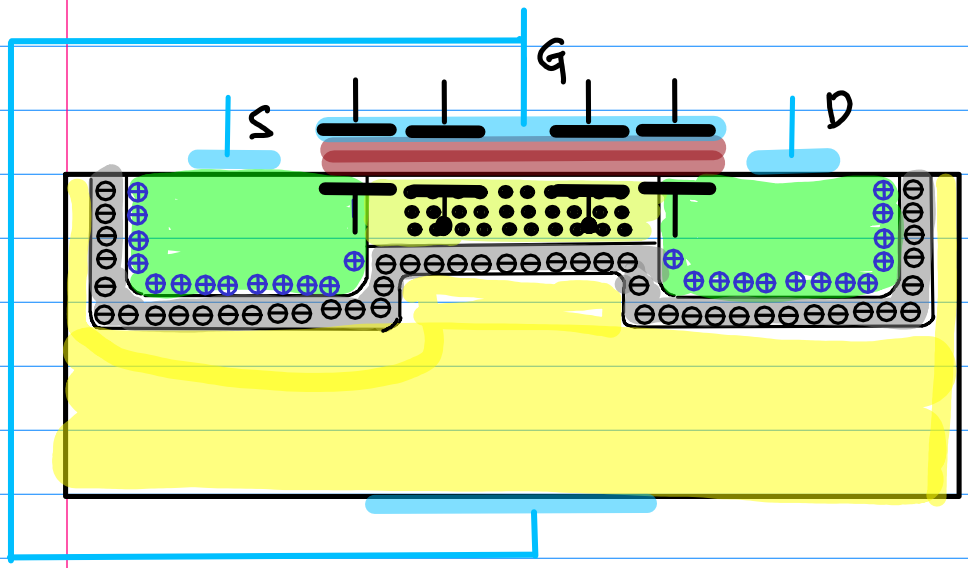
$V_{DS} > V_{GS} - V_t$

Oxide-related Capacitance



OFF

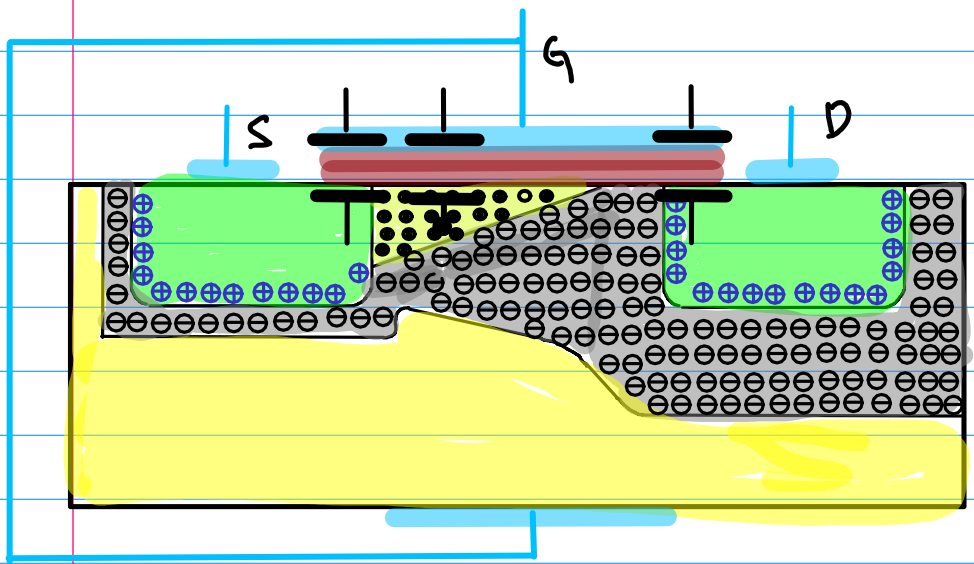
$V_{GS} < V_t$



LIN

$V_t < V_{GS}$

$V_{DS} < V_{GS} - V_t$



SAT

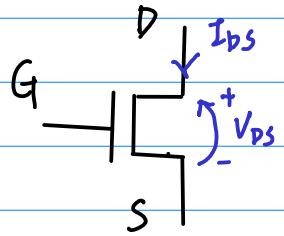
$V_t < V_{GS}$

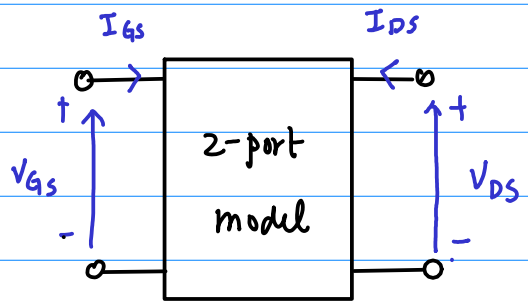
$V_{DS} > V_{GS} - V_t$

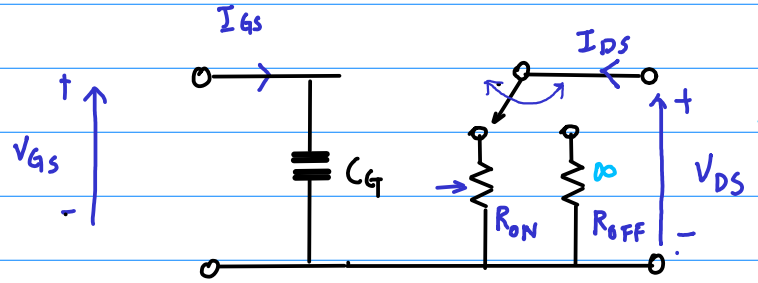
Simple nMOS Modelings for hand calculations

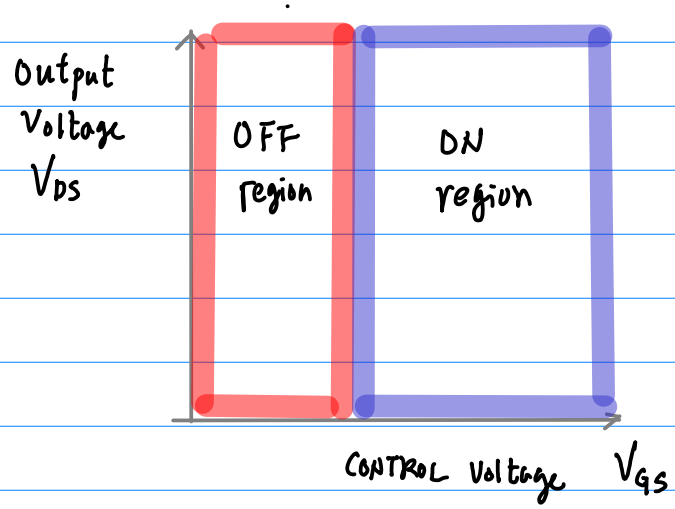
Chalmers.se Kjell Jeppson

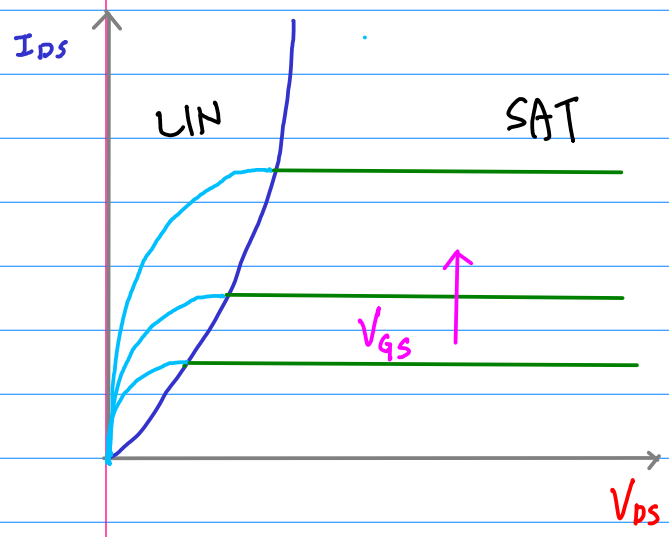
Integrated Circuit Design

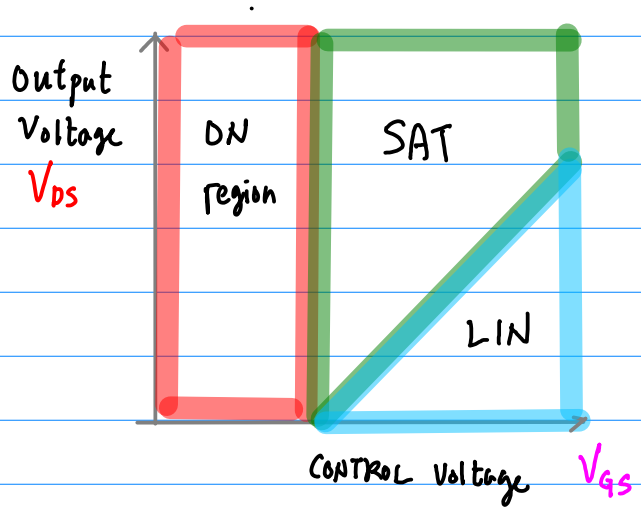


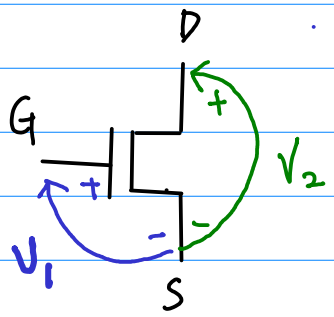


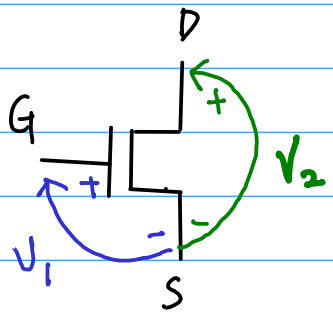












$V_1 - V_t > V_2$

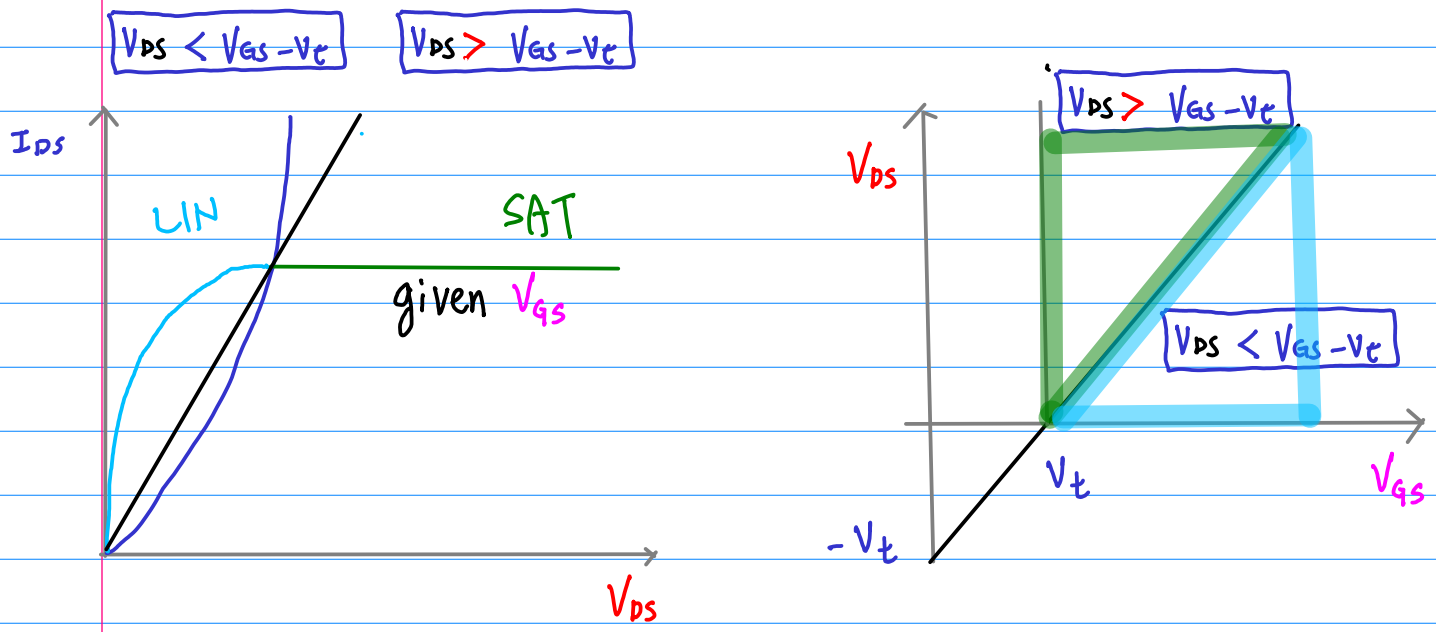
LIN

$I_{DS} \propto V_{DS}$

$V_1 - V_t < V_2$

SAT

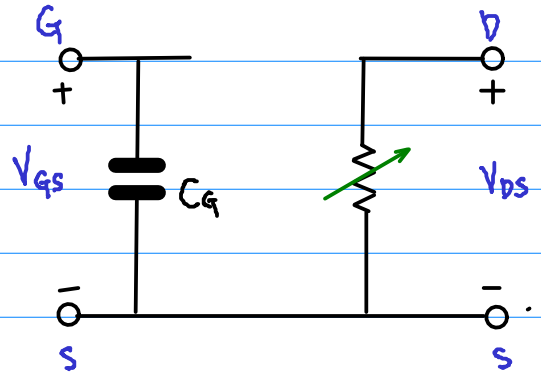
$I_{DS} = I_{SAT}$



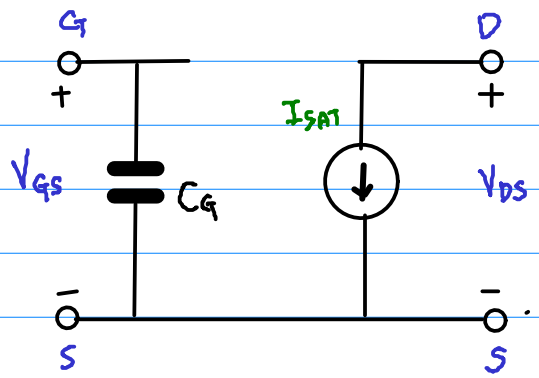
- $V_{GS} < V_t$ • Cut off
- $V_{GS} > V_t$
  - $V_{GD} > V_t$ = $V_{DS} < V_{GS} - V_t$
    • Linear (S-side channel, D-side Channel)
  - $V_{GD} < V_t$ = $V_{DS} > V_{GS} - V_t$
    • Saturation (S-side channel, ~~D-side channel~~)

$C_G = WL C_{ox}$

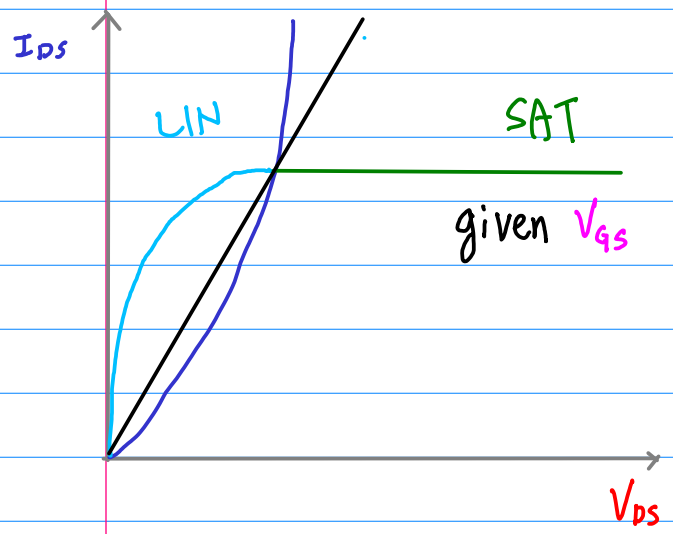
LIN $V_{DS} < V_{DSAT}$

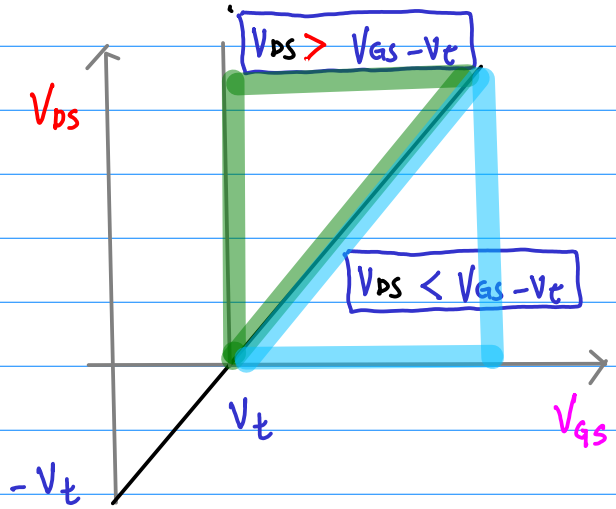


SAT $V_{DS} > V_{DSAT}$



$V_{DS} < V_{GS} - V_t$ $V_{DS} > V_{GS} - V_t$

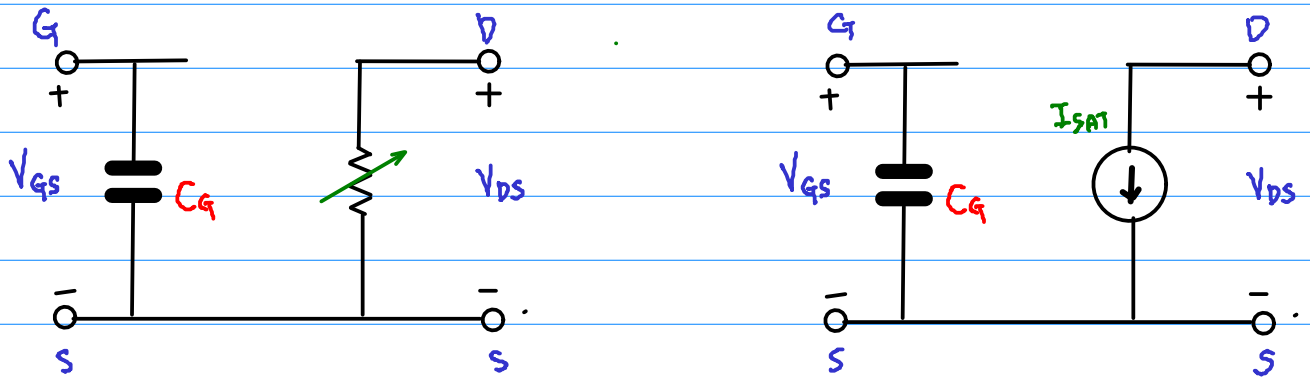




Simple Models

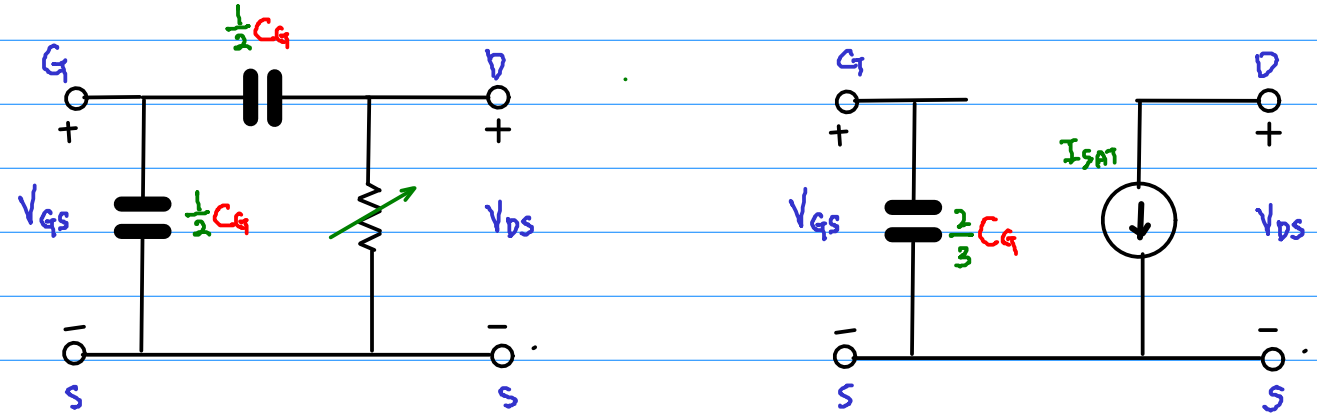
(I)

LIN $V_{DS} < V_{DSAT}$ $C_G = WL C_{ox}$ SAT $V_{DS} > V_{DSAT}$



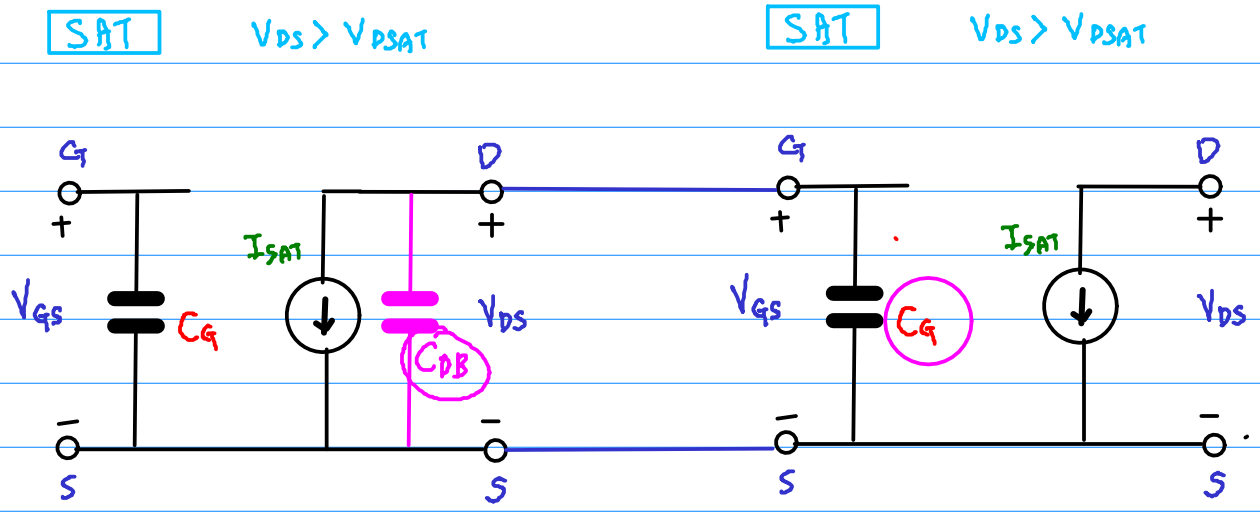
(II)

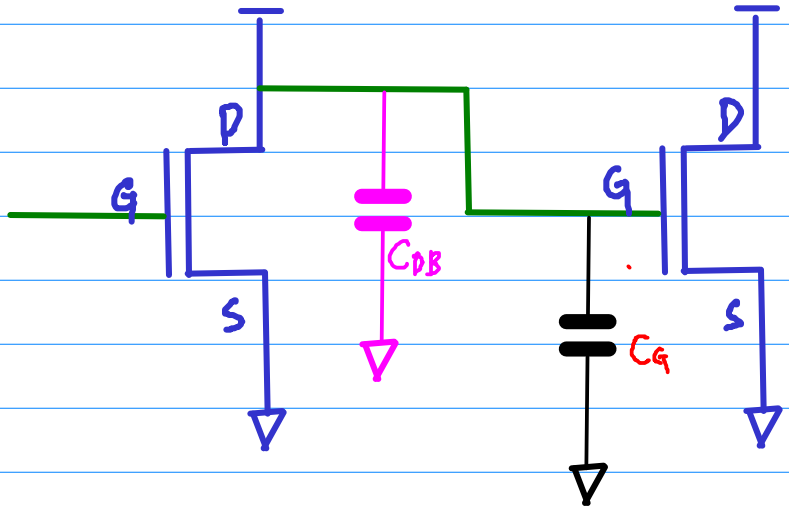
LIN $V_{DS} < V_{DSAT}$ SAT $V_{DS} > V_{DSAT}$



	① Cut off		② Linear		③ saturation	
total C_{GS}	0	+ C_{GSO}	$\frac{1}{2} C_{ox} \cdot W \cdot L$ +	C_{GSO}	$\frac{2}{3} C_{ox} \cdot W \cdot L$ +	C_{GSO}
Total C_{GD}	0	+ C_{GDO}	$\frac{1}{2} C_{ox} \cdot W \cdot L$ +	C_{GDO}	0 +	C_{GDO}
Total C_{GB}	$C_{ox} \cdot W \cdot L$ +	$2C_{GBO}$	0 +	$2 \cdot C_{GBO}$	0 +	$2 \cdot C_{GBO}$

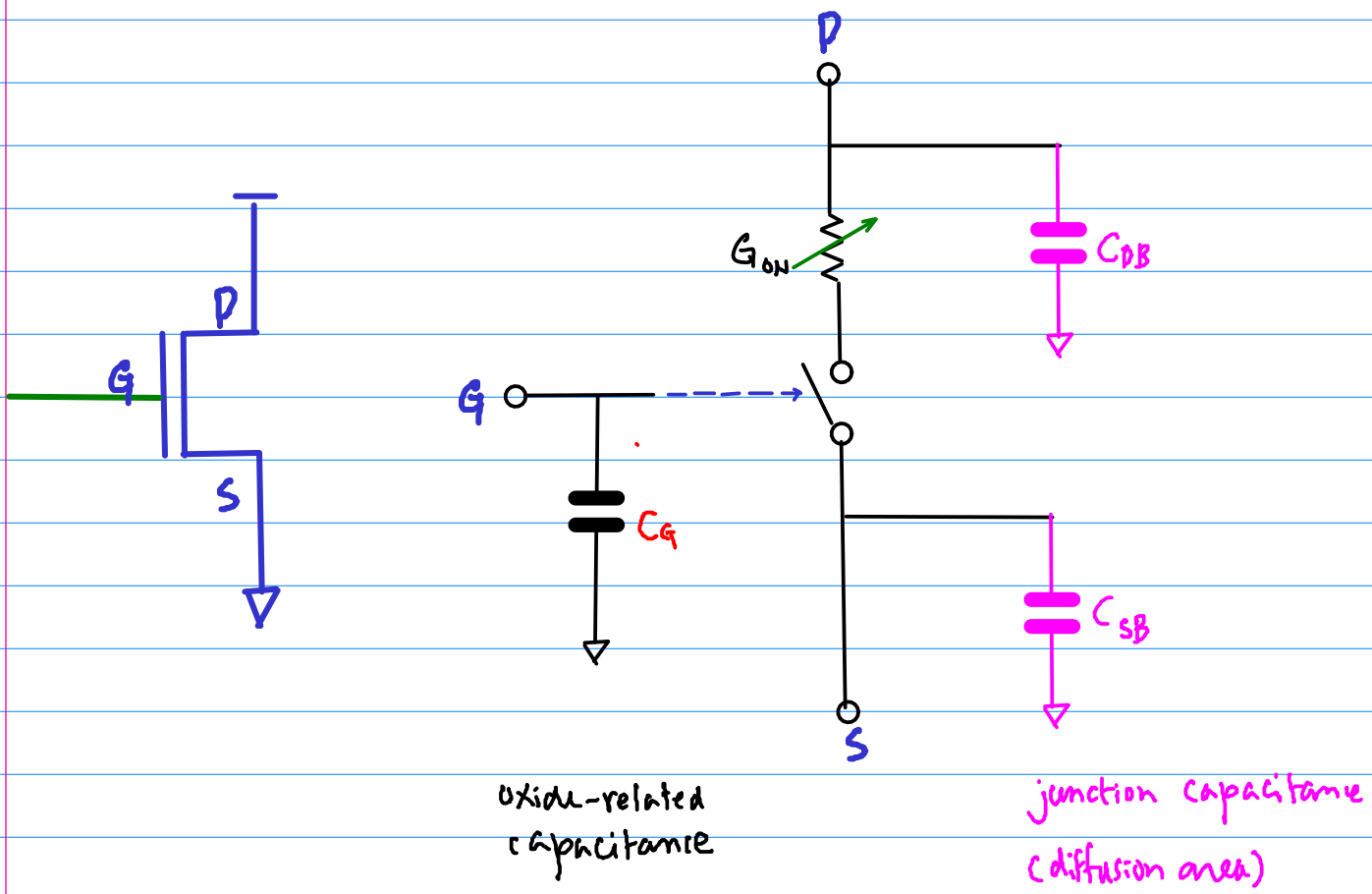
Junction Cap → Load Cap





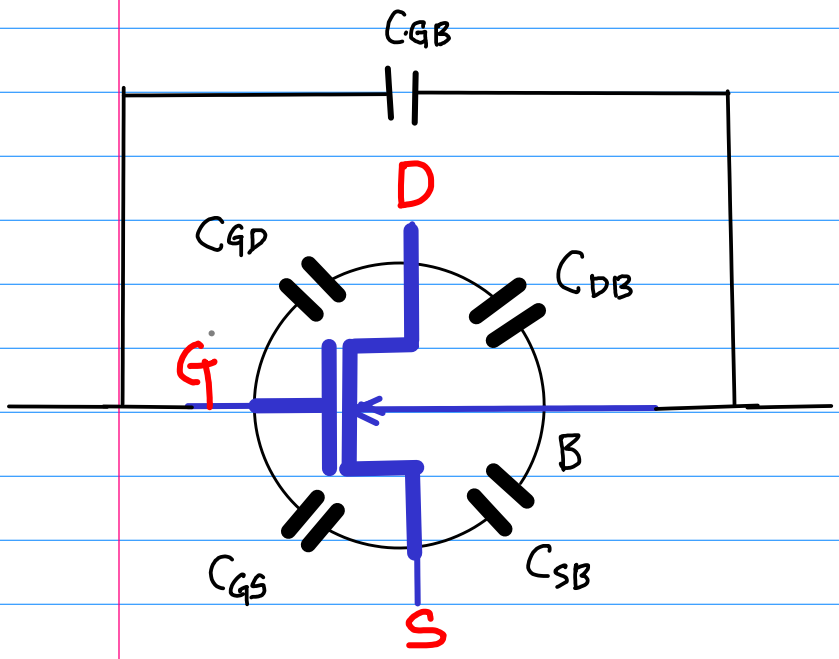
http://pingpong.chalmers.se/public/pp/public_courses/course01705/published/1348131717693/resourceId/947092/content/Chapter%202.pdf

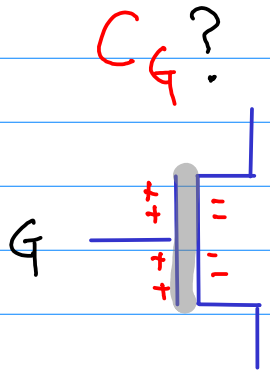
Simple Model (III)



http://pingpong.chalmers.se/public/pp/public_courses/course01705/published/1348131717693/resourceId/947092/content/Chapter%202.pdf

Other nMOS Capacitance Modelling





C_G nMOS Gate Capacitance

oxide related capacitance

overlap capacitance

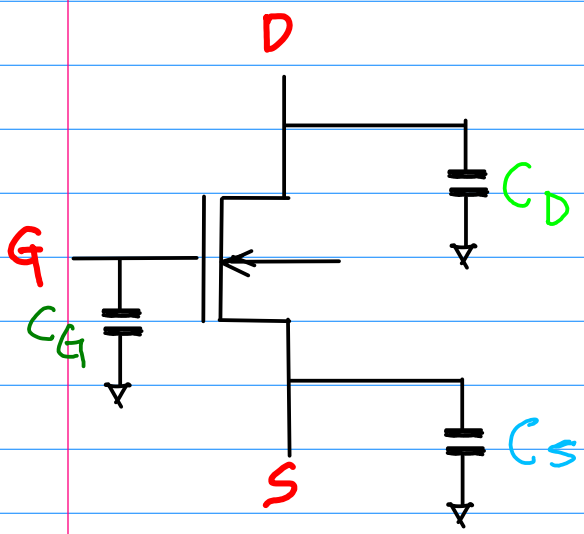
① Cut off	② Linear	③ saturation
$C_{ox} \cdot W \cdot L$	$C_{ox} \cdot W \cdot L$	$\frac{2}{3} C_{ox} \cdot W \cdot L$
$+ C_{GS0}$	$+ C_{GS0}$	$+ C_{GS0}$
$+ C_{GD0}$	$+ C_{GD0}$	$+ C_{GD0}$
$+ 2 C_{GB0}$	$+ 2 C_{GB0}$	$+ 2 C_{GB0}$

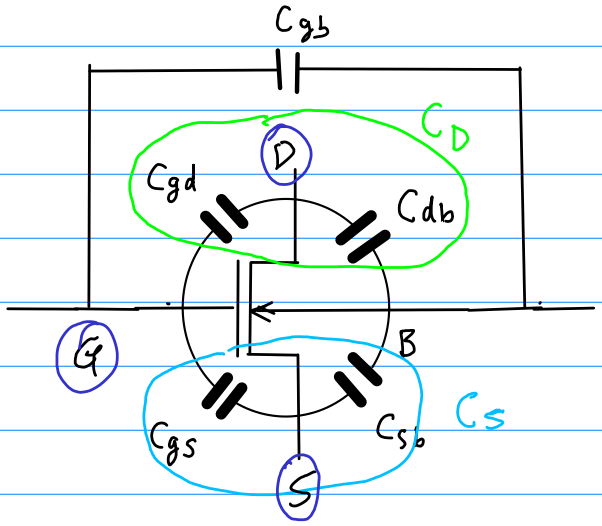
$$C_G = C_{ox} \cdot W \cdot L$$

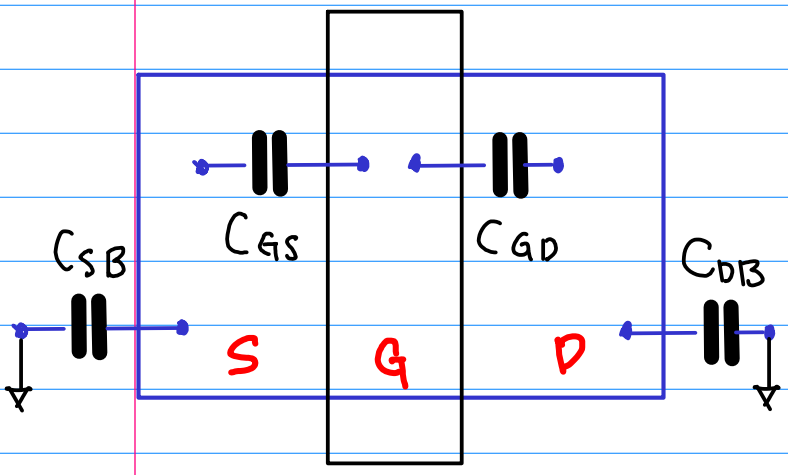
$$C_{GS} = \frac{1}{2} C_G$$

$$C_{GD} = \frac{1}{2} C_G$$

C_S & C_D







Gate Capacitance

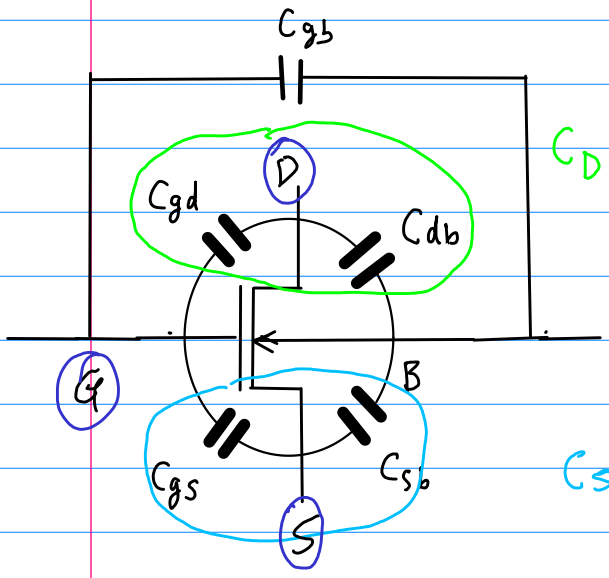
$C_S = C_{GS} + C_{SB}$

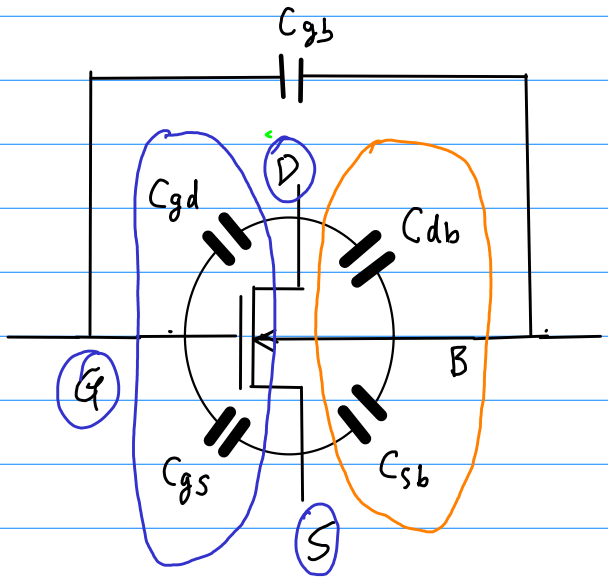
$C_D = C_{GD} + C_{DB}$

C_G

Uyemura

Oxide Cap & Junction Cap





Oxide Capacitance

Junction Capacitance

C_G Gate Capaciance

$C_S = C_{GS} + C_{SB}$

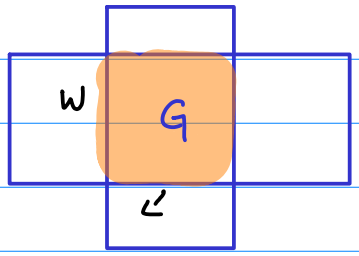
$C_D = C_{GD} + C_{DB}$

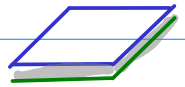
Oxide Capacitance

Junction Capacitance (Diffusion, depletion)

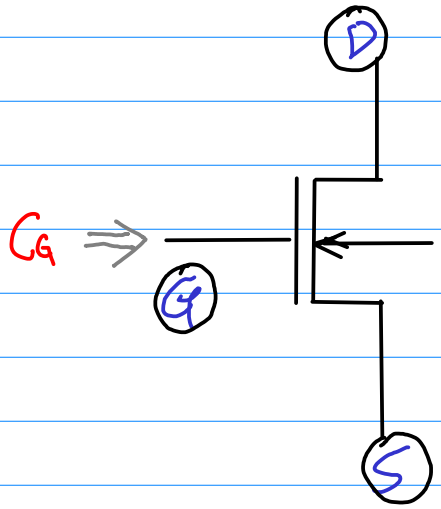
① Oxide Capacitance

C_G

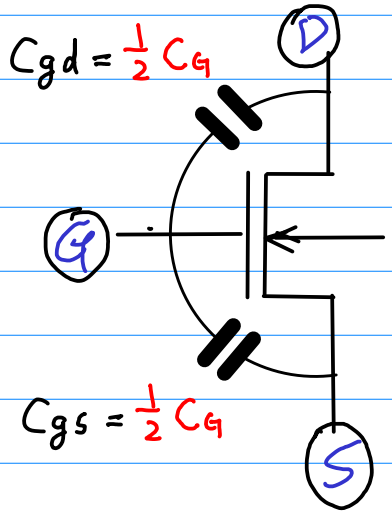




$C_G = C_{ox} L'W$



$C_G \Rightarrow$



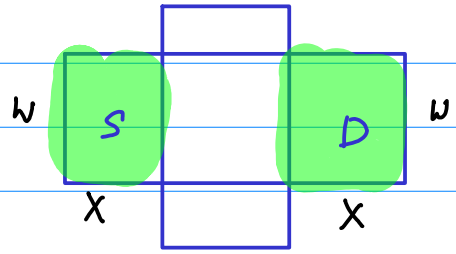
$C_{gd} = \frac{1}{2} C_G$

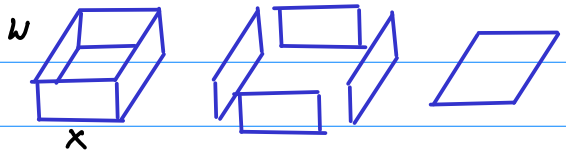
$C_{gs} = \frac{1}{2} C_G$

Oxide Related Capacitance

② Junction Capacitance

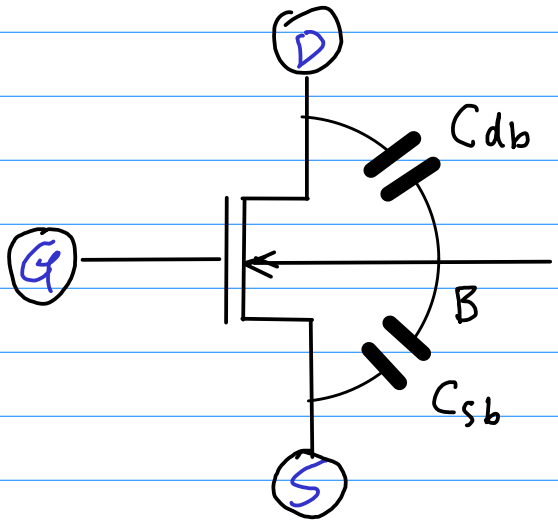
C_S , C_D





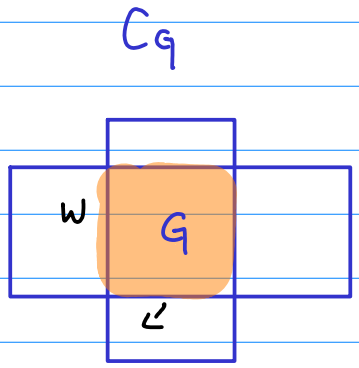
sidewall C_{sw}

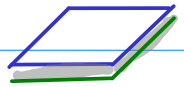
bottom C_{bot}



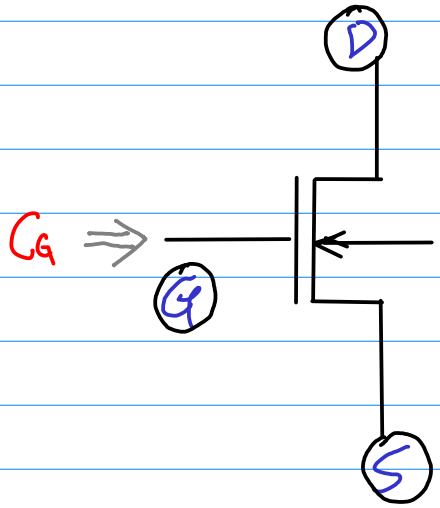
Junction Capacitance

1 Oxide Capacitance





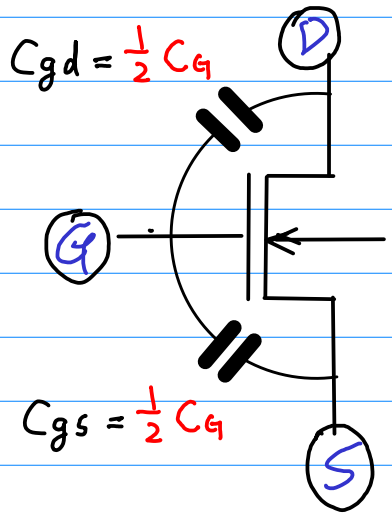
$$C_G = C_{ox} L'W$$



Gate Capaciance

$$C_S = C_{GS} + C_{SB}$$
$$+$$
$$C_D = C_{GD} + C_{DB}$$

C_G

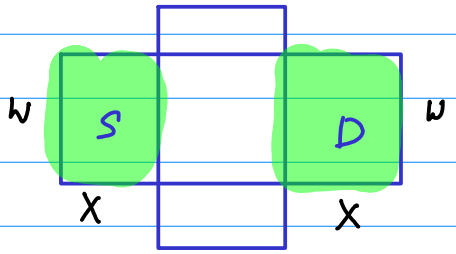


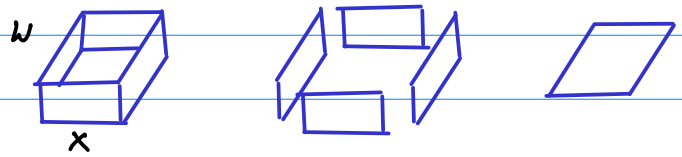
Uyemura

Oxide Related Capacitance

② Junction Capacitance

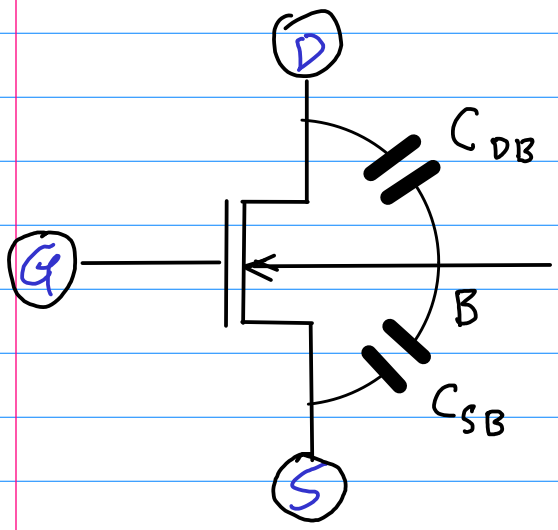
C_S , C_D





sidewall
C_{sw}

bottom
C_{bot}



C_{DB}

C_{SB}

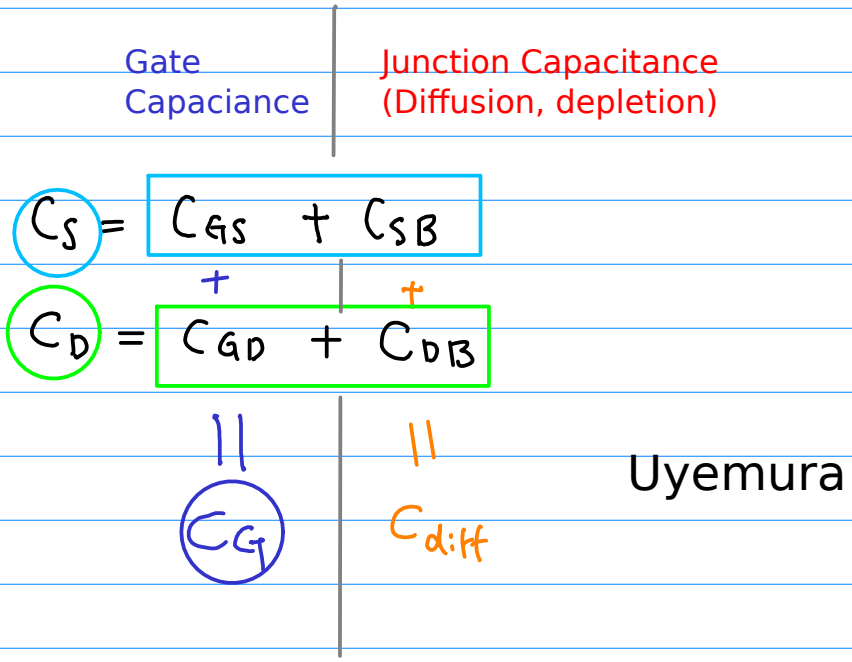
Junction Capacitance

$$C_S = C_{GS} + C_{SB}$$

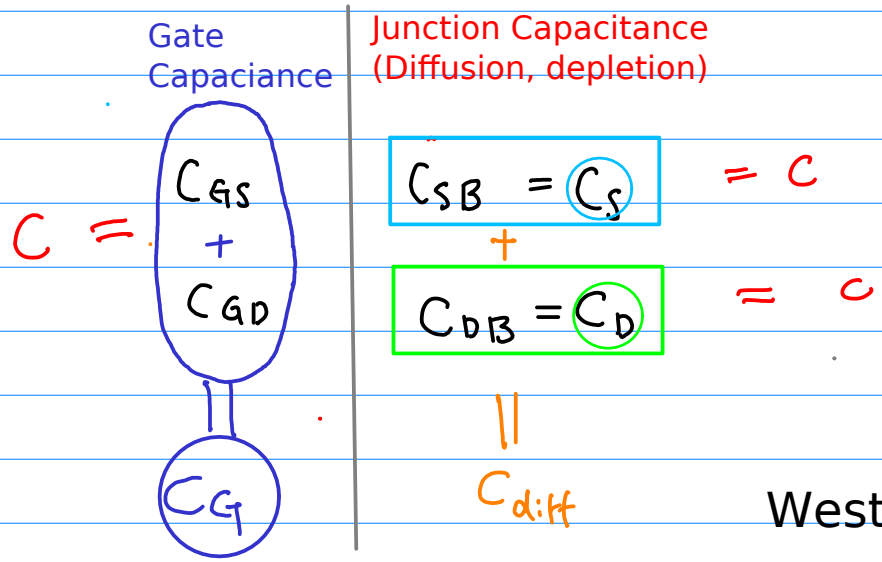
$$C_D = C_{GD} + C_{DB}$$

Junction Capacitance
(Diffusion, depletion)

Further Simplification for hand calculations



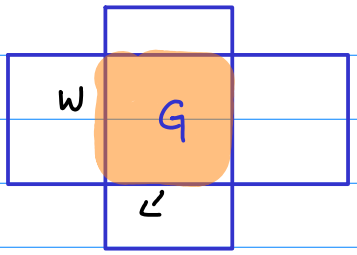
Uyemura



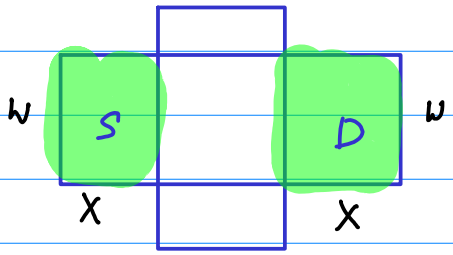
Weste

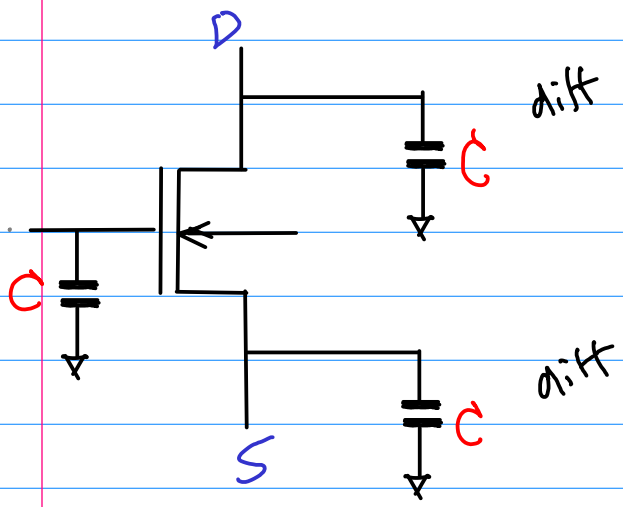
* Cs, Cd consists of diffusion capacitance only

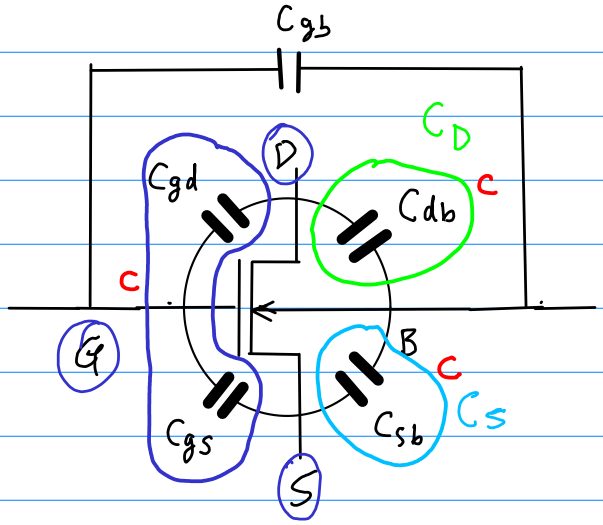
$C_G = C$



$C_S = C_D = C$







Gate Capaciance

$C = C_{GS} + C_{GD}$

C_G

Junction Capacitance (Diffusion, depletion)

$C_{SB} = C_S$ $= C$

$+$

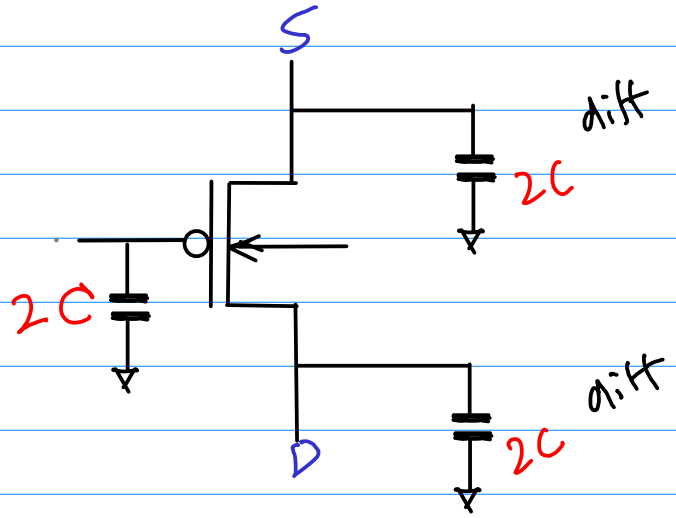
$C_{DB} = C_D$ $= C$

$\parallel$

C_{diff}

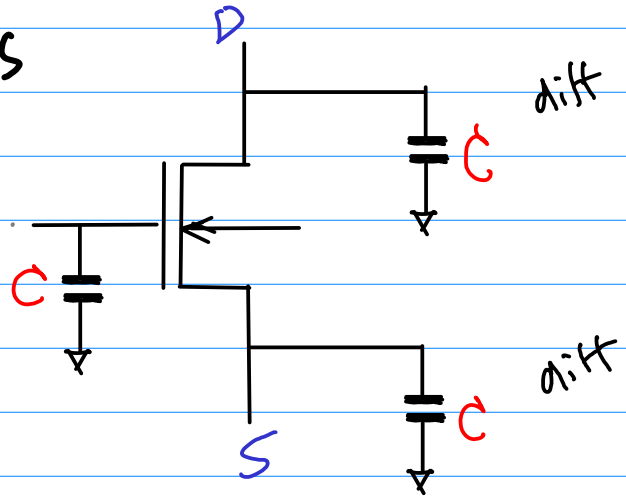
Weste

pMOS

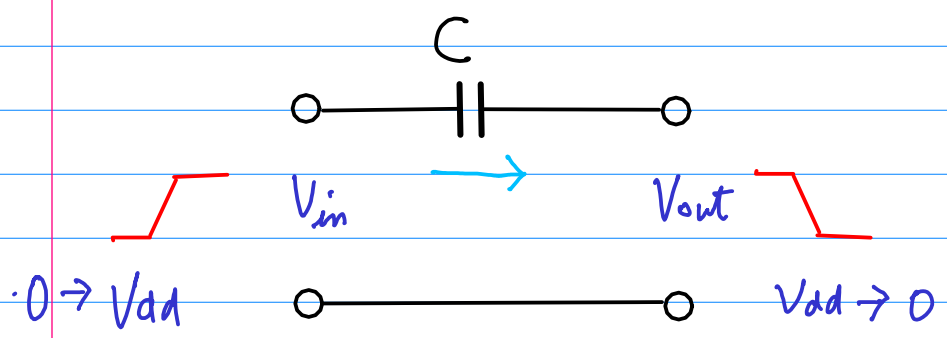


normally
twice bigger

nMOS



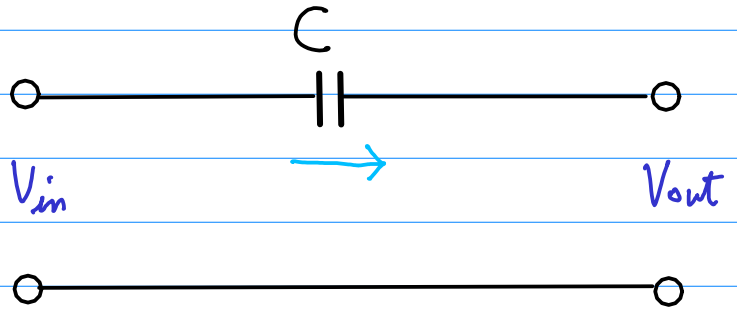
Miller Capacitance

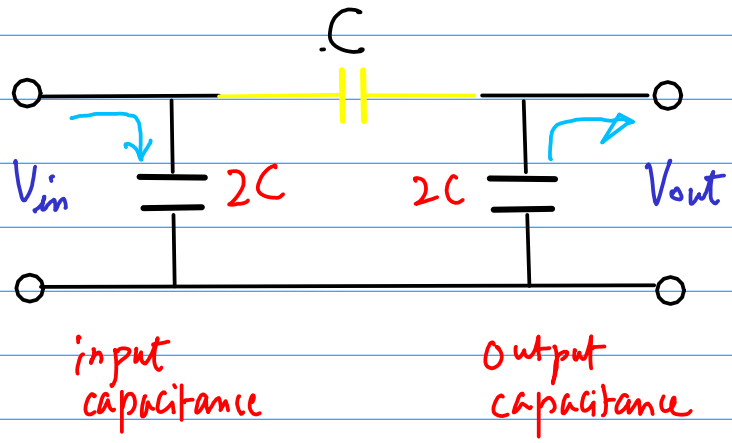


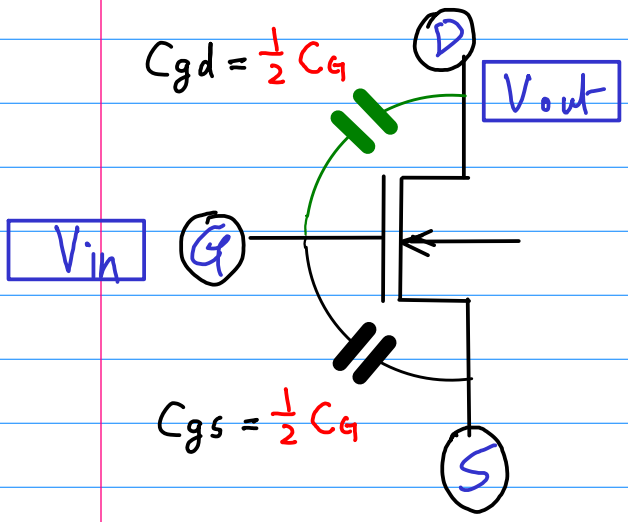
$$Q_{init} = C \cdot (0 - V_{DD}) = -CV_{DD}$$

$$Q_{final} = C \cdot (V_{DD} - 0) = +CV_{DD}$$

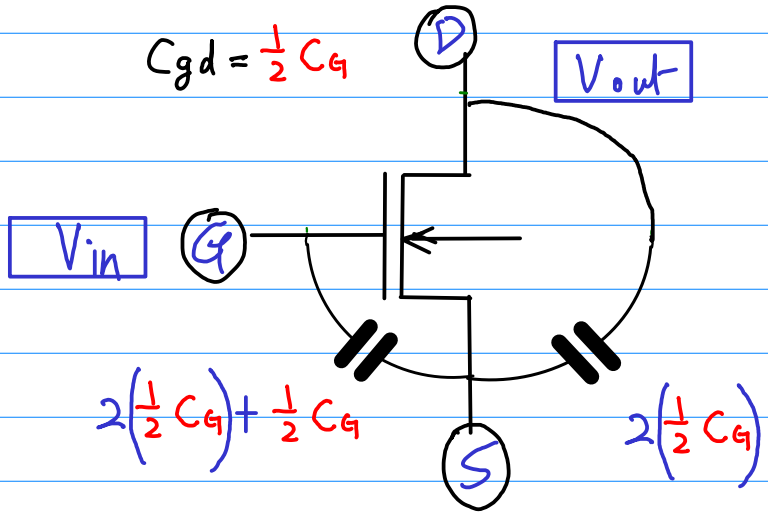
$$Q_{total} = Q_{final} - Q_{init} = 2CV_{DD}$$


C
V_{in}
V_{out}

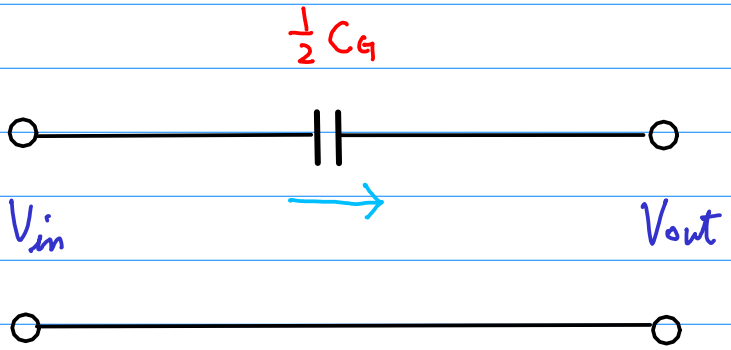

C
V_{in}
2C
2C
V_{out}
input capacitance
output capacitance

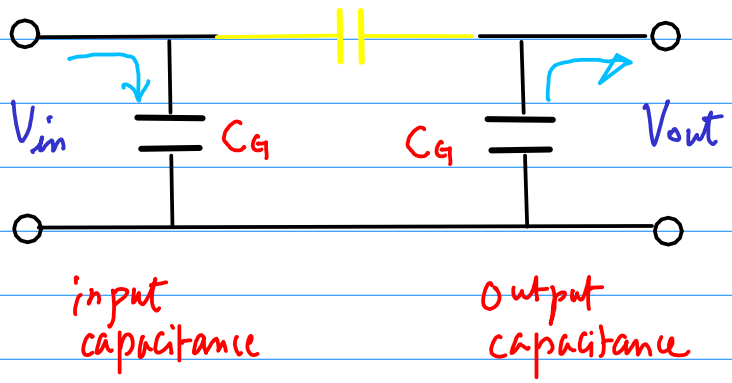


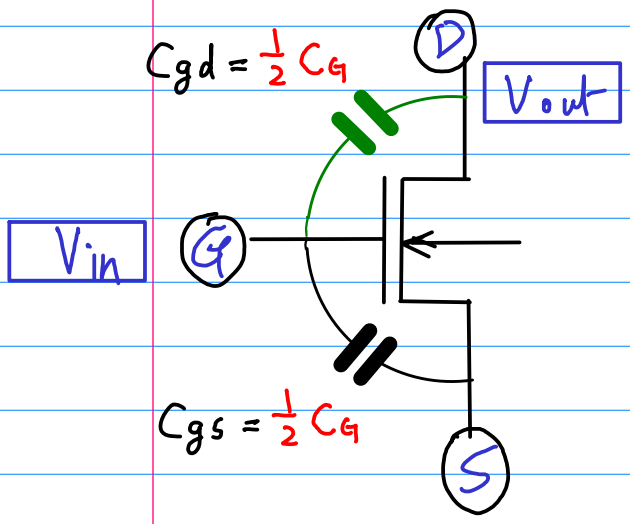
Oxide Related Capacitance



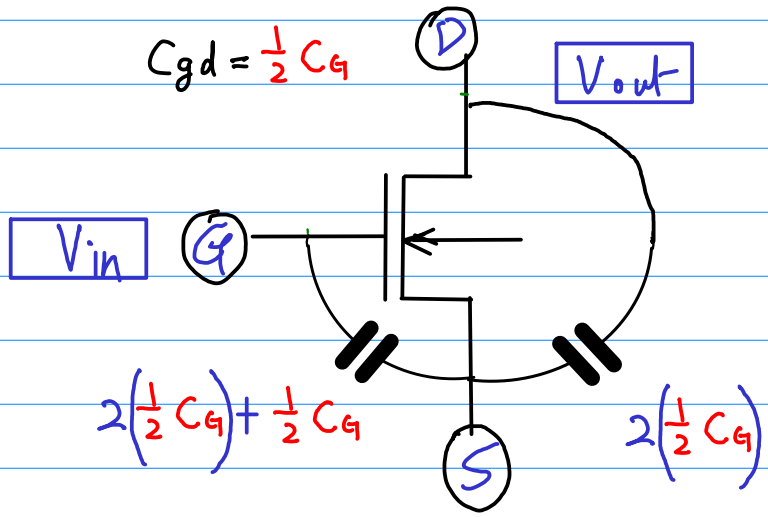
Oxide Related Capacitance



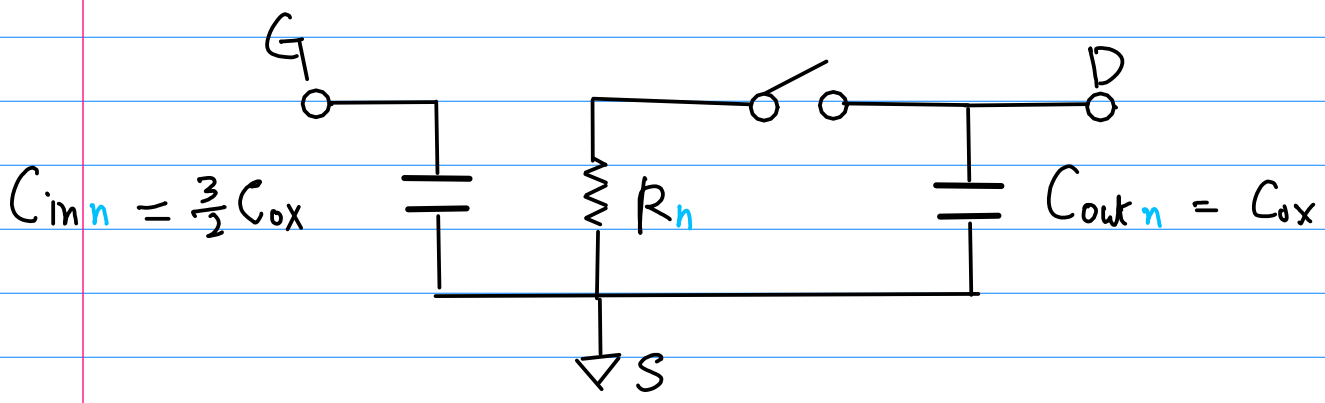




Oxide Related Capacitance



Oxide Related Capacitance



Baker cmosedu

References

Some Figures from the following sites

[1] http://pages.hmc.edu/harris/cmosvlsi/4e/index.html
Weste & Harris Book Site

[2] en.wikipedia.org

[3] Uyemura, Introduction to VLSI Circuits and Systems