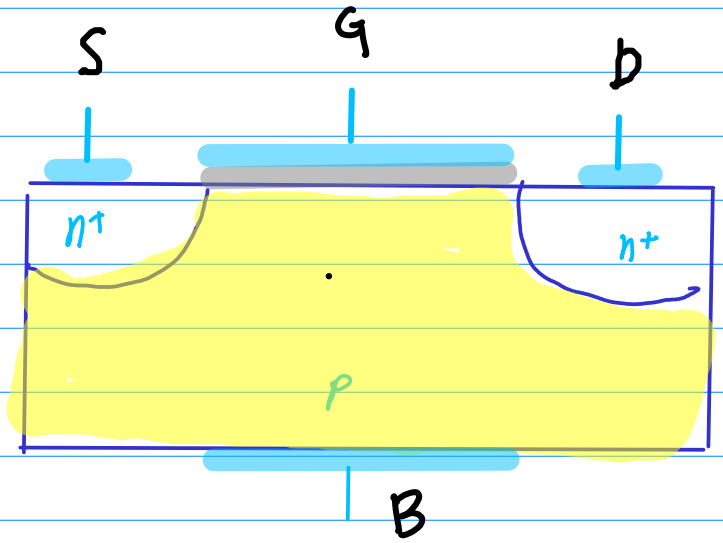
MOSFET Theory (H.1)

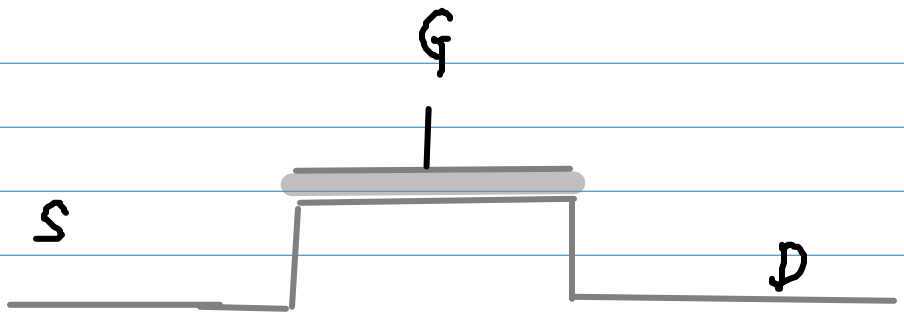
20160227

Principles of nMOS Capacitor

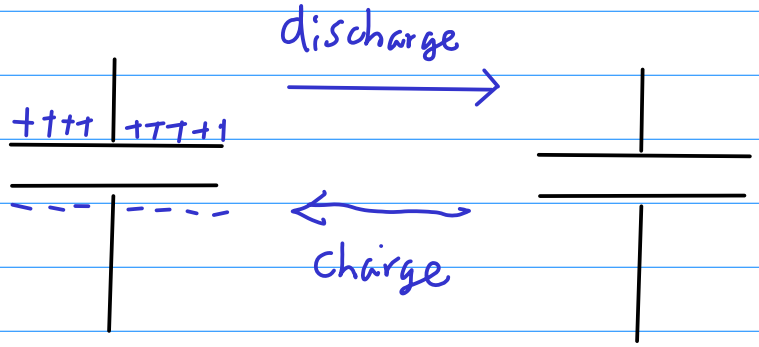
MOS Capacitor



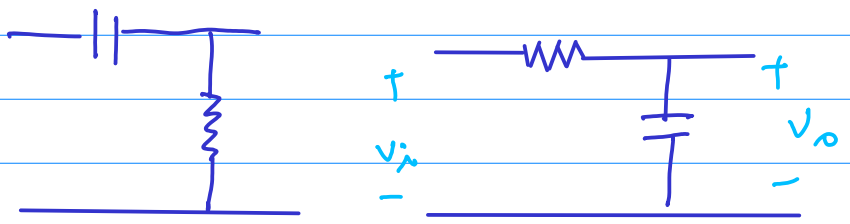
Metal / polysilicon
Oxide – insulator
Silicon

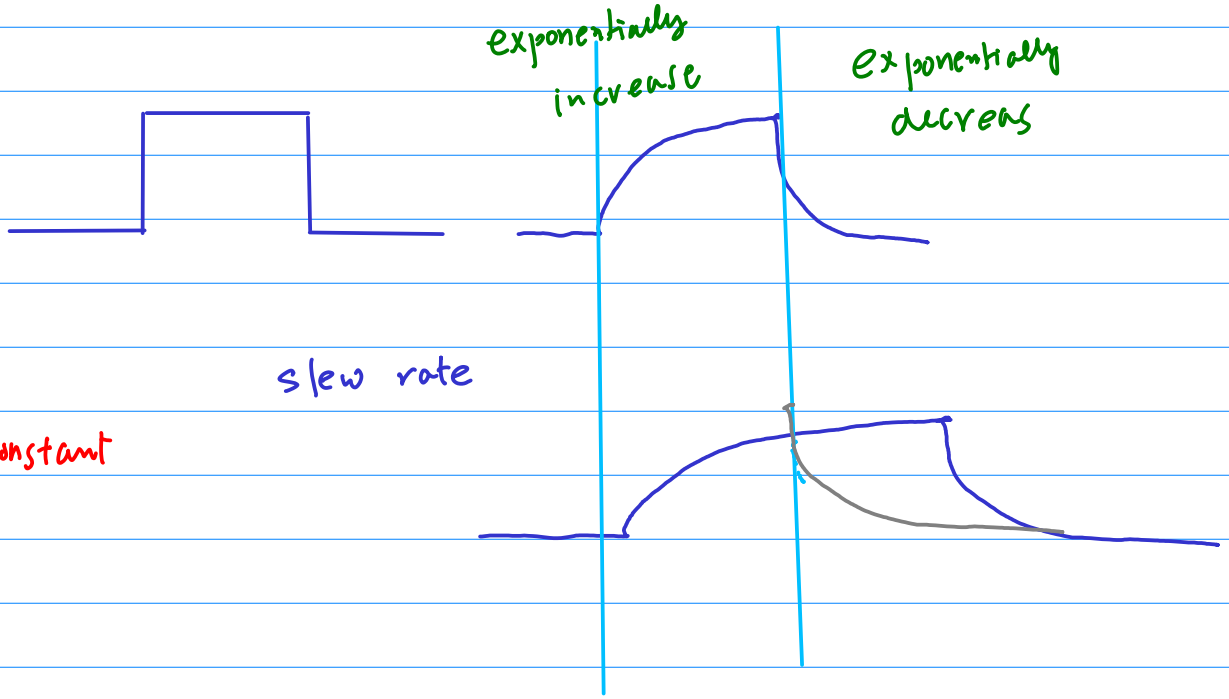


Capacitor C



R · C

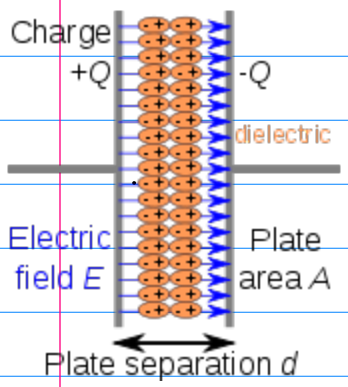




slew rate

Time constant

Capacitor



Definition - What does *Positive Charge* mean?

In an atom, a positive charge occurs when an atom has more protons than electrons. The proton is what determines its positive charge. It is denoted with a plus (+) sign. It attracts negative charges and repels other positive charges. In NaCl, the sodium cations, Na^{+}, are neutralized by chlorine anions, Cl^{-}.

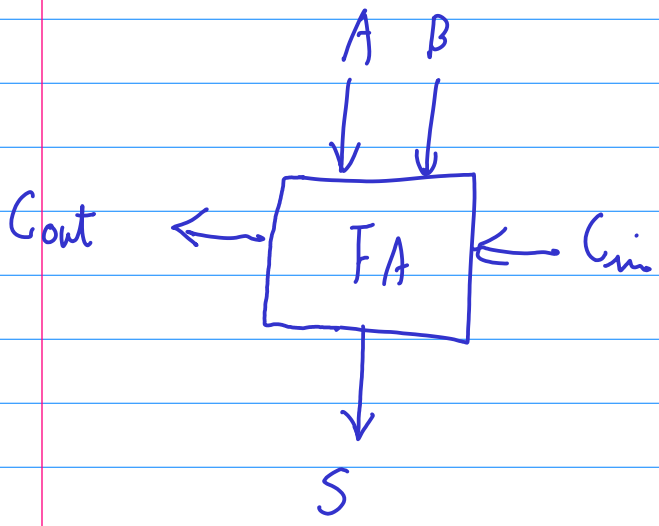
In general, metals lose electrons to form positively charged ions (Fe^{+2}, Au^{+3}, Ag^{+}), and nonmetals gain electrons to form negatively charged ions.

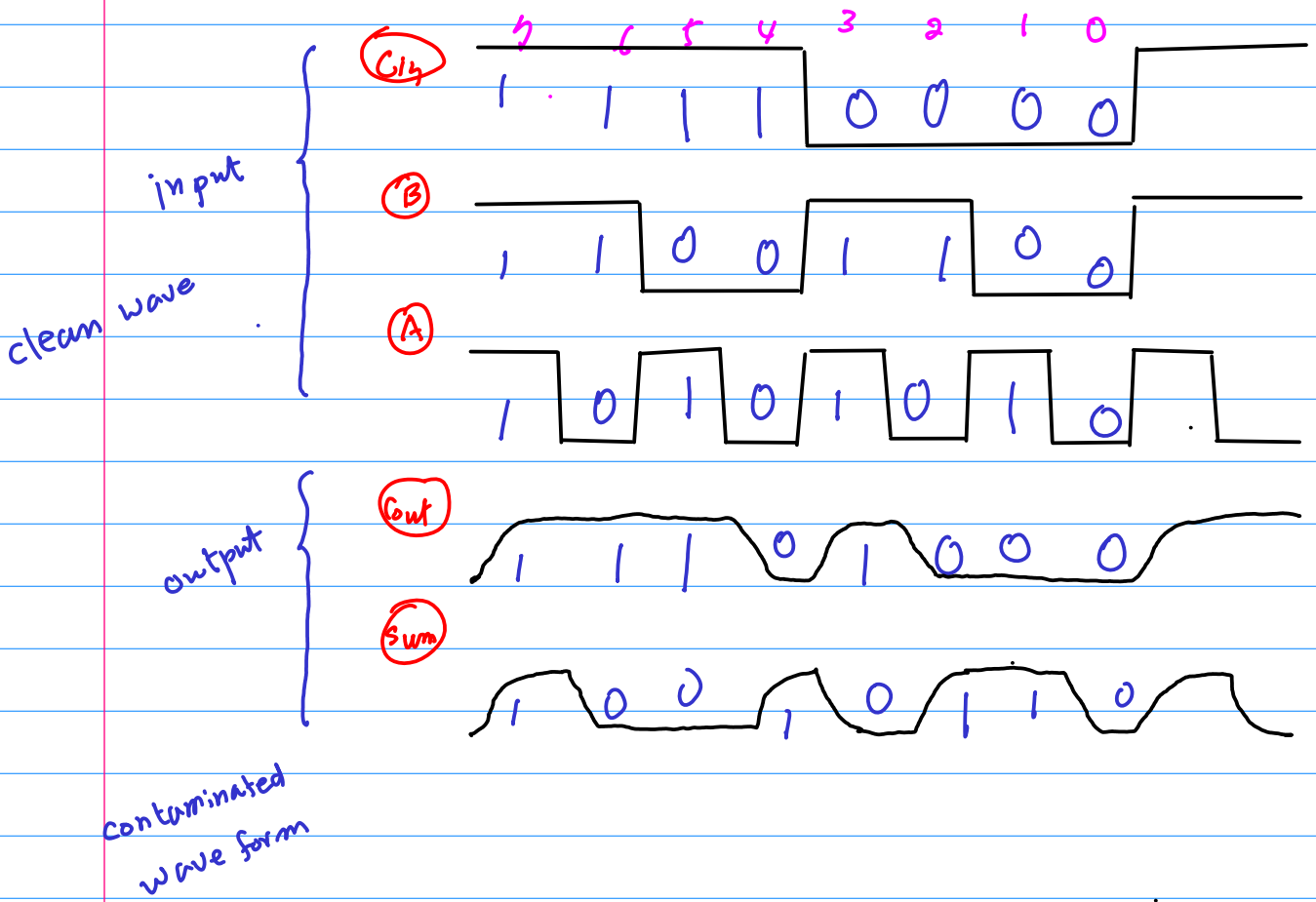
A positive charge is also known as a cation.

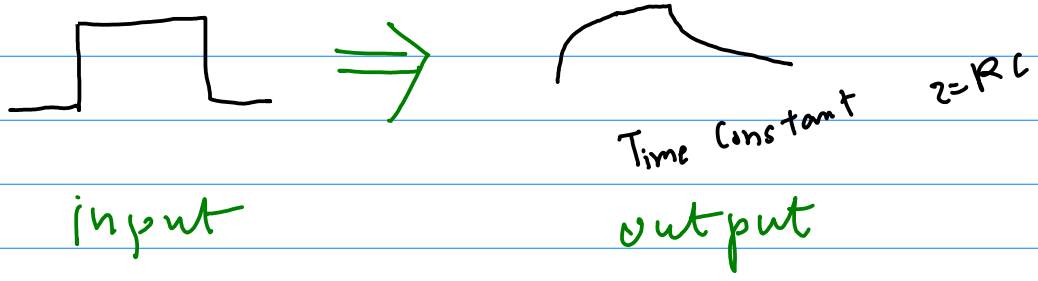
In a battery, the positive end (or cathode) is attractive to electrons, due to its positive charge. Metal loss at anodic sites in an electrochemical cell occurs when the metal atoms give up one or more electrons and move as positively charged ions into the electrolyte.

https://www.corrosionpedia.com/

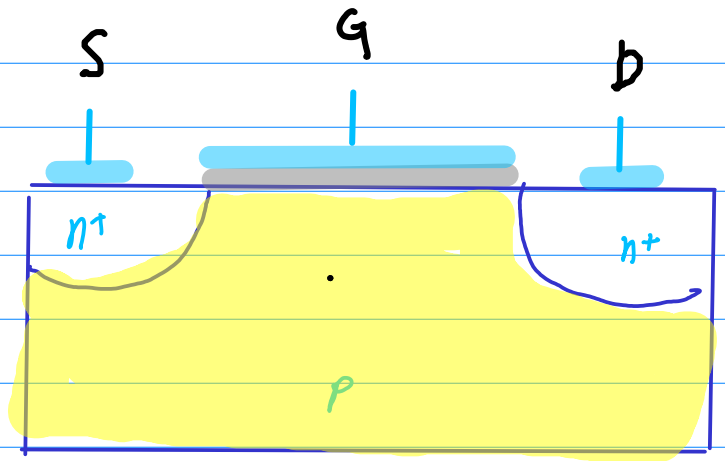
Delay Example: Full Adder







majority carrier

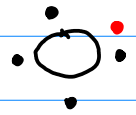


Metal / polysilicon
Oxide – insulator
Silicon

n-type added impurities
⇒ extra electrons
⇒ majority carrier

Donor

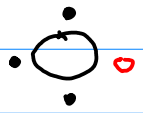
n-type semiconductor



p-type added impurities
⇒ extra hole
⇒ majority carrier

Acceptor

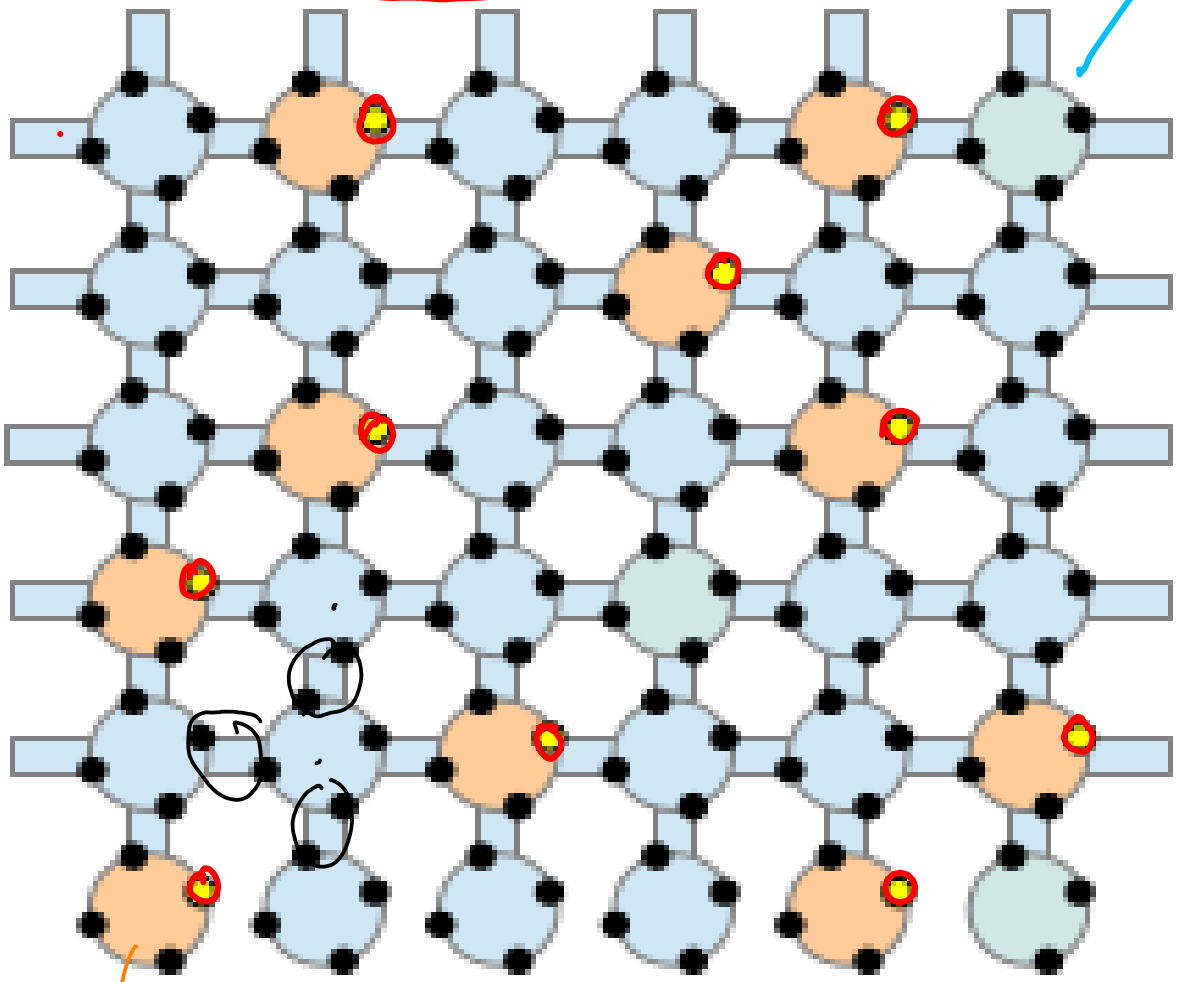
p-type semiconductor



Acceptor Doping Impurities

vacancies of impurity atoms

Silicon atoms



Covalent Bonding

an Impurity atom and vacancy

Vacancy v.s. hole

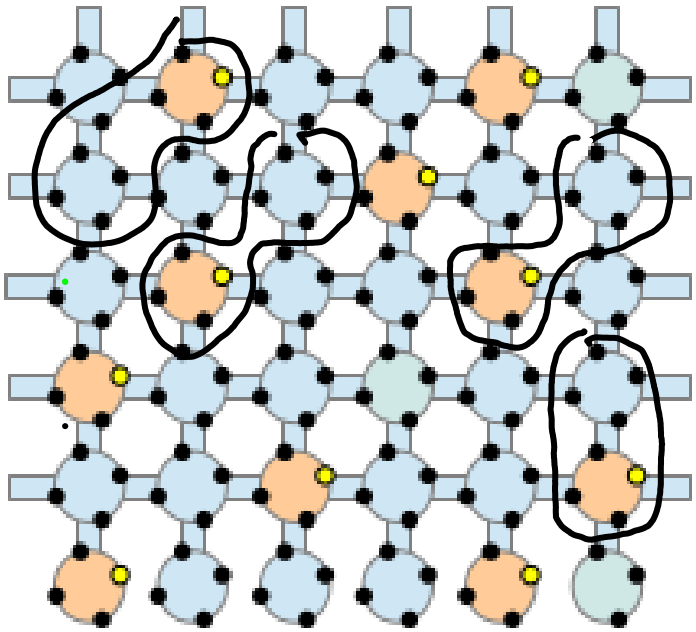
immobile ion

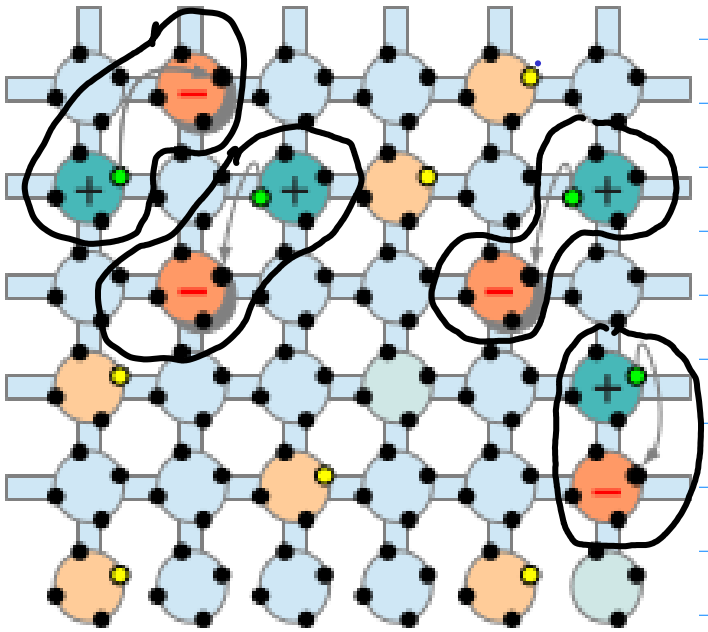
⊖ negative ion

⊕ positive ion

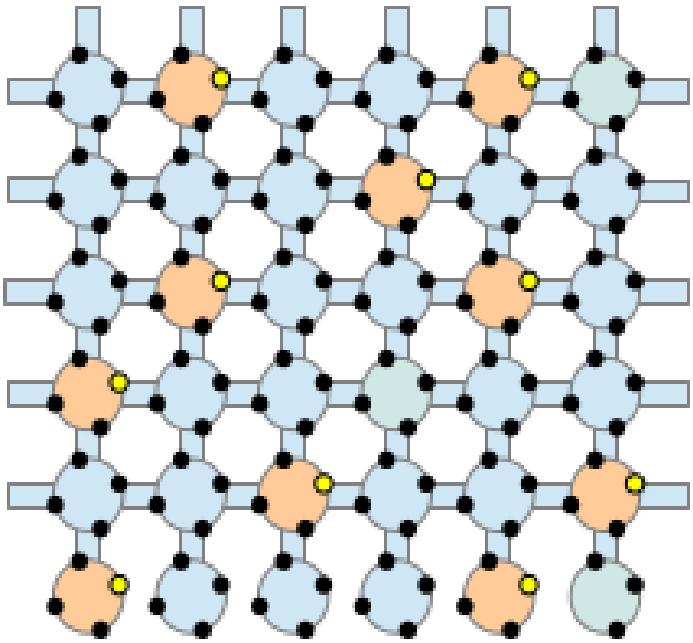
vacancies

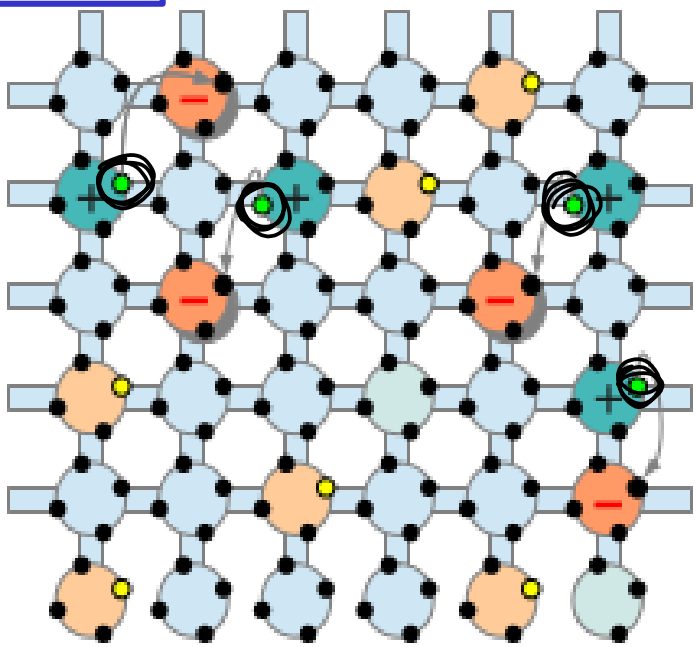
holes



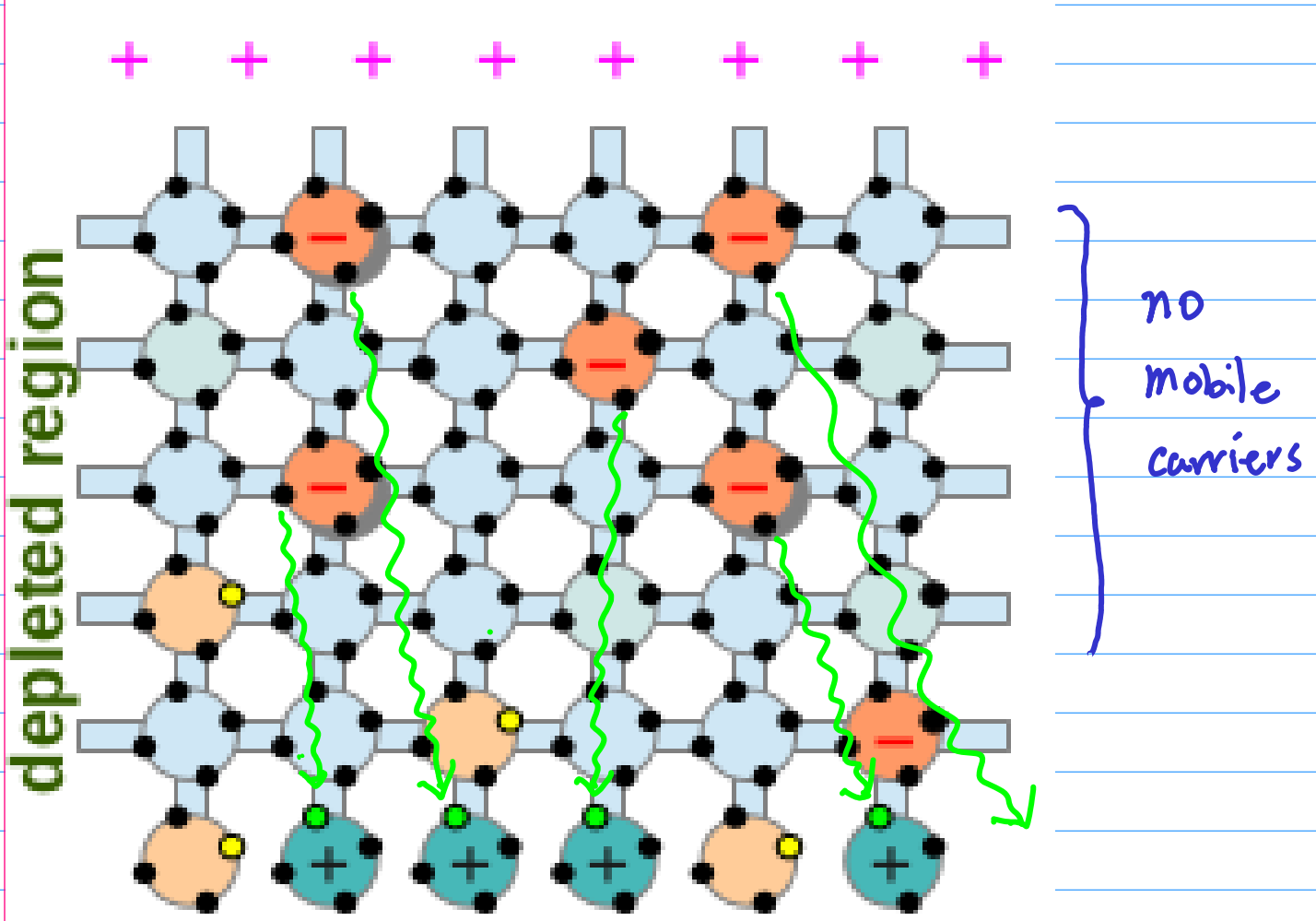


vacancies ⟷ holes



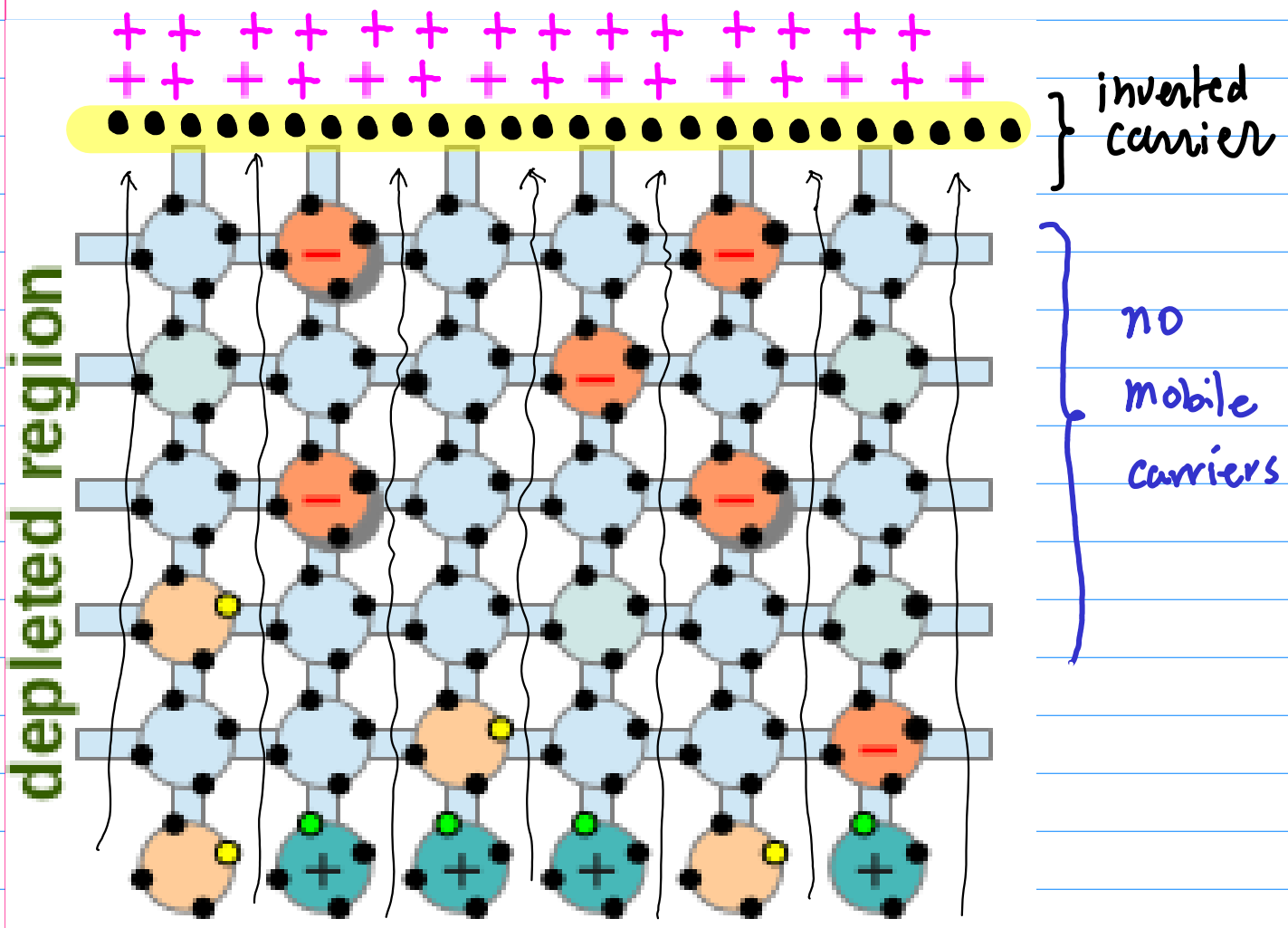


Deplete 'mobile' carriers



holes are repelled by +

Invert carrier type (majority → minority)

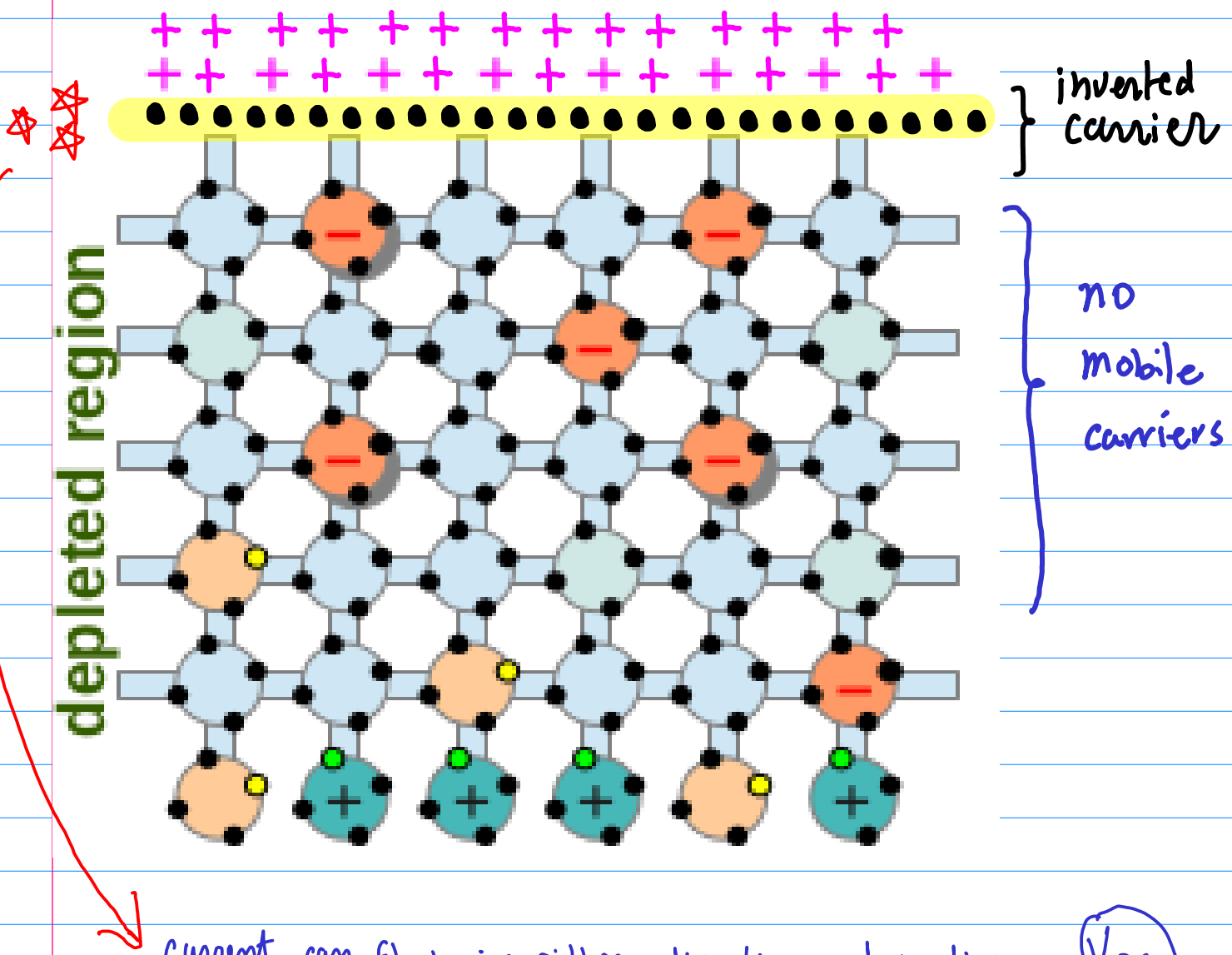


holes are repelled by +

electrons are attracted toward the surface

		majority carrier	minority carrier
donor	p-type	electrons	holes
acceptor	n-type	holes	electrons

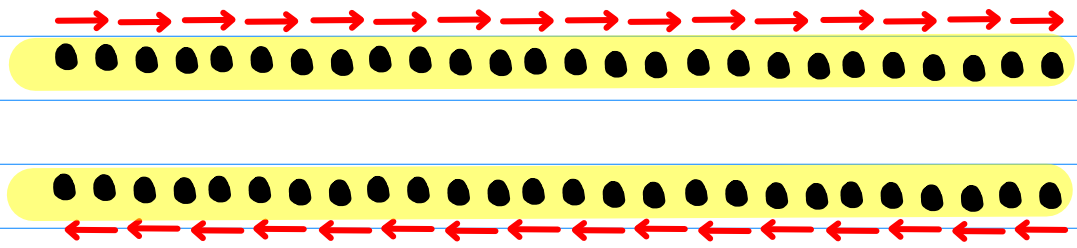
Invert carrier type (majority → minority)



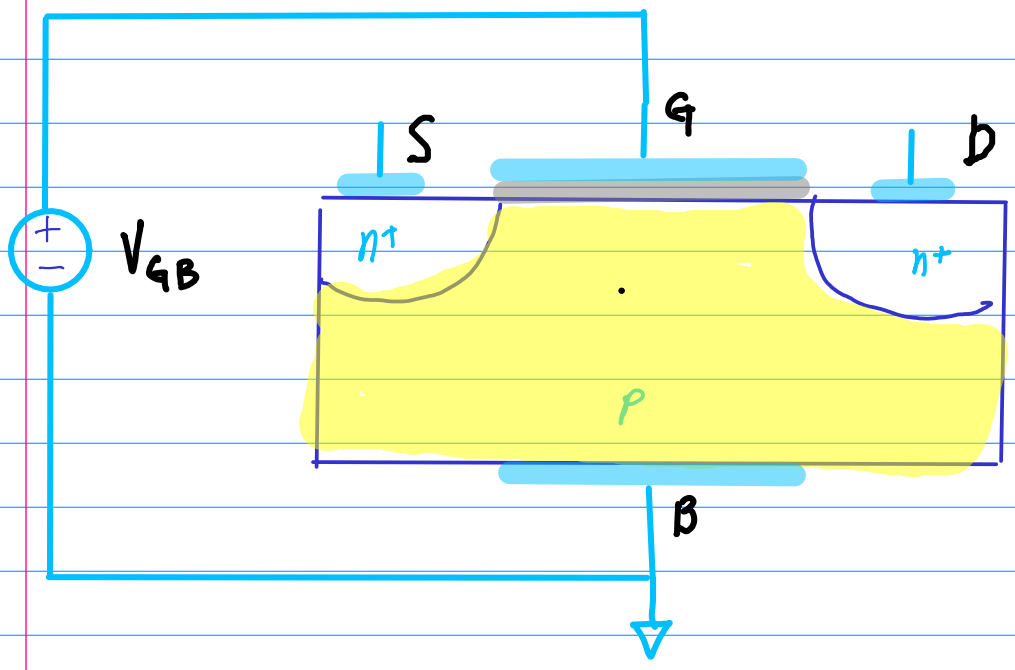
current can flow in either direction, depending on V_{DS}

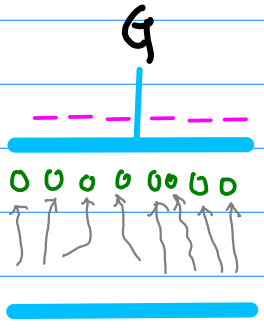
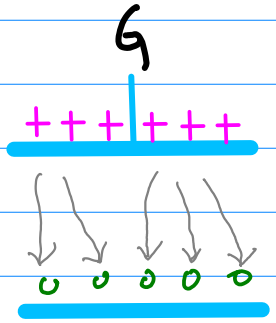
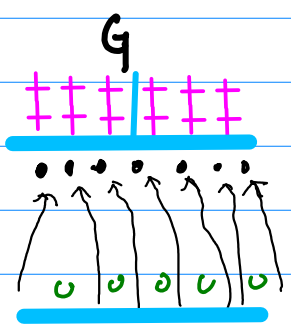
not in the depletion layer

but in the inversion layer

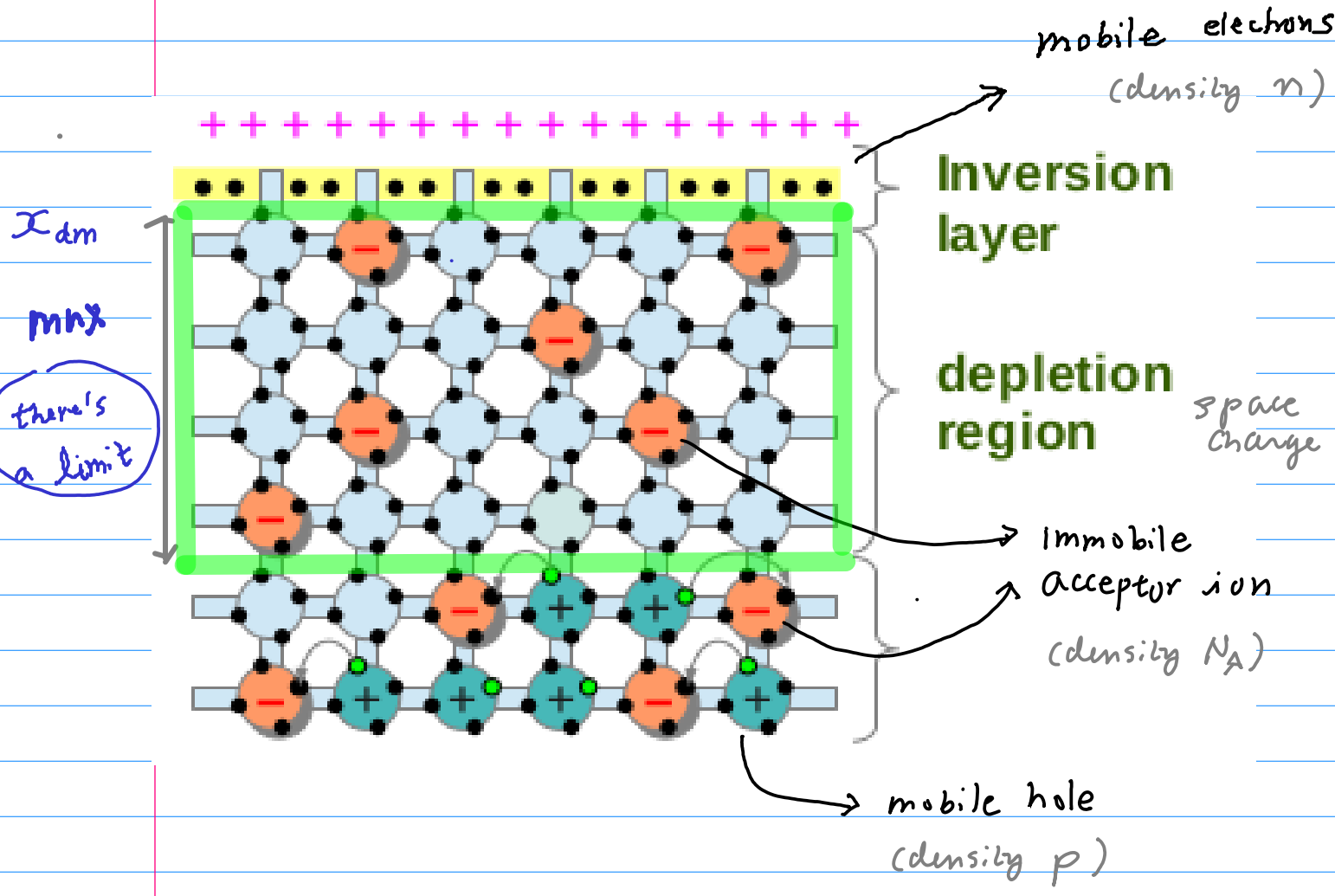


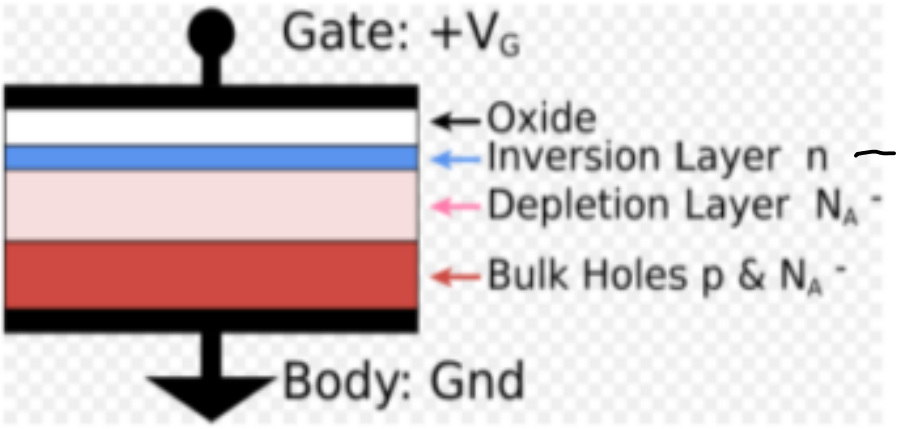
MOS structure : V_{GB} Bias

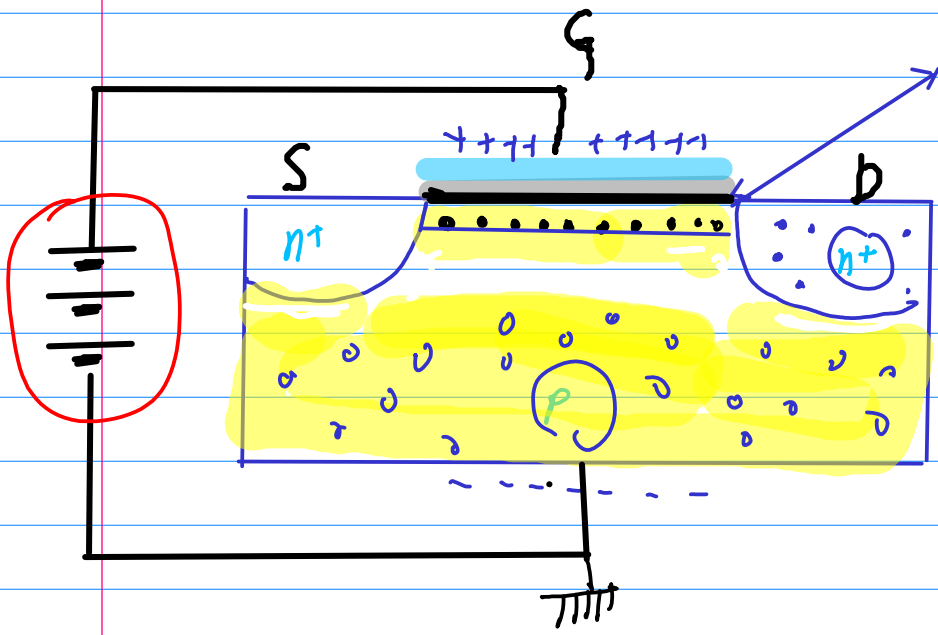


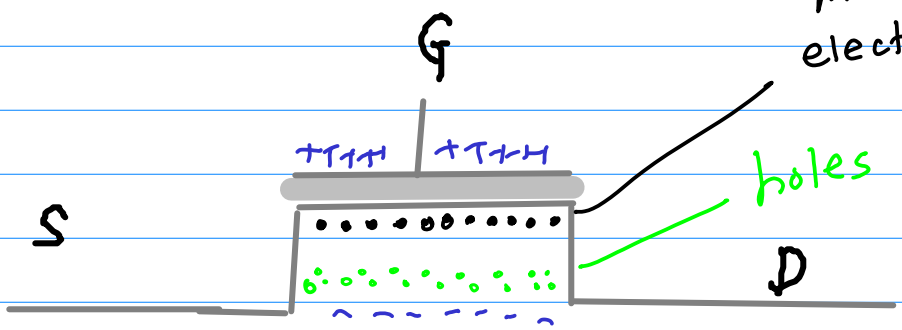
Accumulation	Depletion	Inversion
majority carriers	majority carrier	minority carrier
		
attracts holes	repels holes	repels holes attracts electrons
$V_{GB} < 0$	$0 < V_{GB} < V_t$	$V_t < V_{GB}$

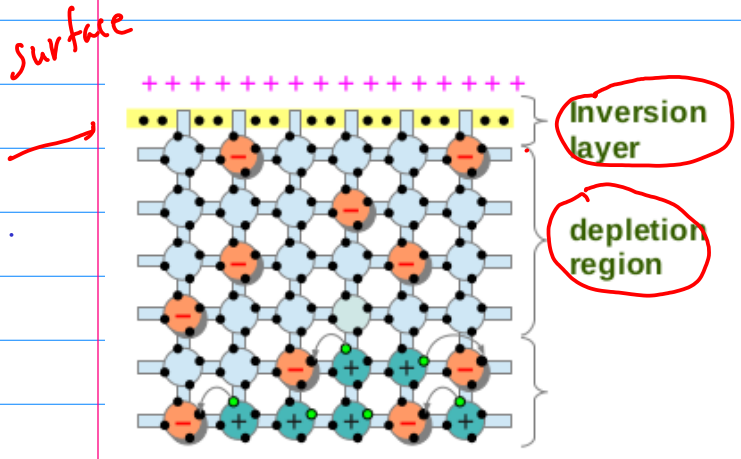
Layers

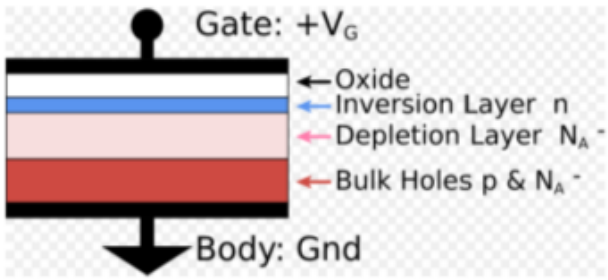

mobile electrons
(density n)
Inversion layer
depletion region
space charge
x_{dm}
max
there's a limit
immobile acceptor ion
(density N_A)
mobile hole
(density p)


Gate: $+V_G$
Oxide
Inversion Layer n
Depletion Layer N_A^-
Bulk Holes p & N_A^-
Body: Gnd
mobile electrons
immobile ions


G
surface
S
D
n+
n+
p
Metal / polysilicon
Oxide
Silicon


G
mobile electrons → Channel
(inversion layer)
holes
S
D


surface
Inversion layer
depletion region


Gate: +V_G
Oxide
Inversion Layer n
Depletion Layer N_A -
Bulk Holes p & N_A -
Body: Gnd

Gate and body form MOS capacitor

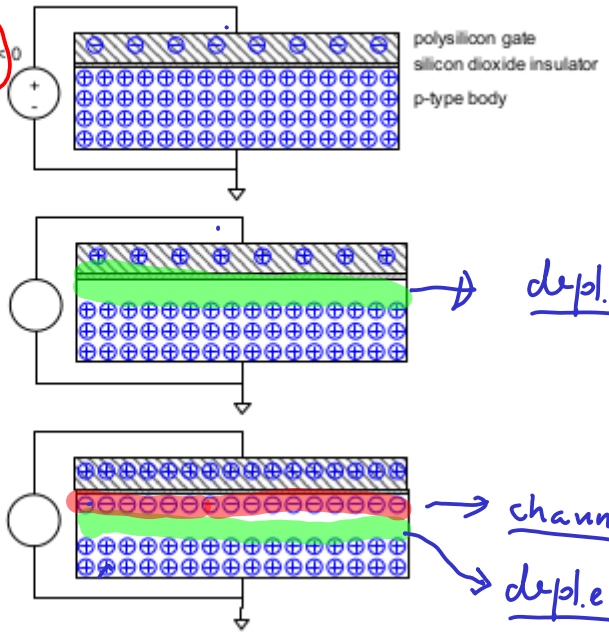
Operating modes

- Accumulation — hole
- Depletion — hole
- Inversion — electron

$V_g < 0$

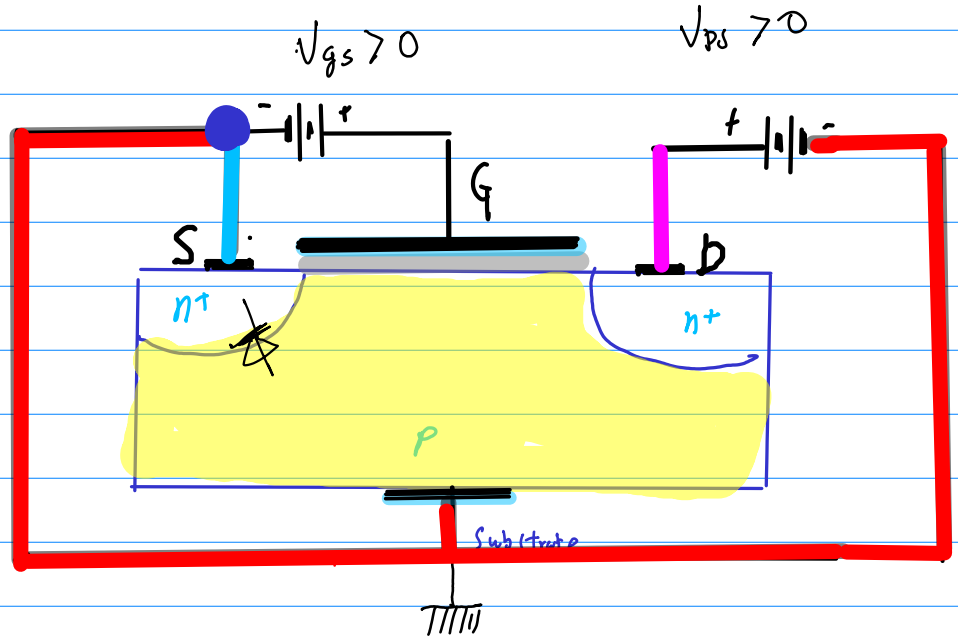
$0 < V_g < V_t$

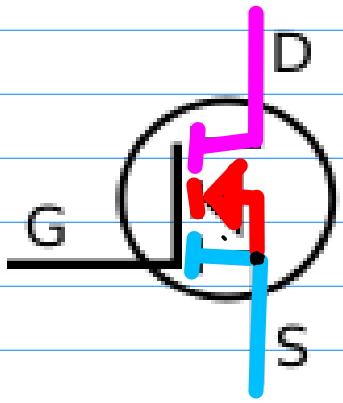
$V_g > V_t$

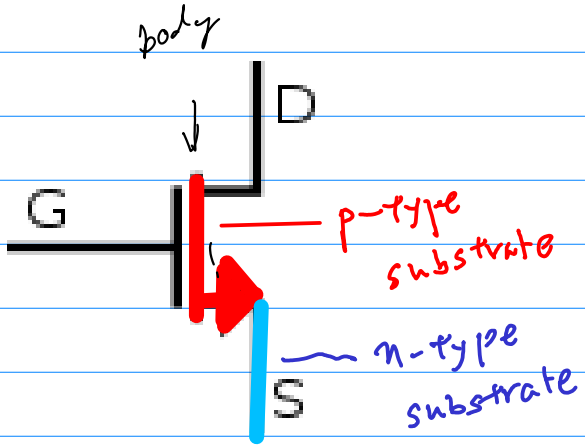


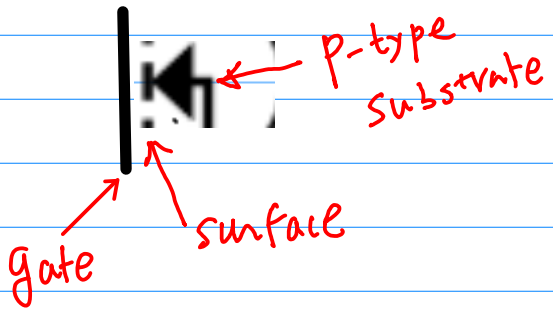
depletion — no mobile carrier (hole or electrons)

Substrate connection









nMOS Symbols

Although the MOSFET is a four-terminal device
with source (S), gate (G), drain (D), and body (B) terminals,
the body (or substrate) of the MOSFET is often
connected to the source terminal,
making it a three-terminal device
like other field-effect transistors.

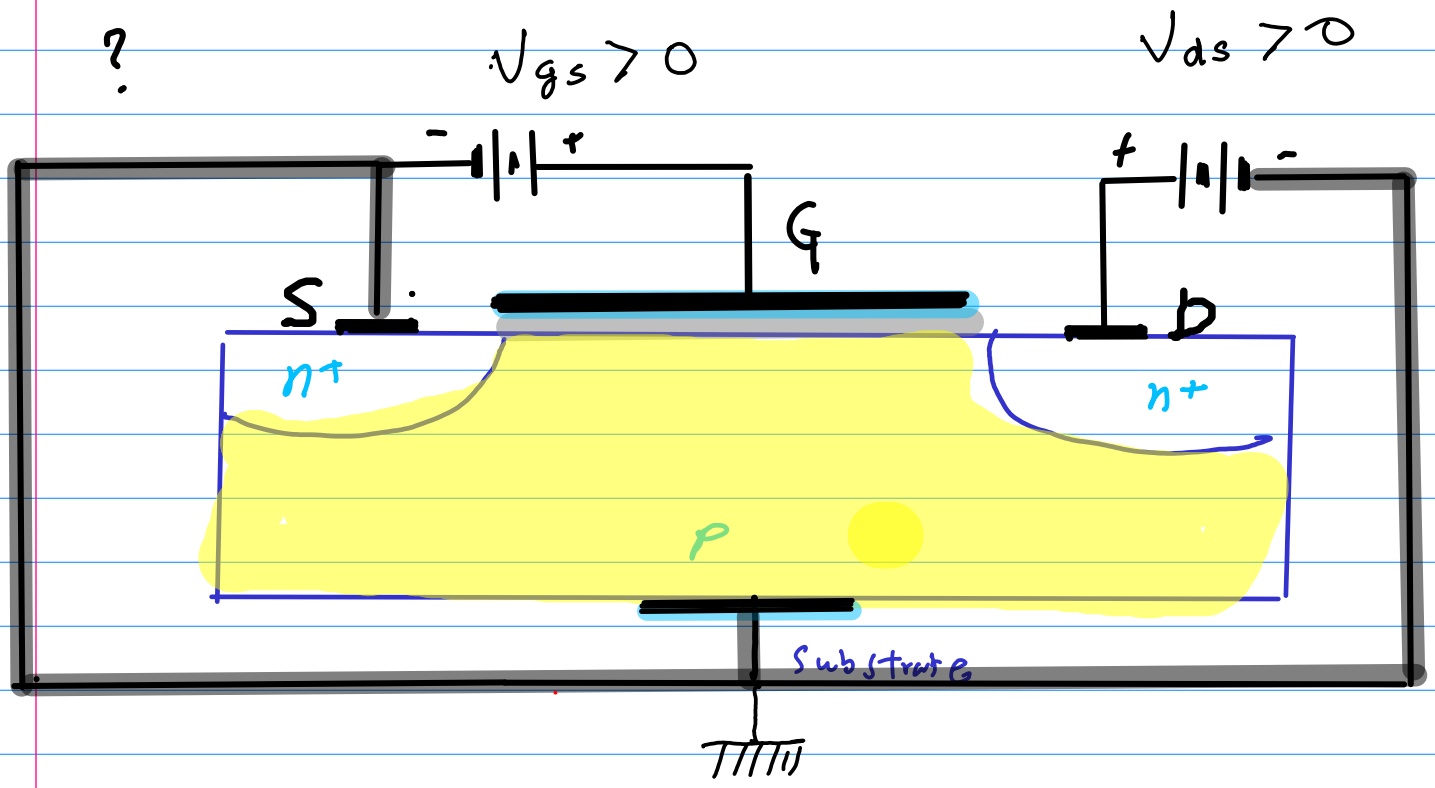
http://electronics.stackexchange.com/questions
/72582/mosfet-why-the-drain-and-source-are-different

Latch-up

Body Effect

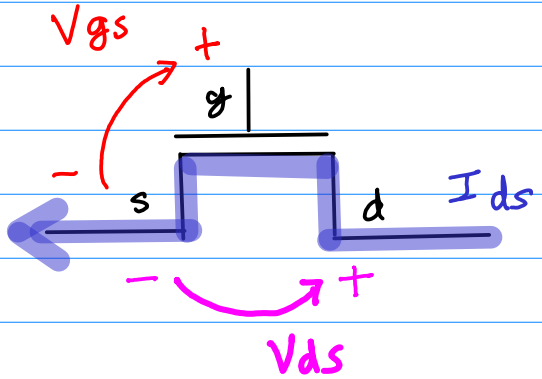
MOS Bias

?



$V_g > V_t$

$V_{gs} > V_t$



Source (S)

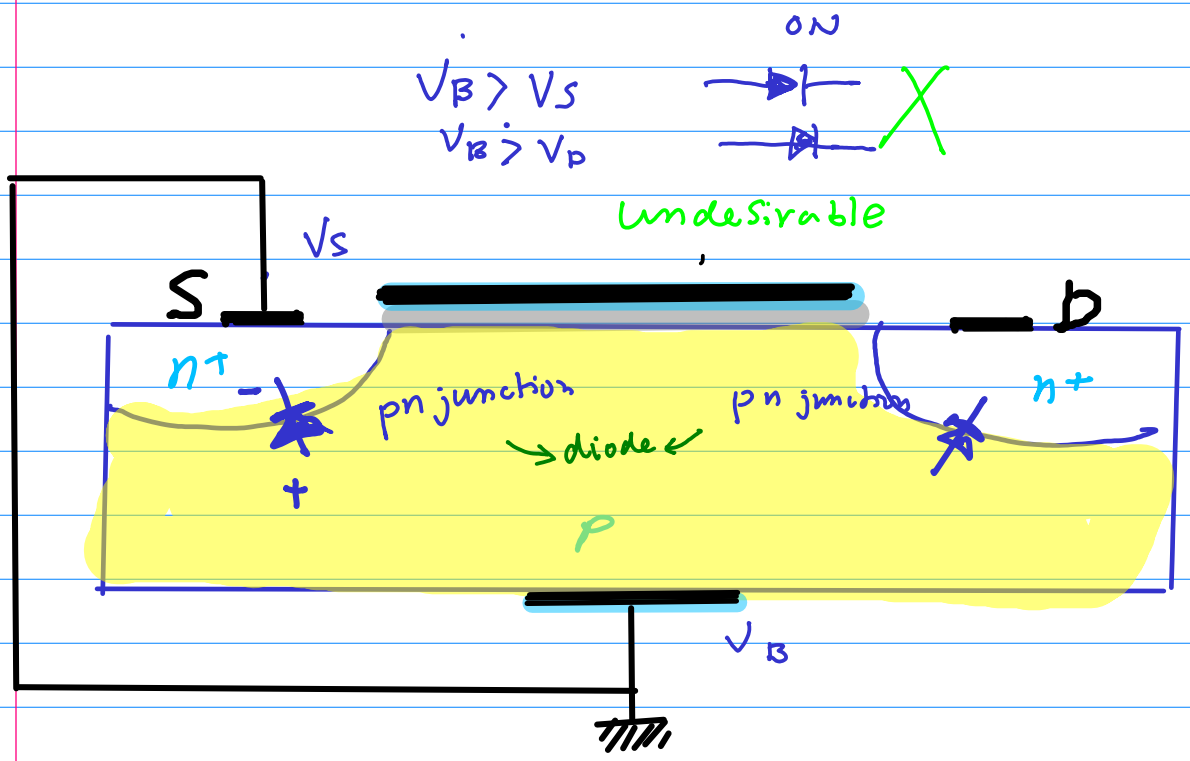
Substrate (B)

physical connection

body

bulk

Pn junction

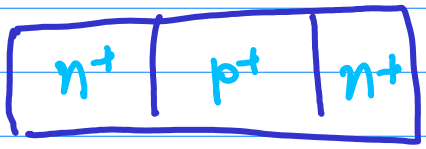


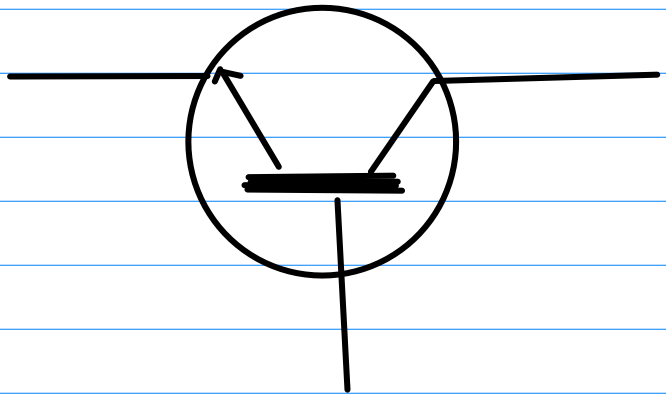
physical connection S–B

→ $V_B = V_S$

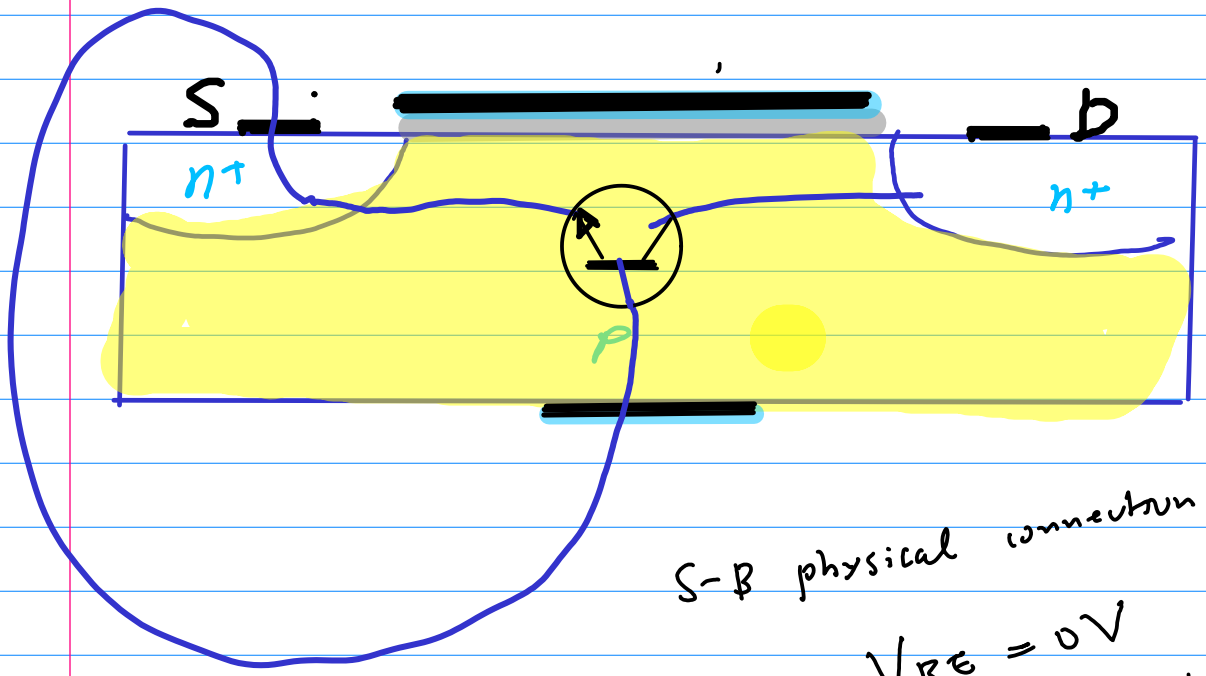
same potential

$V_B = V_S$ OFF





Embedded BJT



S-B physical connection → same voltage

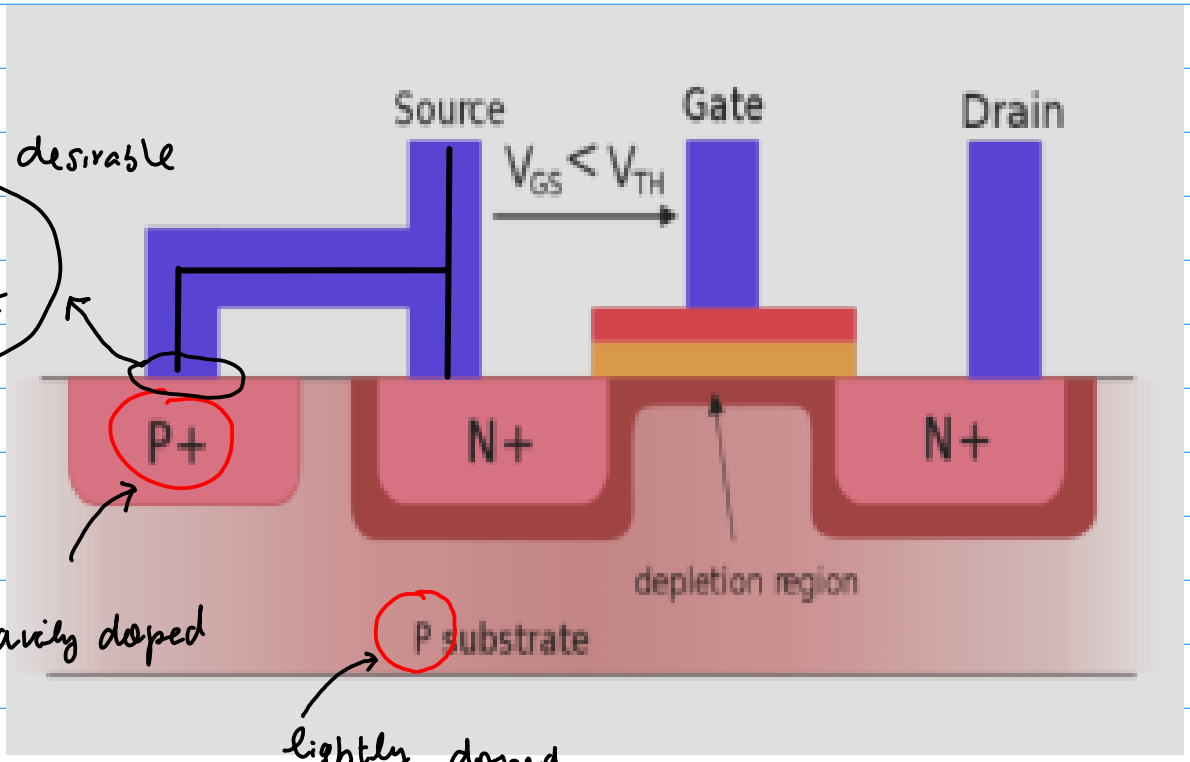
$V_{BE} = 0V$

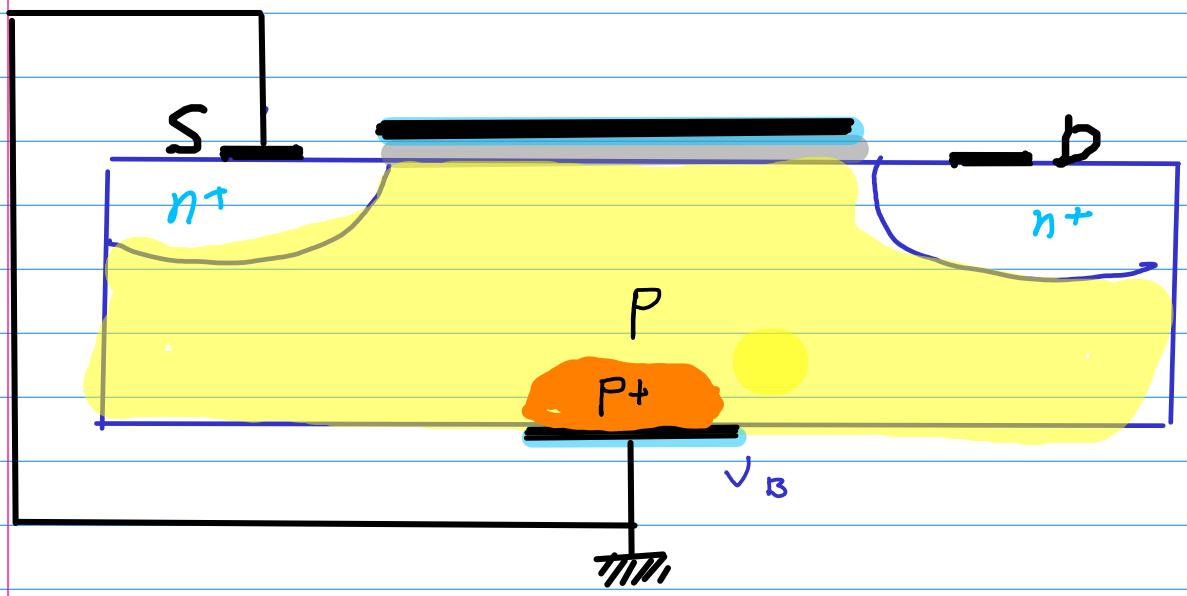
(Base, emitter)

⇒ turns off the embedded BJT

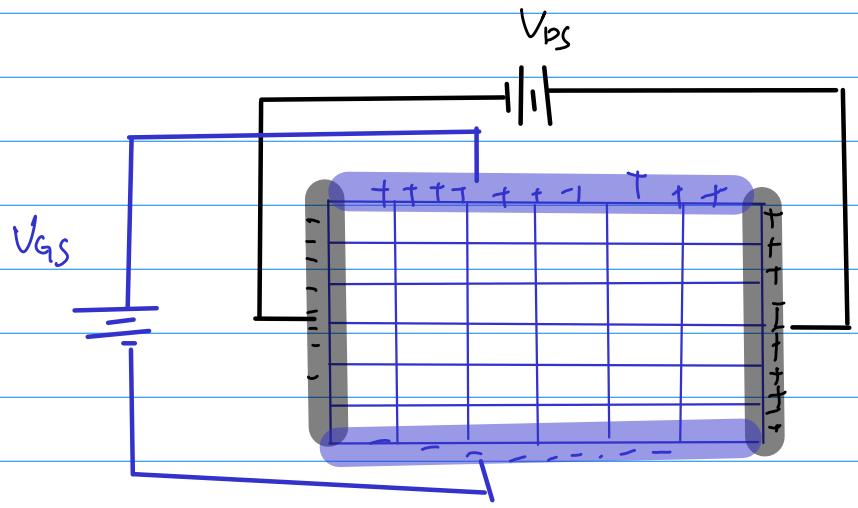
⇒ no drain current

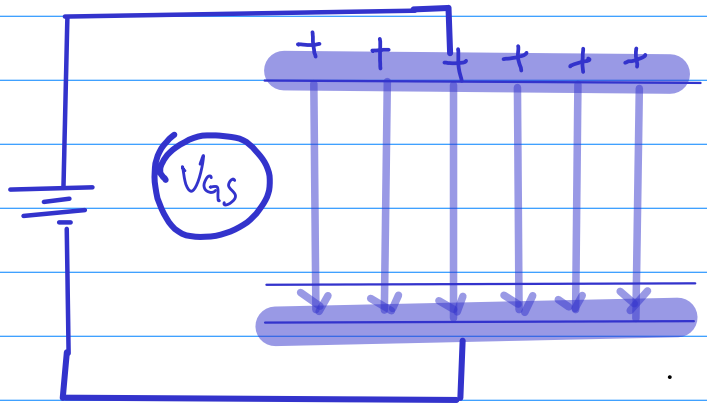
Substrate Tab





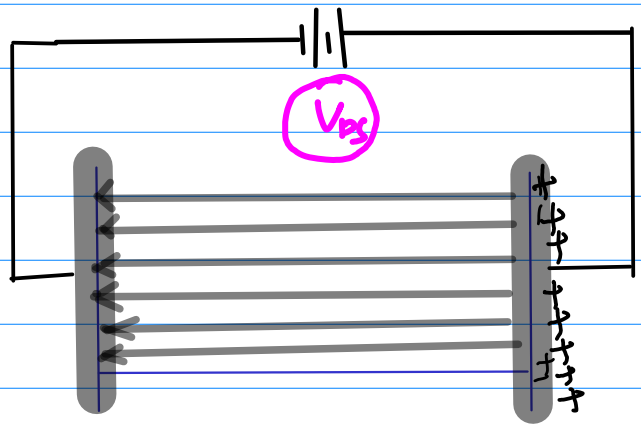
Horizontal & Vertical Bias



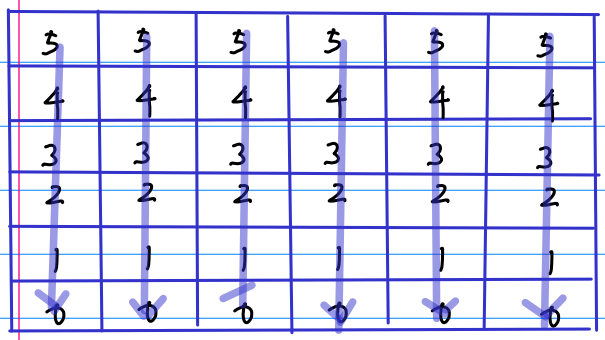


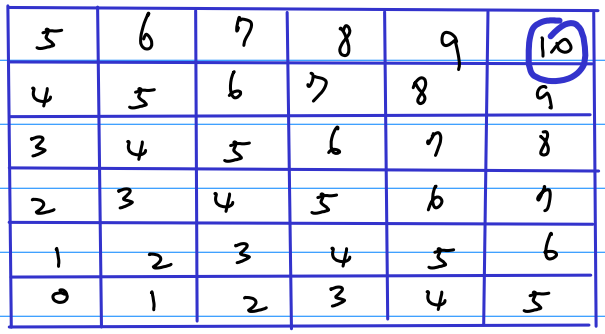
Vertical

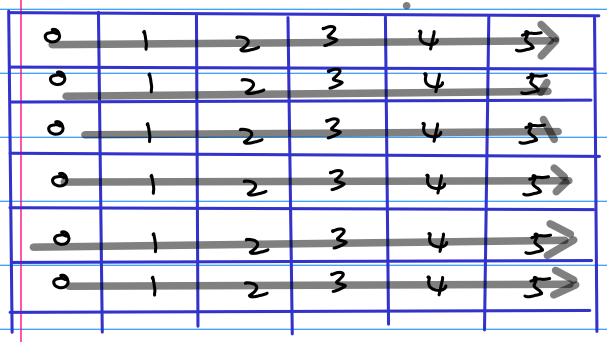
+

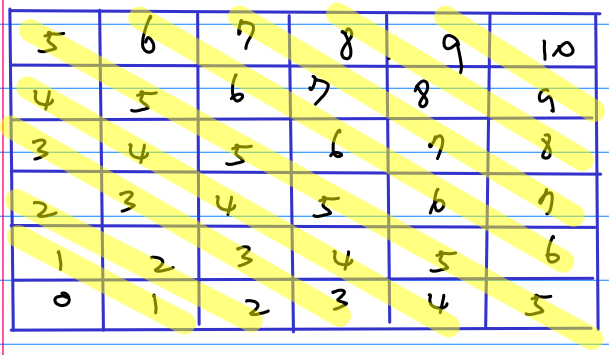


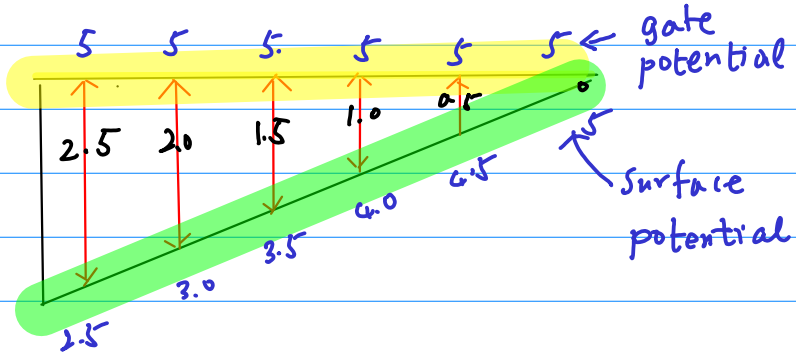
Horizontal



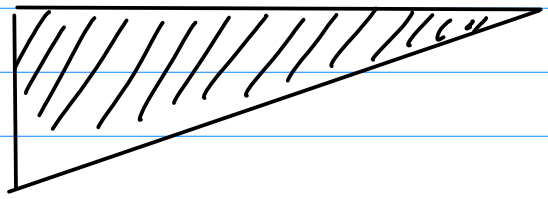




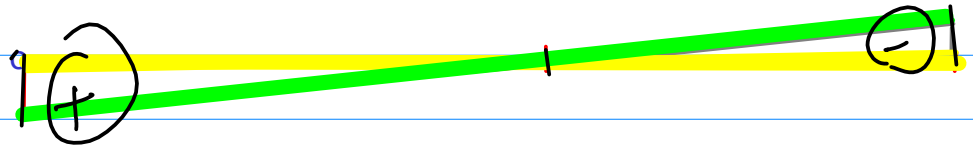




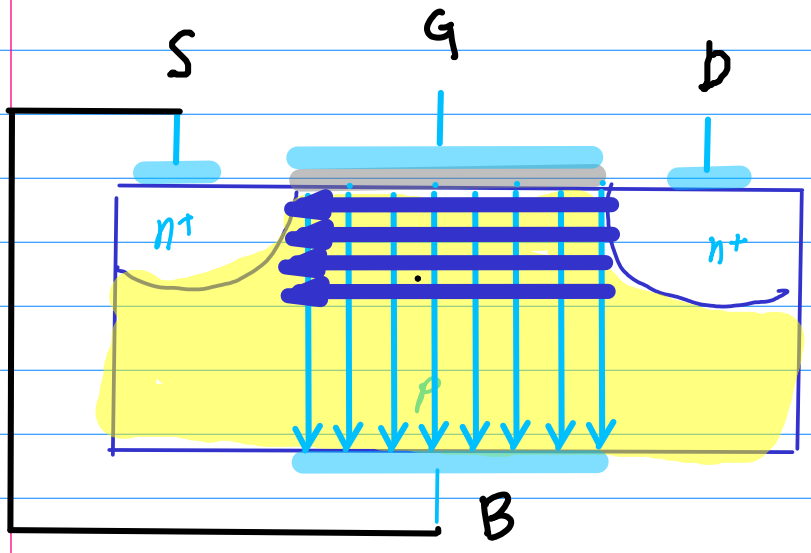
inversion channel shape



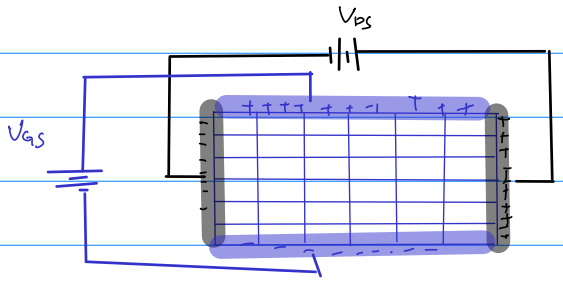
```
octave:16> a
a =

   5   5   5   5   5   5
   4   4   4   4   4   4
   3   3   3   3   3   3
   2   2   2   2   2   2
   1   1   1   1   1   1
   0   0   0   0   0   0

octave:17>
octave:17> b
b =

   0.00000   1.40000   2.80000   4.20000   5.60000   7.00000
   0.00000   1.40000   2.80000   4.20000   5.60000   7.00000
   0.00000   1.40000   2.80000   4.20000   5.60000   7.00000
   0.00000   1.40000   2.80000   4.20000   5.60000   7.00000
   0.00000   1.40000   2.80000   4.20000   5.60000   7.00000
   0.00000   1.40000   2.80000   4.20000   5.60000   7.00000

octave:18> c
c =

   5.00000   6.40000   7.80000   9.20000  10.60000  12.00000
   4.00000   5.40000   6.80000   8.20000   9.60000  11.00000
   3.00000   4.40000   5.80000   7.20000   8.60000  10.00000
   2.00000   3.40000   4.80000   6.20000   7.60000   9.00000
   1.00000   2.40000   3.80000   5.20000   6.60000   8.00000
   0.00000   1.40000   2.80000   4.20000   5.60000   7.00000

octave:19> d
d =

   2.91667   3.73333   4.55000   5.36667   6.18333   7.00000
   2.33333   3.15000   3.96667   4.78333   5.60000   6.41667
   1.75000   2.56667   3.38333   4.20000   5.01667   5.83333
   1.16667   1.98333   2.80000   3.61667   4.43333   5.25000
   0.58333   1.40000   2.21667   3.03333   3.85000   4.66667
   0.00000   0.81667   1.63333   2.45000   3.26667   4.08333
```

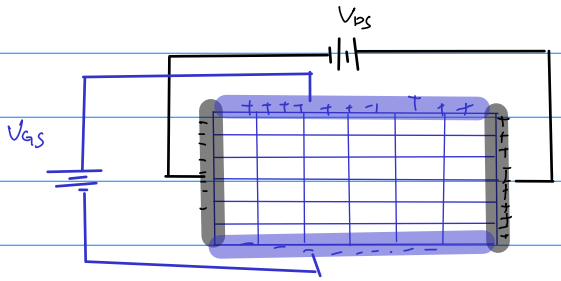


Channel → Inversion Layer



Electric Field
- Horizontal V_{DS}
- Vertical V_{GS}



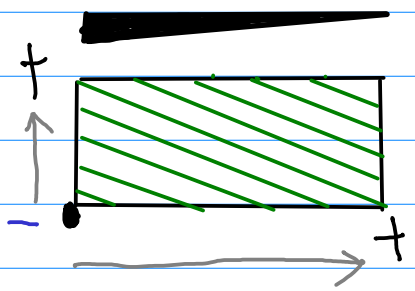


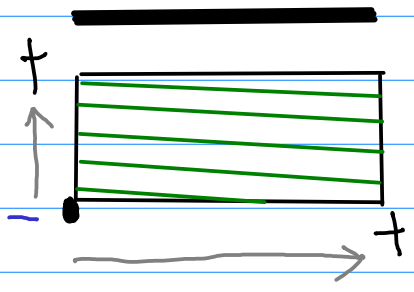
Inversion

Inversion

inverted Channel

equipotential lines

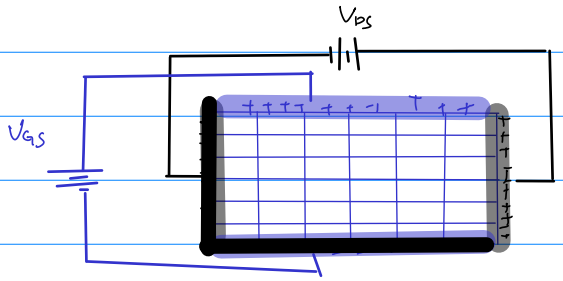


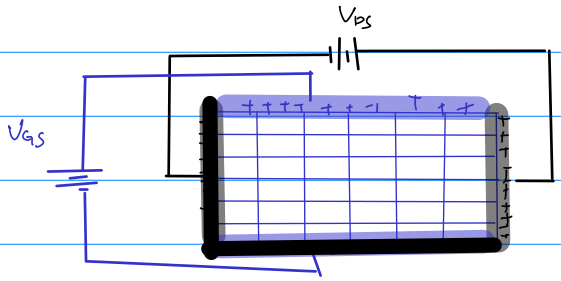


$V_t < V_{GS}$

$V_t < V_{GS}$

V_{DS} Bias





Inversion

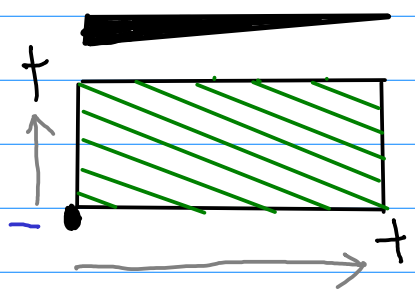
$V_t < V_{GS}$

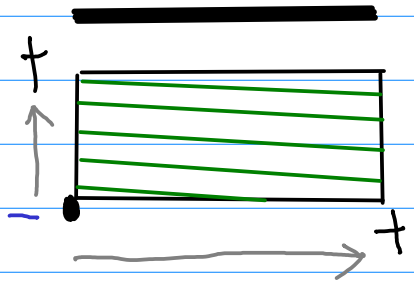
Inversion

$V_t < V_{GS}$

inverted channel

equipotential lines





SAT

$V_{GD} < V_t$

LIN

$V_t < V_{GD}$

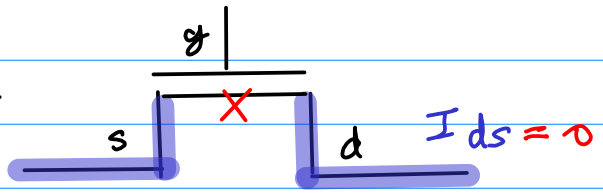
$V_{DS} > V_{GS} - V_t$

$V_{DS} < V_{GS} - V_t$

Operation Modes

$V_{gs} < V_t$

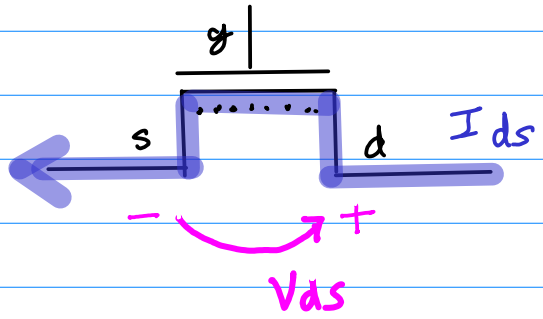
no channel



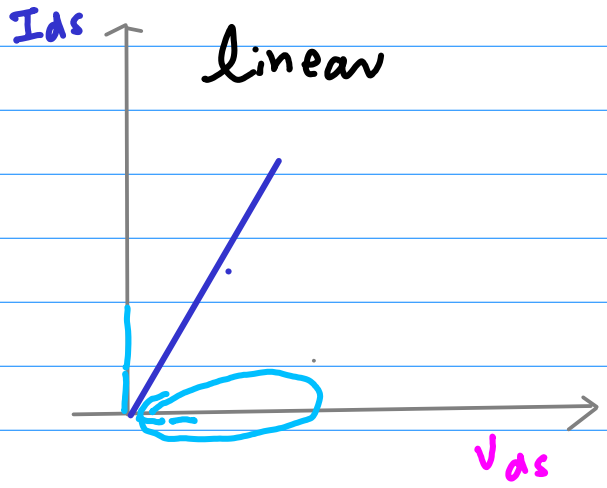
- Cut off

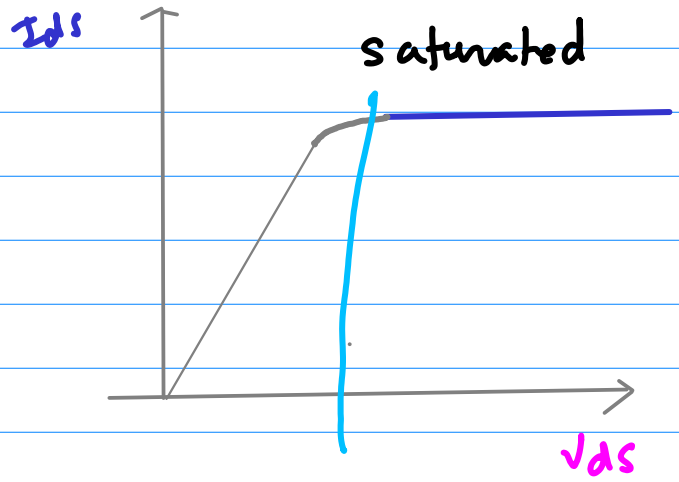
$V_{gs} > V_t$

inversion



- linear
- saturated



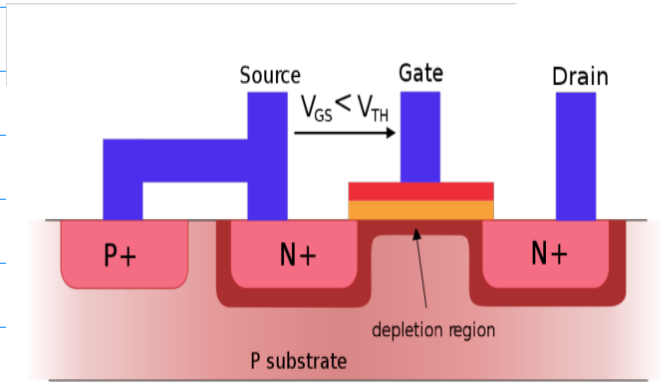


Current I_{ds} increases linearly with increasing V_{ds}

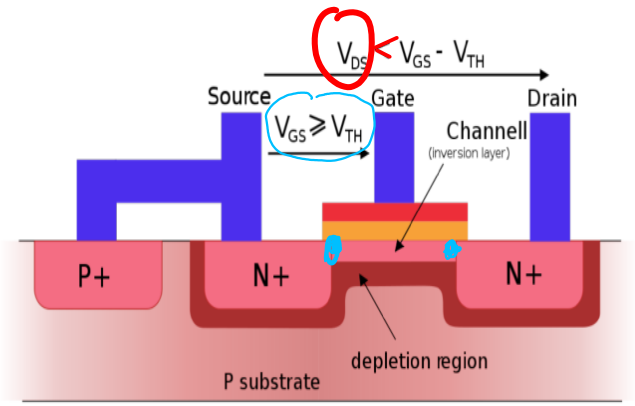
Current I_{ds} increases no more with increasing V_{ds}

Saturated

$V_{GS} < V_T$

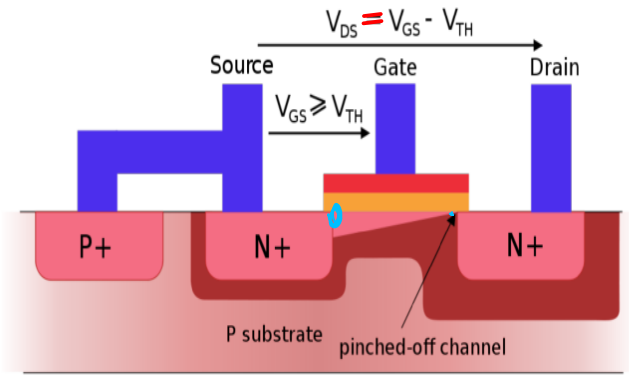


$V_{GS} \geq V_T$

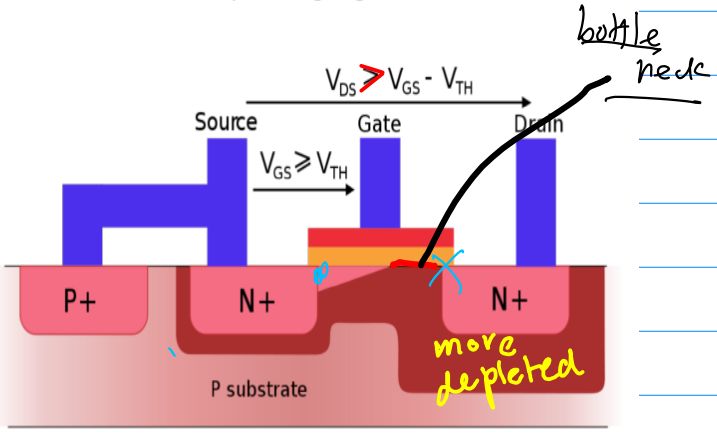


Linear operating region (ohmic mode)

$V_{GS} \geq V_T$

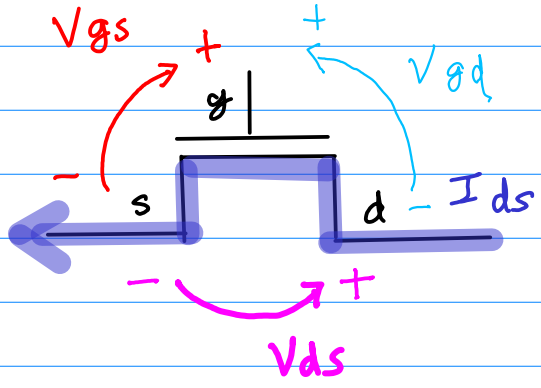


Saturation mode at point of pinch-off

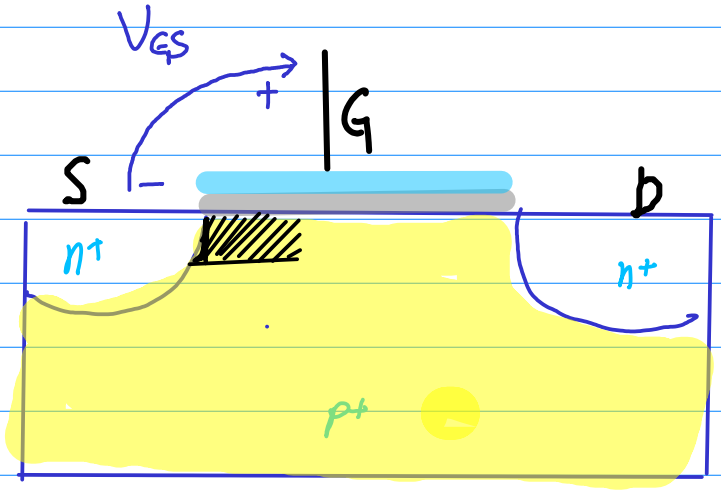


Saturation mode

①	$V_{DS} < V_{GS} - V_T$	$\Leftrightarrow$ $V_T < V_{GS} - V_{DS}$	$\Leftrightarrow$ $V_T < V_{GD}$
②	$V_{DS} = V_{GS} - V_T$	$\Leftrightarrow$ $V_T = V_{GS} - V_{DS}$	$\Leftrightarrow$ $V_T = V_{GD}$
③	$V_{DS} > V_{GS} - V_T$	$\Leftrightarrow$ $V_T > V_{GS} - V_{DS}$	$\Leftrightarrow$ $V_T > V_{GD}$

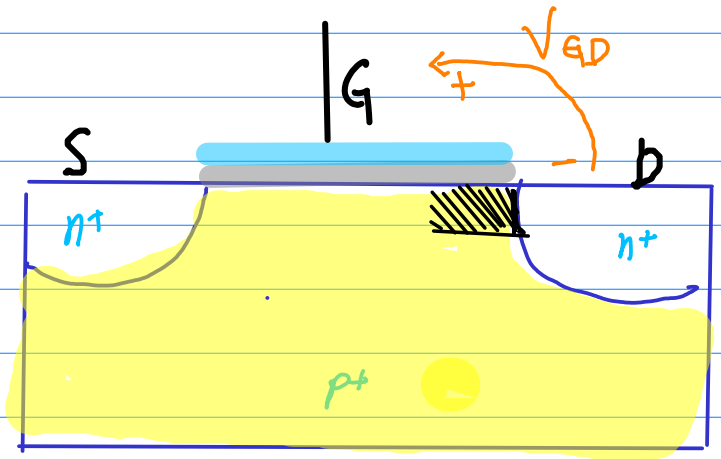


Channel Existence Conditions



$V_{GS} > V_t$

existence of a channel at the (S) side



$V_{GD} > V_t$

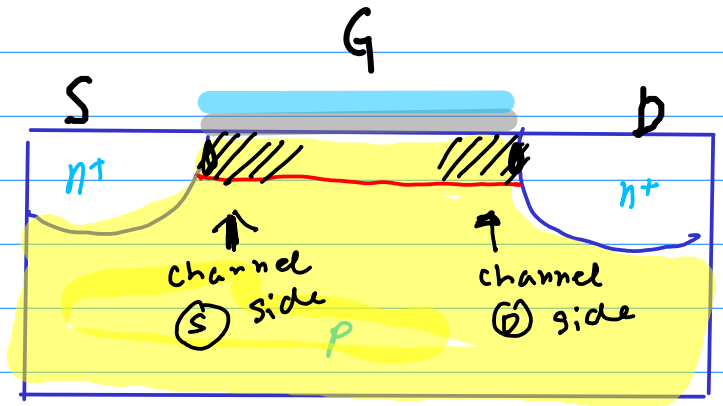
existence of a channel at the (D) side

$$V_{GD} = V_{GS} - V_{DS} > V_t$$

$$V_{GS} - V_t > V_{DS}$$

$$V_{GD} > V_t \iff V_{DS} < V_{GS} - V_t$$

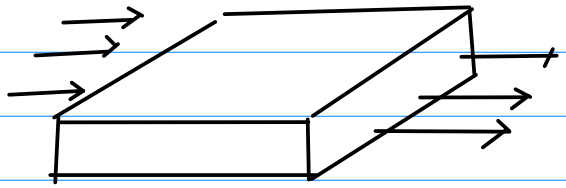
Linear



$V_{GS} > V_t$

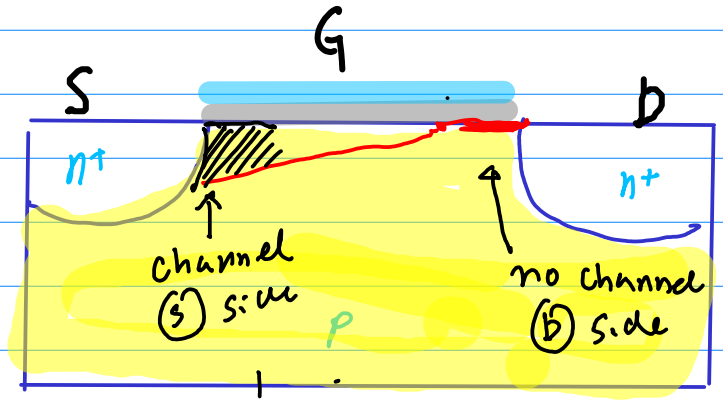
$V_{GD} > V_t$

$V_{DS} < V_{GS} - V_t$



Resistor

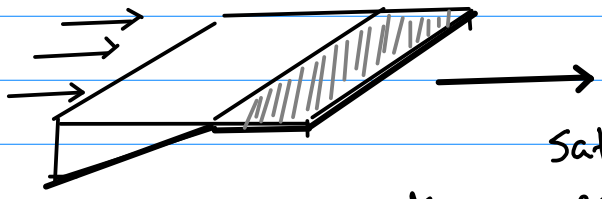
Saturation



$V_{GS} > V_t$

$V_{GD} < V_t$

$V_{DS} > V_{GS} - V_t$



Saturated current

bottleneck

→ constant current.

References

Some Figures from the following sites

[1] http://pages.hmc.edu/harris/cmosvlsi/4e/index.html
Weste & Harris Book Site

[2] en.wikipedia.org