CMOS Inverter (H.3)

20151218

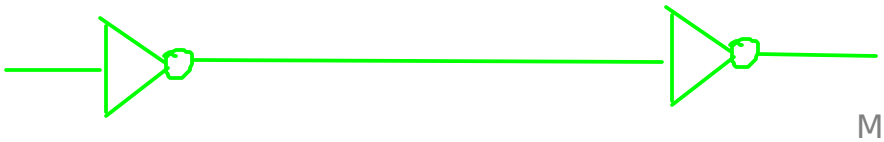
Inverter Fall Delay
Inverter Rise Delay
Inverter Propagation Delay
Inverter Gate Delay

References

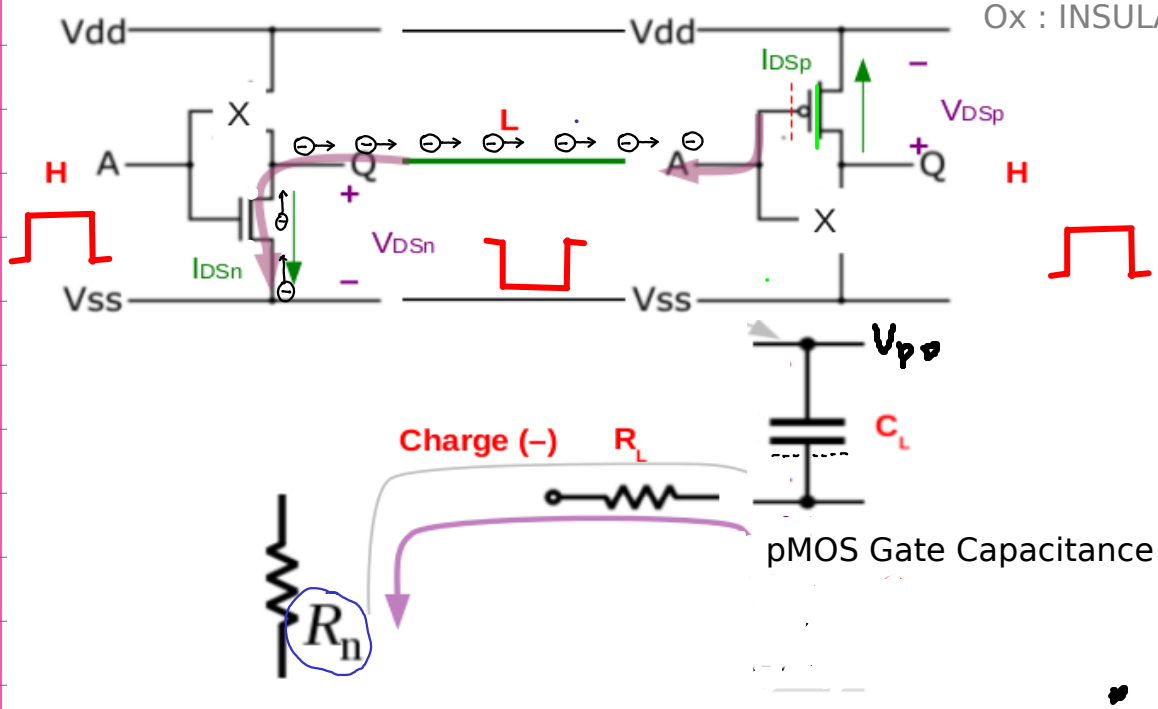
Some Figures from the following sites

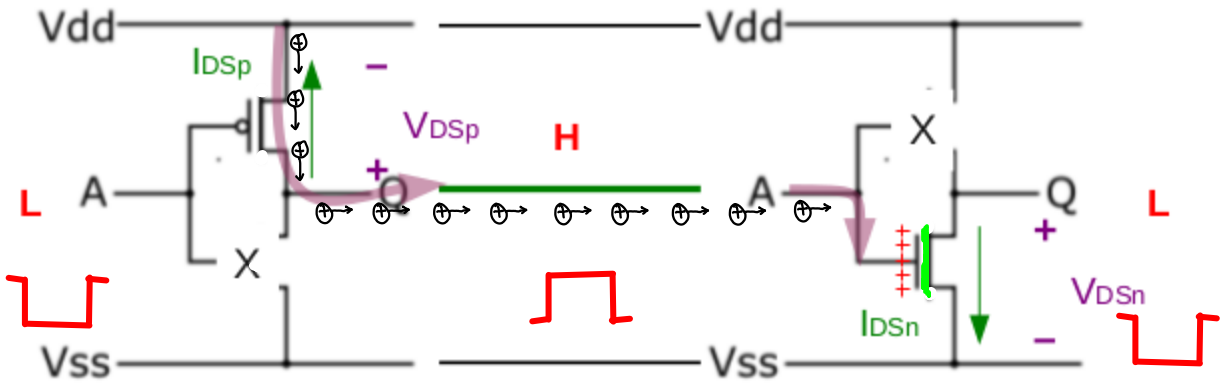
[1] http://pages.hmc.edu/harris/cmosvlsi/4e/index.html
Weste & Harris Book Site

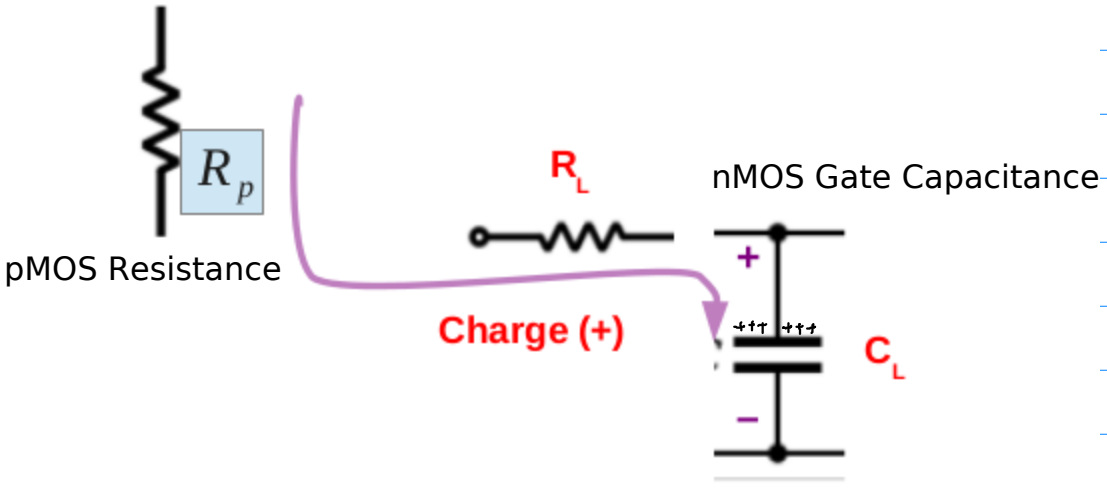
[2] en.wikipedia.org



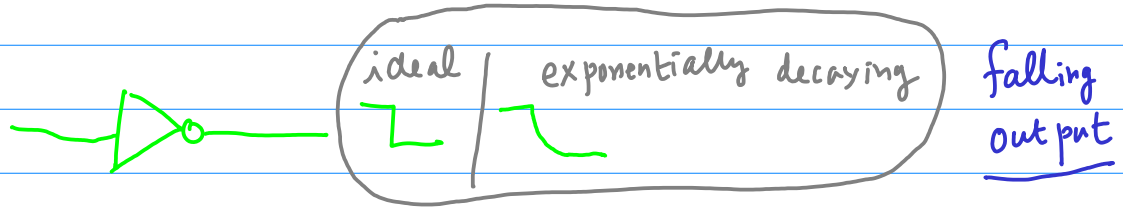
Metal-Oxide-Semiconductor
Ox : INSULATOR

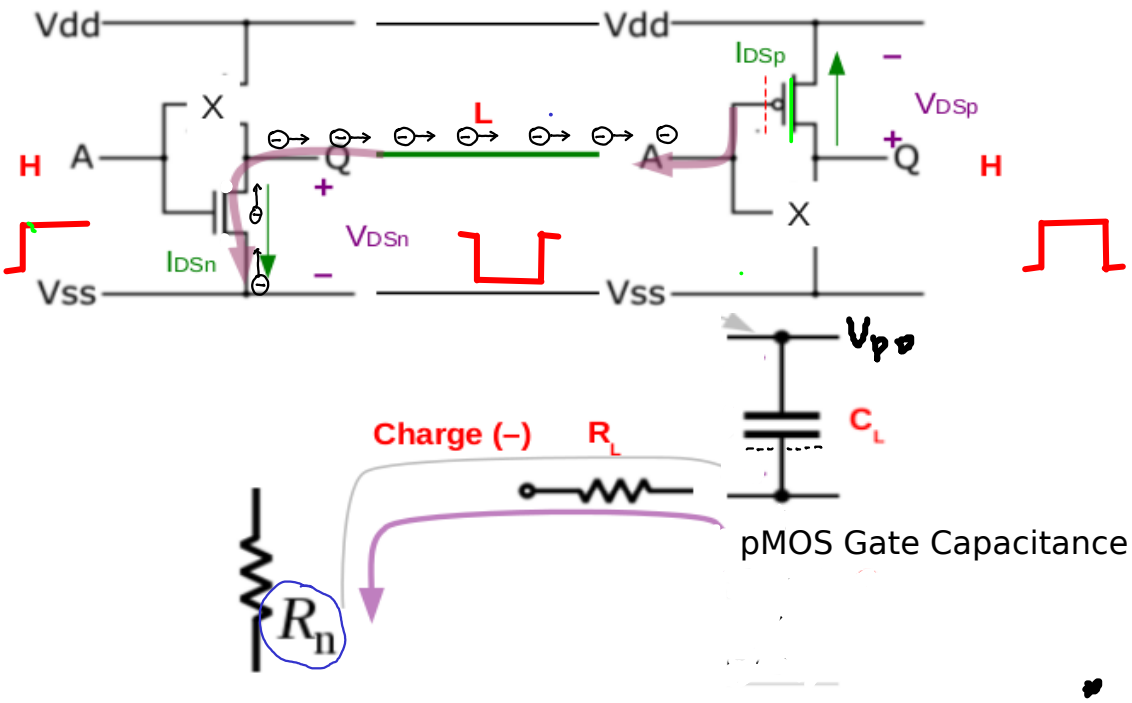


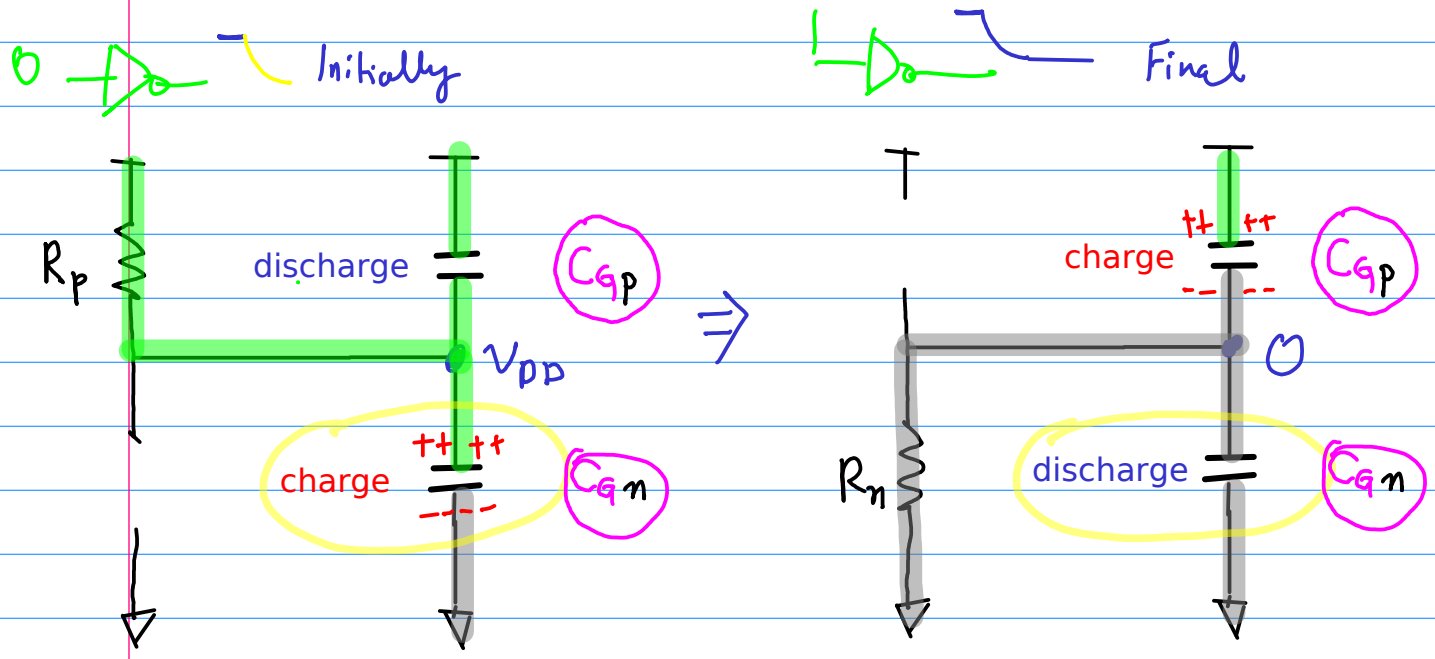




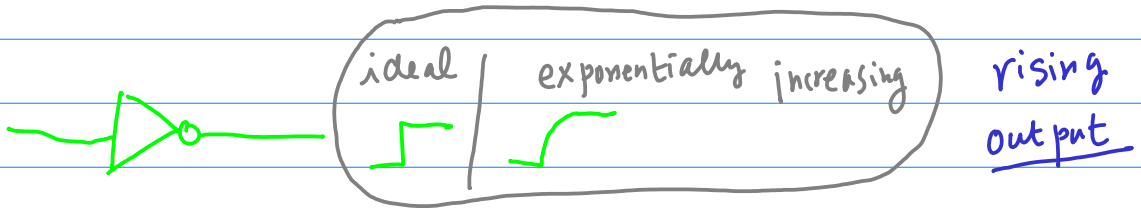
Fall Time

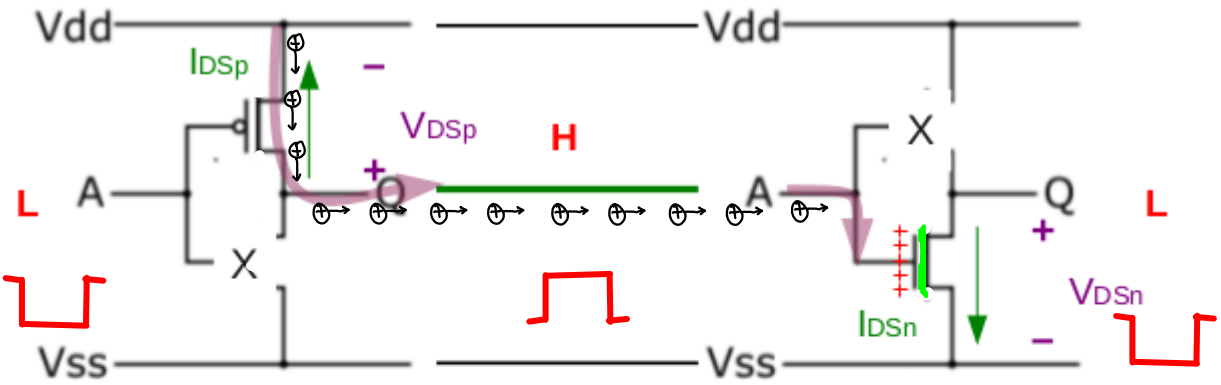

ideal
exponentially decaying
falling output

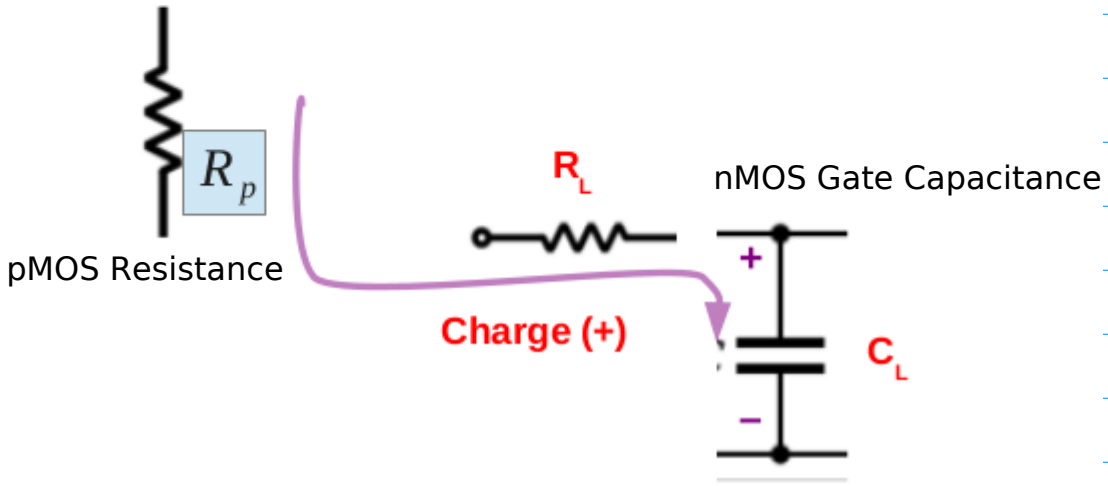

Vdd
Vdd
IDSp
VDSp
X
L
H
A
Q
A
Q
H
X
VDSn
IDSn
Vss
Vss
Vpp
CL
Charge (–)
RL
Rn
pMOS Gate Capacitance
nMOS Resistance

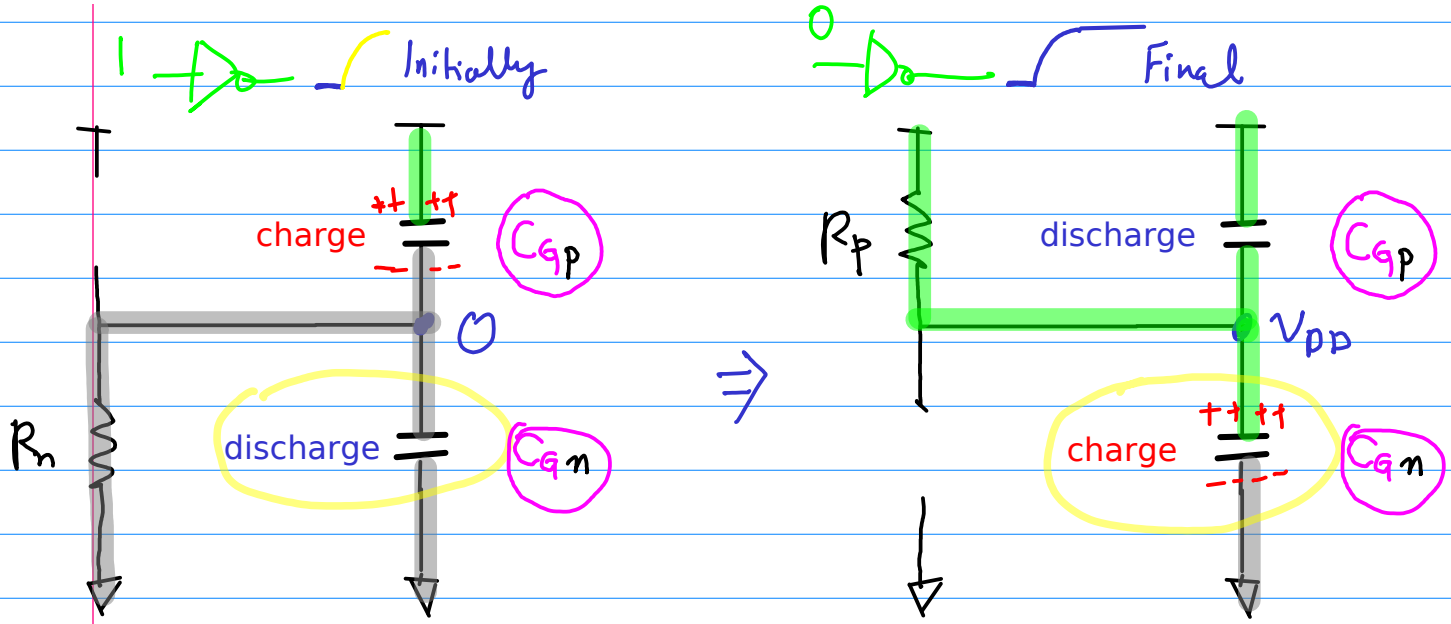

Initially
Final
Rp
discharge
Cgp
Vpp
charge
Cgn
charge
Cgp
Rn
discharge
Cgn

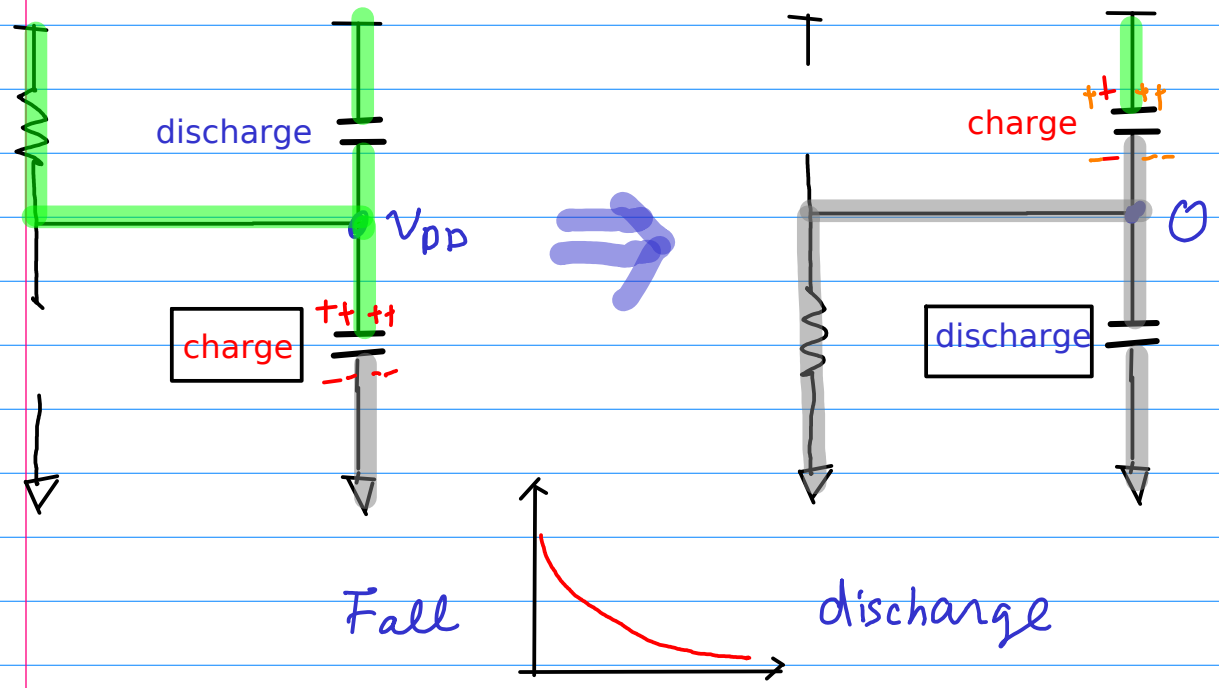
Rise Time


ideal
exponentially increasing
rising output


Vdd
Vdd
IDSp
VDSp
H
L
A
X
Q
A
X
Q
L
VDSn
IDSn
Vss
Vss

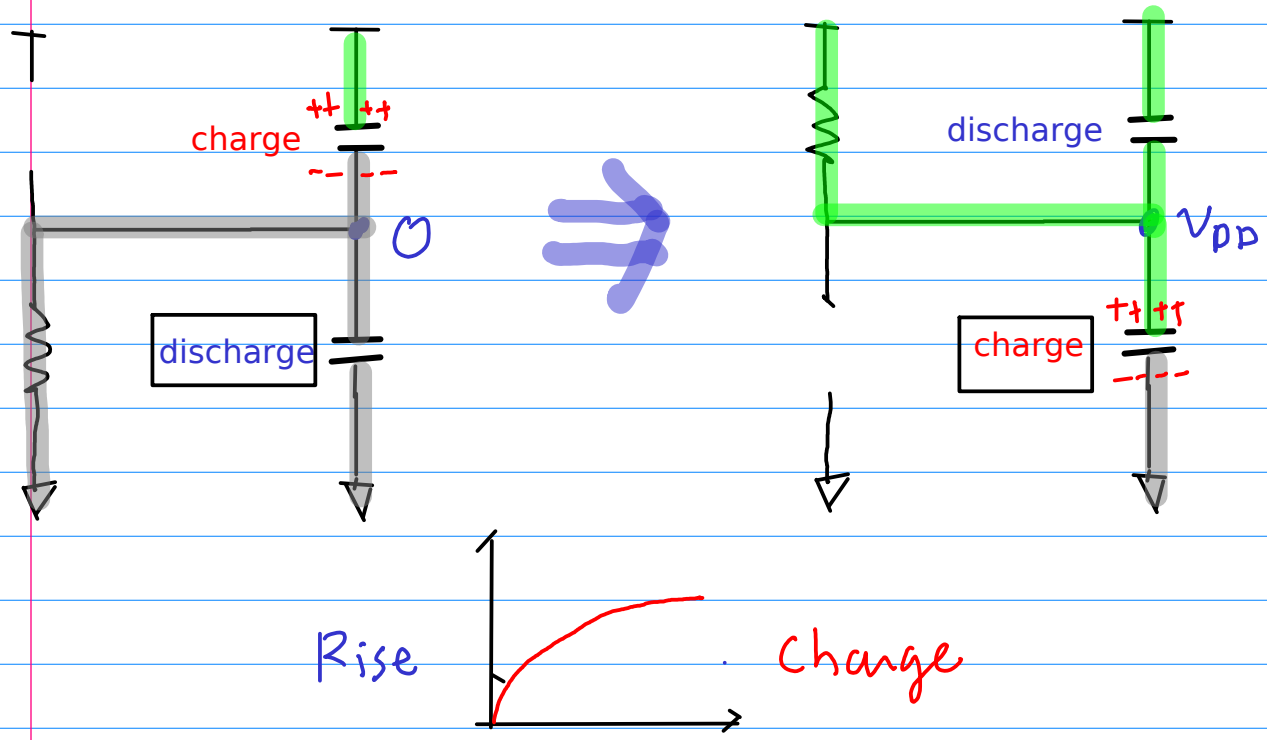

R_p
pMOS Resistance
R_L
nMOS Gate Capacitance
Charge (+)
C_L


1
Initially
0
Final
charge
C_{gp}
discharge
C_{gn}
R_n
R_p
discharge
C_{gp}
V_{DD}
charge
C_{gn}



Fall

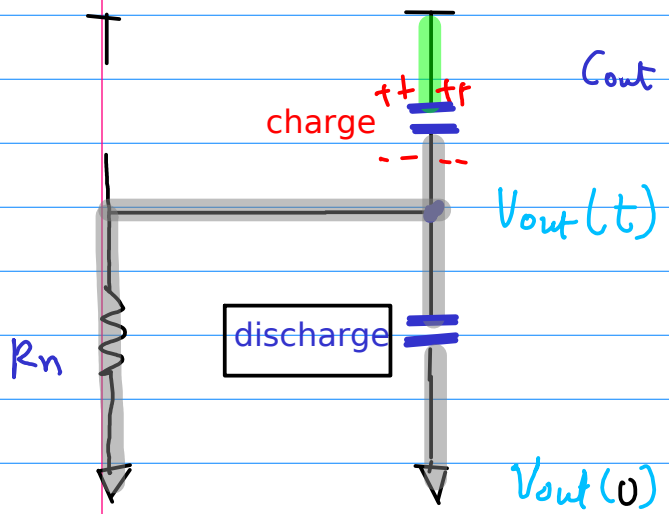
discharge

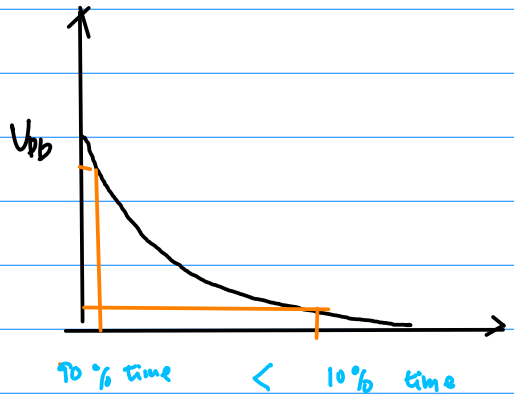


Rise

Charge

Fall Time





$V_{out}(0) = V_{DD}$

$$i = -C_{out}\frac{dV_{out}}{dt} = \frac{V_{out}}{R_n}$$

$$V_{out}(t) = V_{DD}\, e^{-t/\tau_n} \qquad \boxed{\tau_n = R_n C_{out}}$$

$$\frac{V_{out}}{V_{DD}} = e^{-t/\tau_n} \qquad t = -\tau_n \ln\left(\frac{V_{out}}{V_{DD}}\right)$$

$$= \tau_n \ln\left(\frac{V_{DD}}{V_{out}}\right)$$

$$t_f = t_{time}(10\%) - t_{time}(90\%)$$

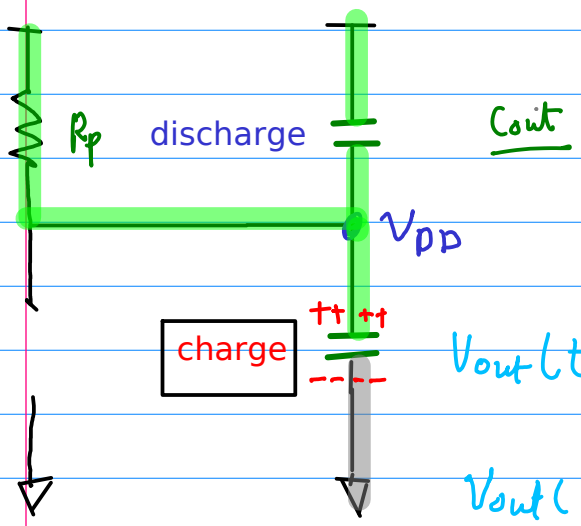
$$= \tau_n \ln\left(\frac{V_{DD}}{0.1 V_{DD}}\right) - \tau_n \ln\left(\frac{V_{DD}}{0.9 V_{DD}}\right)$$

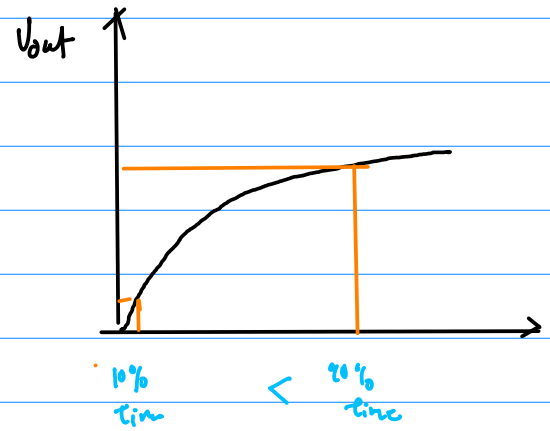
$$= \tau_n \left(\ln(10) - \ln\left(\frac{10}{9}\right)\right) = \tau_n \ln\left(10 \cdot \frac{9}{10}\right)$$

$$= \tau_n \ln(9)$$

$$\boxed{t_f = 2.2\,\tau_n} = 2.2\, R_n C_{out}$$

Rise Time





$$i = -C_{out}\frac{dV_{out}}{dt} = \frac{V_{DD} - V_{out}}{R_n}$$

$$V_{out}(t) = V_{DD}\left(1 - e^{-t/\tau_p}\right) \qquad \boxed{\tau_p = R_p C_{out}}$$

$$\frac{V_{out}}{V_{DD}} = 1 - e^{-t/\tau_p} \qquad t = -\tau_p \ln\left(1 - \frac{V_{out}}{V_{DD}}\right)$$

$$= \tau_p \ln\left(\frac{V_{DD}}{V_{DD} - V_{out}}\right)$$

$$t_r = t_{time}(90\%) - t_{time}(10\%)$$

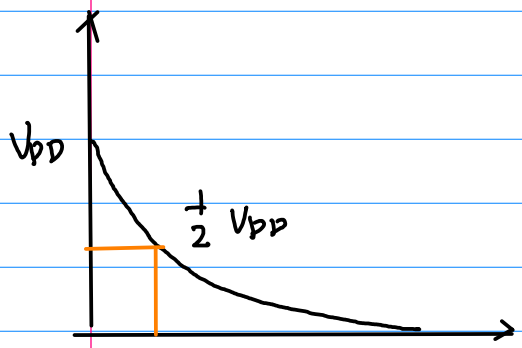
$$= \tau_p \ln\left(\frac{V_{DD}}{(1-0.9)V_{DD}}\right) - \tau_p \ln\left(\frac{V_{DD}}{(1-0.1)V_{DD}}\right)$$

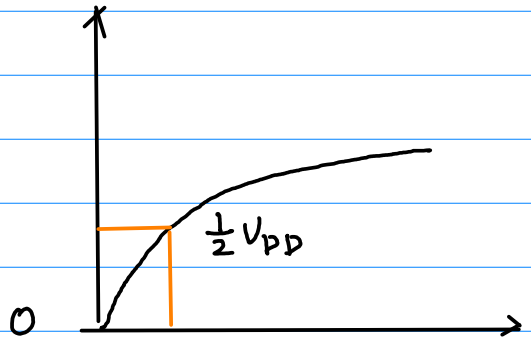
$$= \tau_p \left(\ln(10) - \ln\left(\frac{10}{9}\right)\right) = \tau_p \ln\left(10 \cdot \frac{9}{10}\right)$$

$$= \tau_p \ln(9)$$

$$\boxed{t_r = 2.2\,\tau_p}$$

Propagation Delay





$$V_{out}(t) = V_{DD} e^{-t/\tau_n}$$

$$\frac{V_{out}}{V_{DD}} = e^{-t/\tau_n}$$

$$t = \tau_n \ln\left(\frac{V_{DD}}{V_{out}}\right)$$

$$= \tau_n \ln\left(\frac{V_{DD}}{0.5 V_{DD}}\right)$$

$$t_{pf} = \tau_n \ln(2)$$

$$V_{out}(t) = V_{DD}\left(1 - e^{-t/\tau_p}\right)$$

$$\frac{V_{out}}{V_{DD}} = 1 - e^{-t/\tau_p}$$

$$t = \tau_p \ln\left(\frac{V_{DD}}{V_{DD} - V_{out}}\right)$$

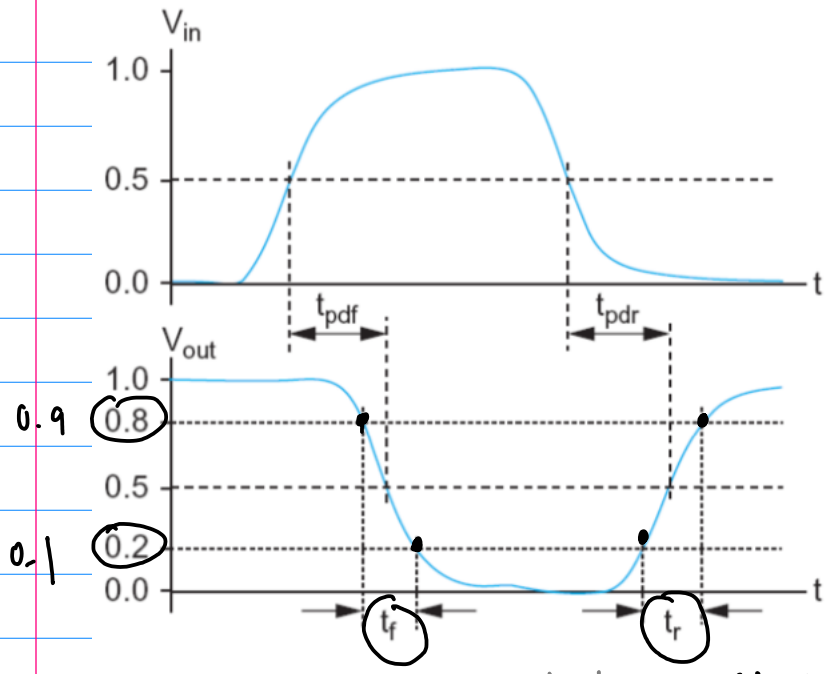
$$= \tau_p \ln\left(\frac{V_{DD}}{0.5 V_{DD}}\right)$$

$$t_{pr} = \tau_p \ln(2)$$

$$t_p = \frac{1}{2}\left(t_{pf} + t_{pr}\right) = 0.35\left(\tau_n + \tau_p\right)$$

$$\tau_n = R_n C_{out}$$

$$\tau_p = R_p C_{out}$$

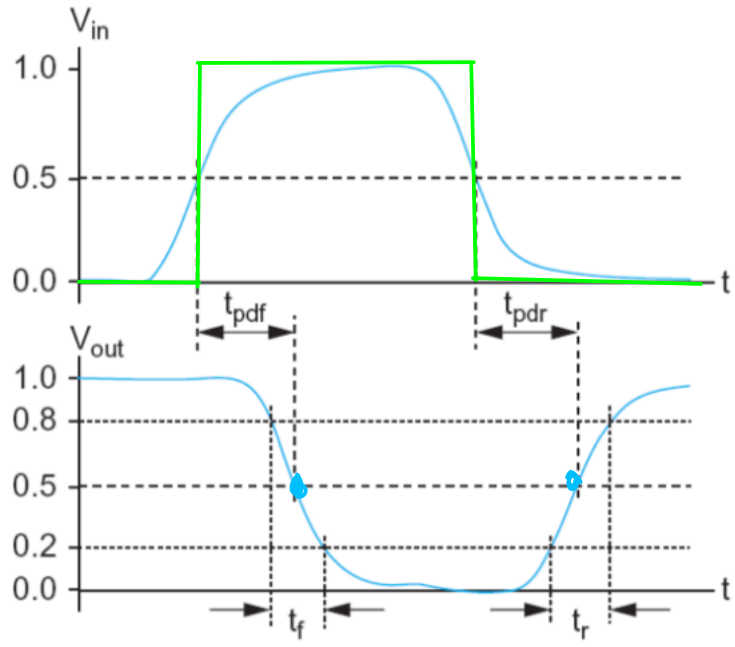


output fall time

output rise time

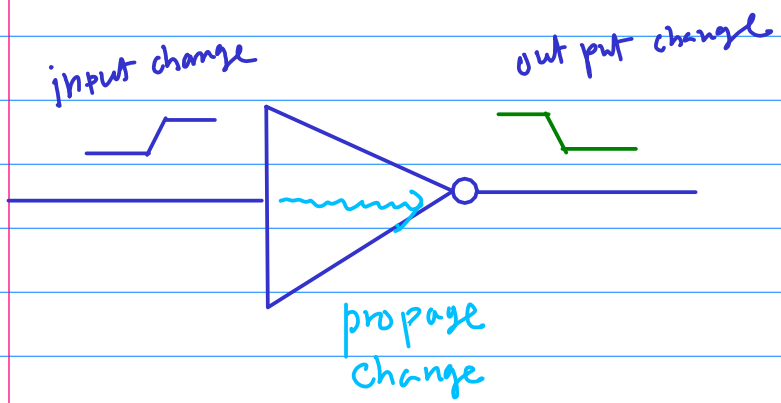
$$t_f = 2.2\,\tau_n$$

$$t_r = 2.2\,\tau_p$$



$$t_f = 2.2\,\tau_n$$

$$t_r = 2.2\,\tau_p$$



to estimate the reaction
delay time from input to output

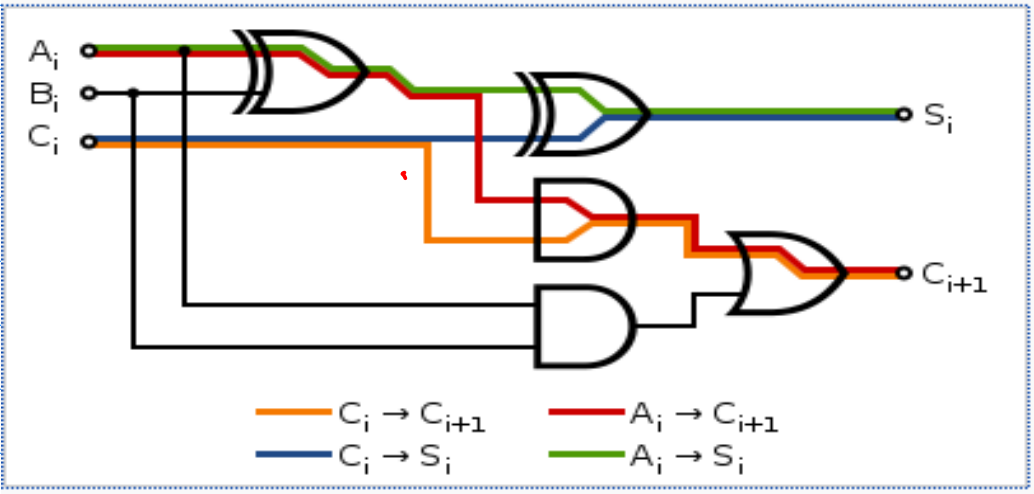
if input is ideal square shape,

$$t_p = \frac{1}{2}(t_{pf} + t_{pr}) = 0.35(\tau_n + \tau_p)$$

$$\tau_n = R_n C_{out}$$

$$\tau_p = R_p C_{out}$$

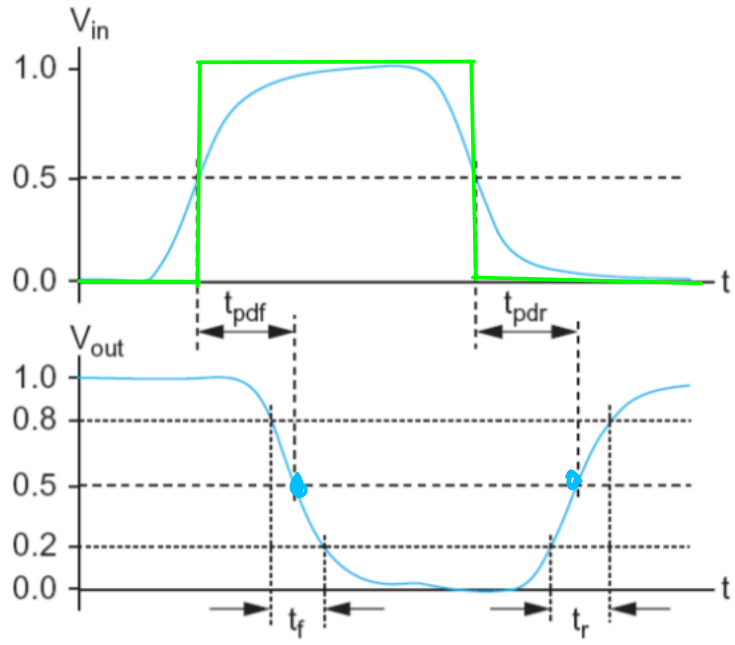
Gate Delay in RTL Simulation



A full adder has an overall gate delay of 3 logic gates from the inputs *A* and *B* to the carry output C_{out} shown in red

In electronics, digital circuits and digital electronics, the propagation delay, or **gate delay**, is the length of time which starts when the input to a logic gate becomes stable and valid to change, to the time that the output of that logic gate is stable and valid to change. Often on manufacturers' datasheets this refers to the time required for the output to reach 50% of its final output level when the input changes to 50% of its final input level. Reducing gate delays in digital circuits allows them to process data at a faster rate and improve overall performance.

wikipedia.org



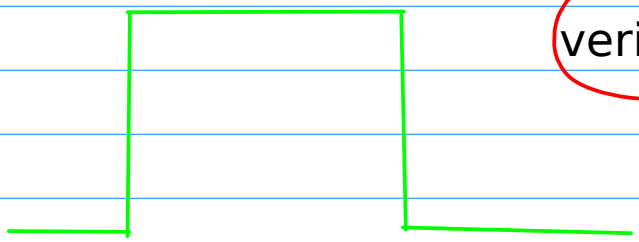
spice simulations

$$t_f = 2.2\,\tau_n$$

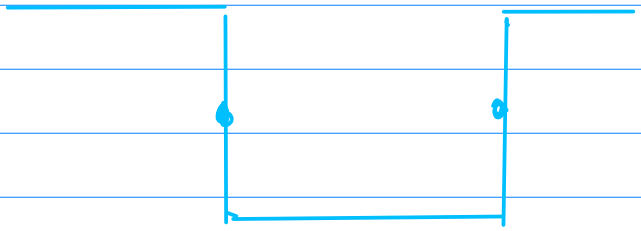
$$t_r = 2.2\,\tau_p$$

SDF (Standard Delay Format)

Annotation



verilog gate level simulations



$$t_f = 2.2\,\tau_n$$

$$t_r = 2.2\,\tau_p$$