CMOS Inverter (H.2)

20160227

nMOS Linear Model
nMOS Resistance
nMOS Capacitance

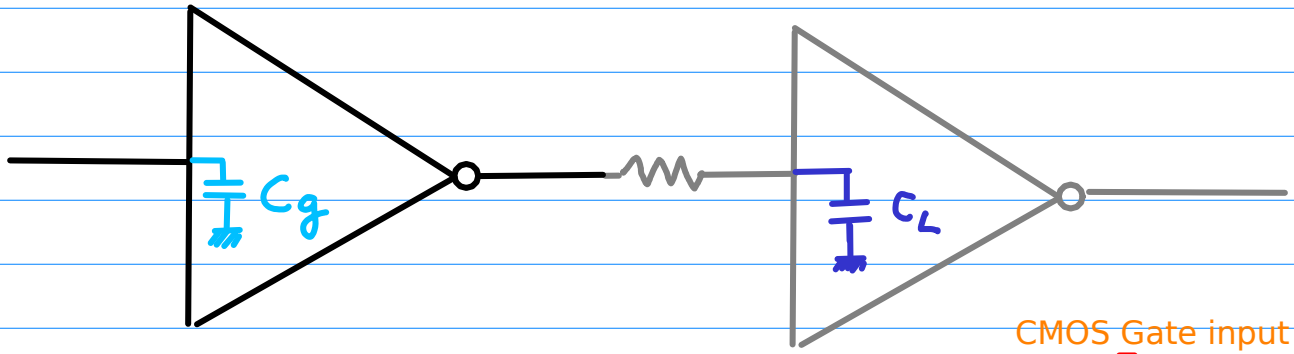
References

Some Figures from the following sites

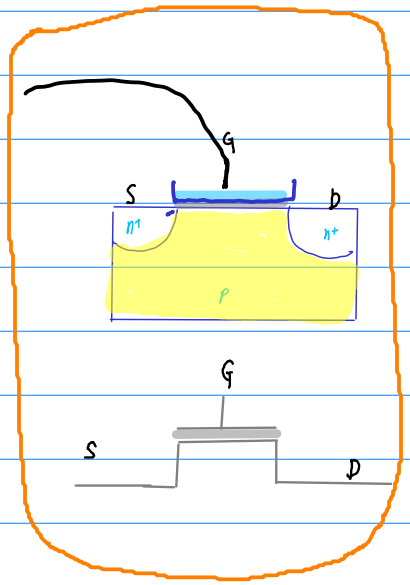
[1] http://pages.hmc.edu/harris/cmosvlsi/4e/index.html
Weste & Harris Book Site

[2] en.wikipedia.org

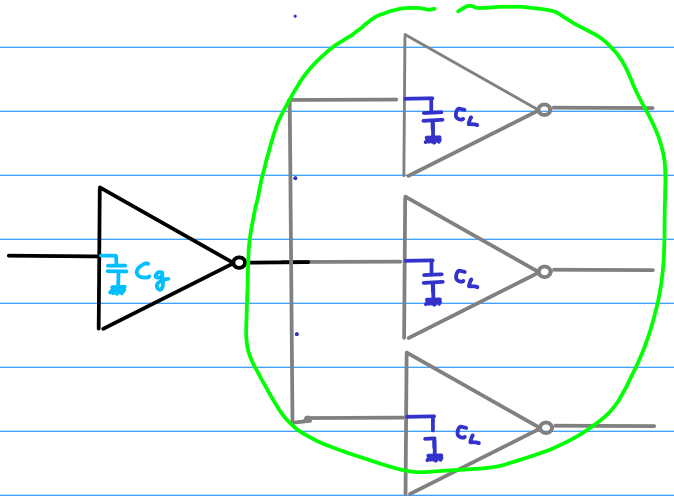
Logic Gate : Inverter



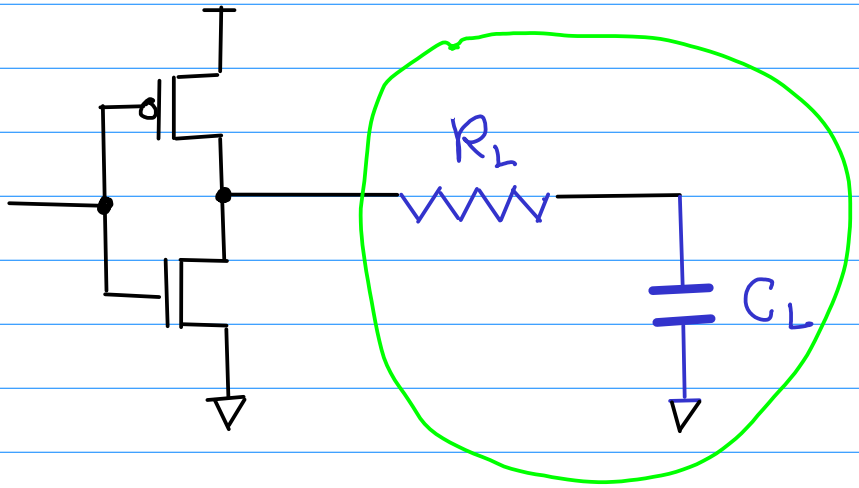
CMOS Gate input

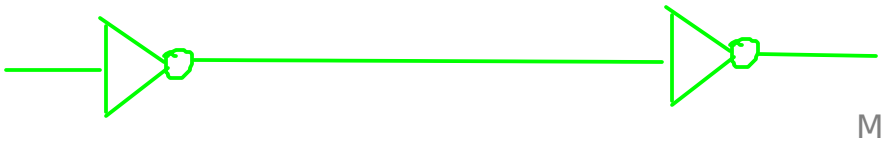


Fan out : 3

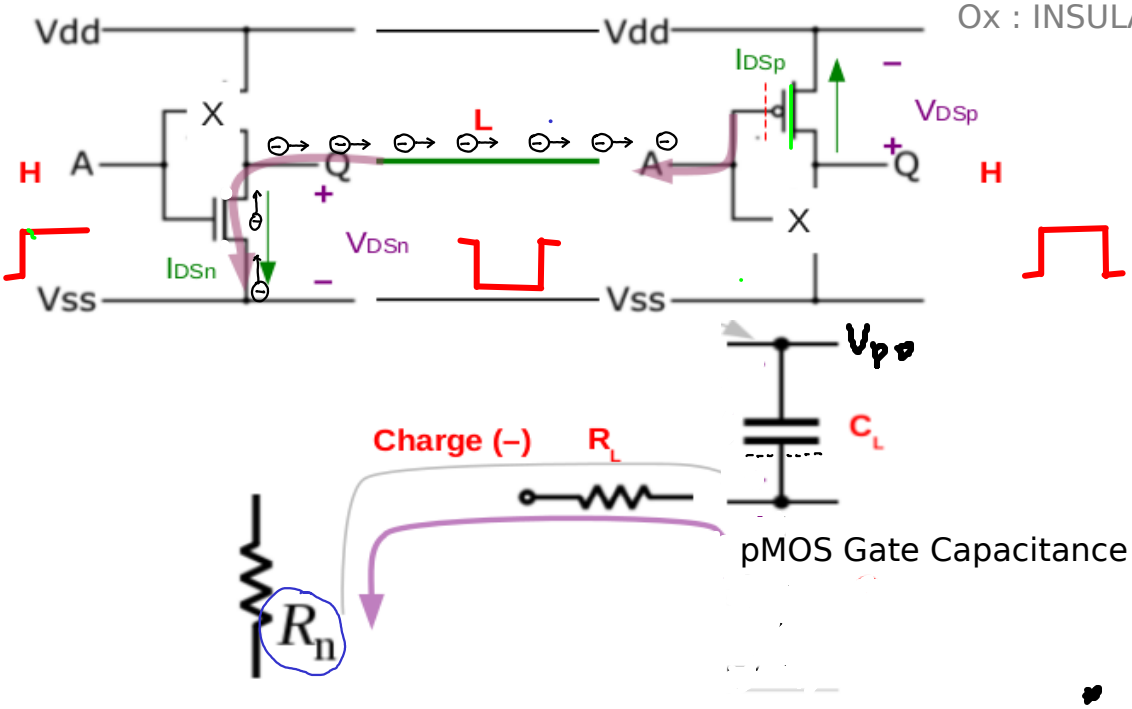


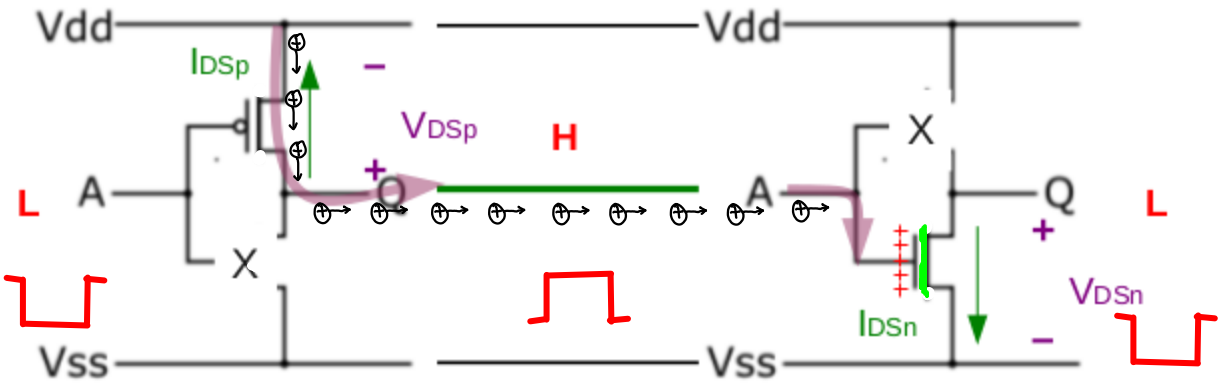
$3C_L$

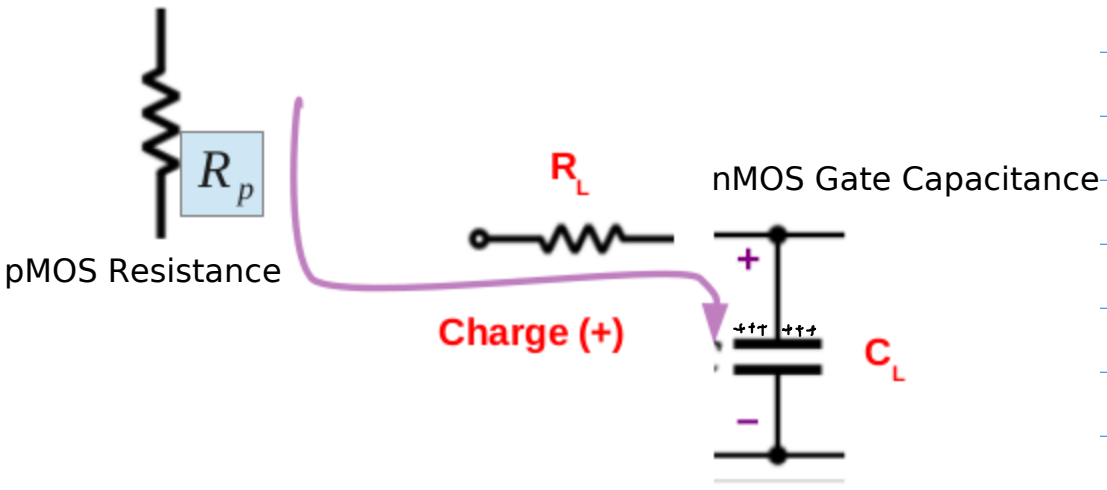


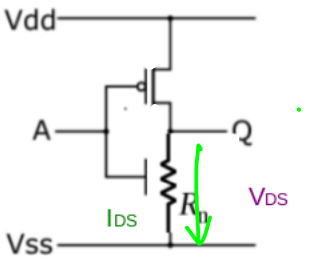


Metal-Oxide-Semiconductor
Ox : INSULATOR

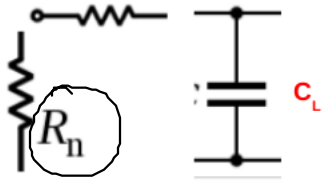


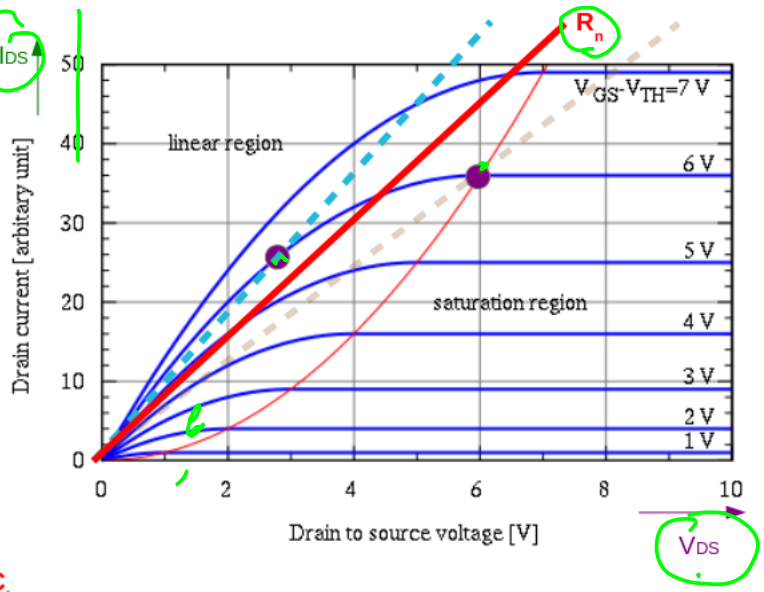






nMOS





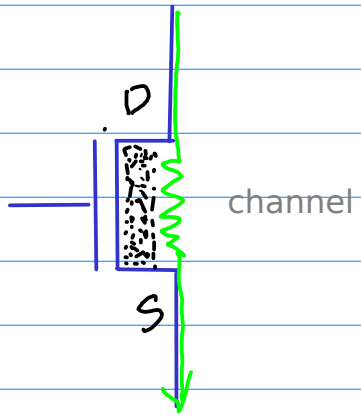
nMOS Resistance

V = IR

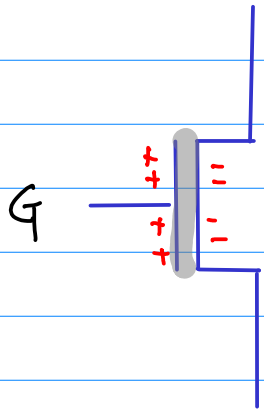
R = V / I = Vds / Ids

nMOS Gate Capacitance

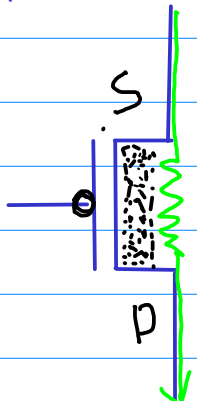
insulator



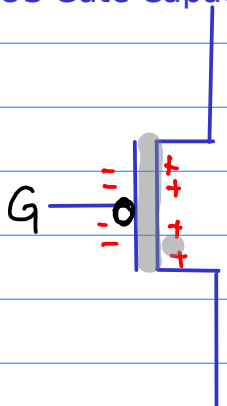
channel



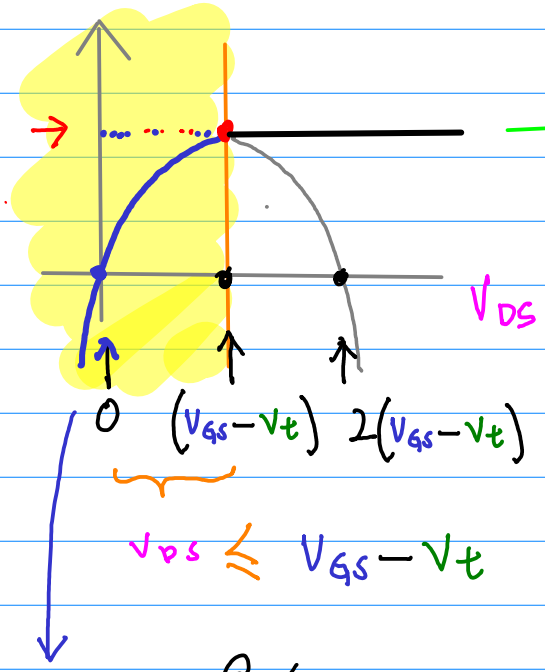
pMOS Gate Capacitance



pMOS Gate Capacitance



Linear and Saturation Current



SAT

$$I_{DS} = \frac{\beta}{2}(V_{GS}-V_t)^2$$

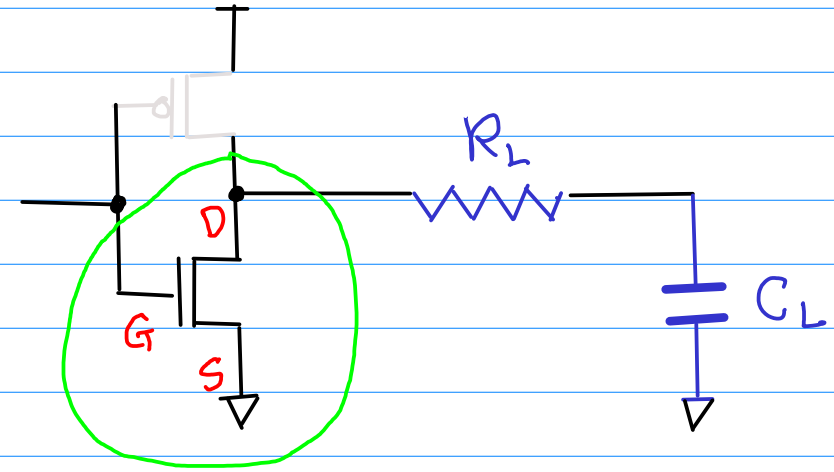
$$V_{DS} \lesssim V_{GS}-V_t$$

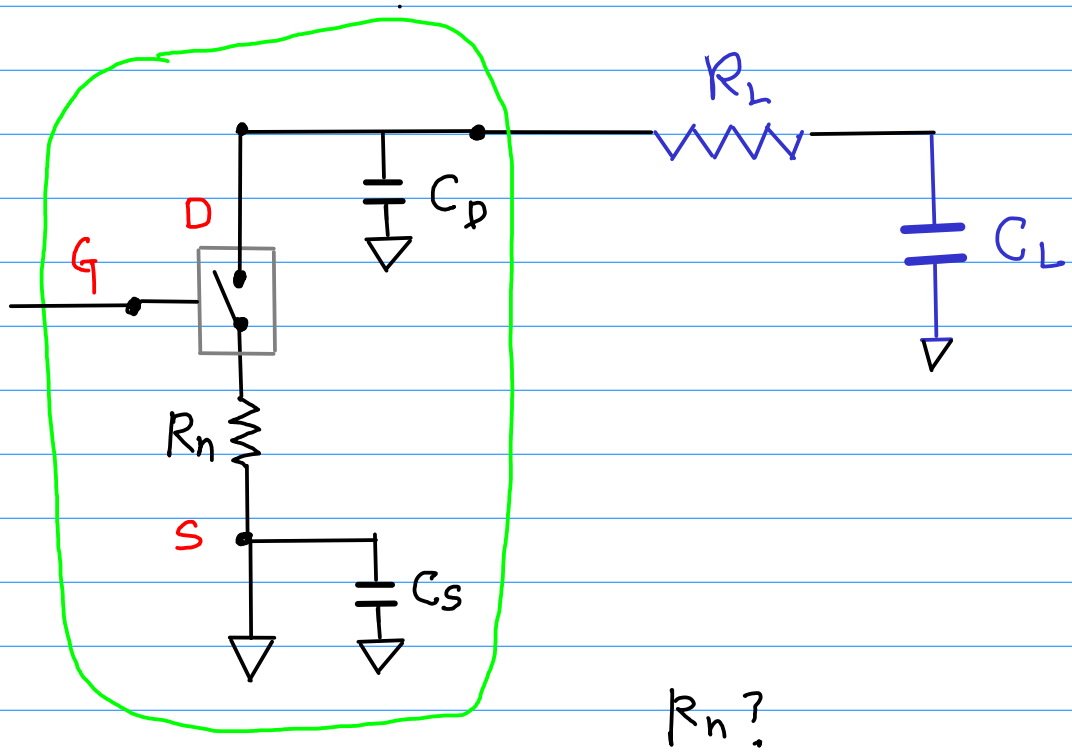
LIN

$$I_{DS} = \frac{\beta}{2}\left(2(V_{GS}-V_t) - V_{DS}\right)V_{DS}$$

$$= \frac{\beta}{2}\left(2(V_{GS}-V_t)V_{DS} - V_{DS}^2\right)$$

Linear Model of nMOS





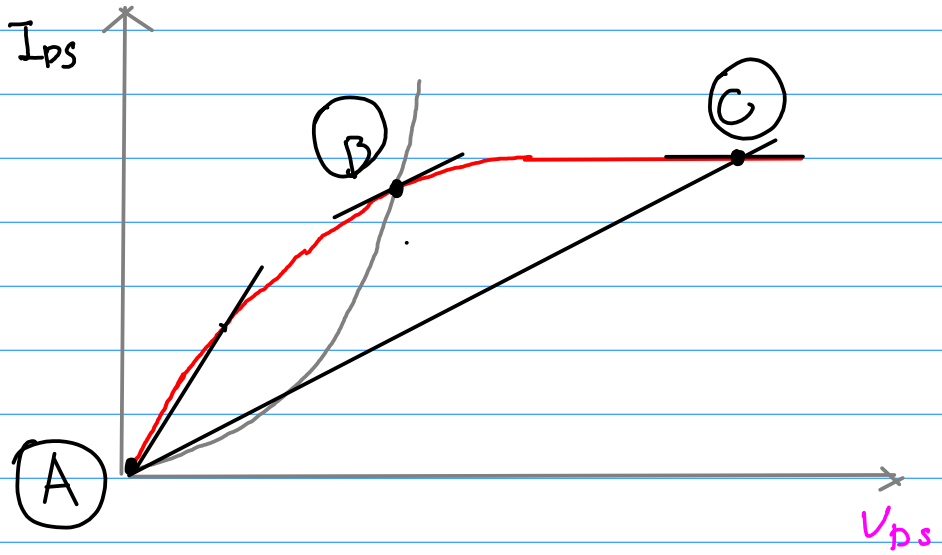
R_n ?

C_S ?

C_D ?

$$R_n = \frac{V_{DS}}{I_{DS}} \quad , \quad \frac{\Delta V_{DS}}{\Delta I_{DS}} \quad , \quad \frac{\partial V_{DS}}{\partial I_{DS}}$$

(A), (C) (B)



LIN (A)

$$I_{DS} = \frac{\beta}{2}\left(2(V_{GS}-V_t)V_{DS} - V_{DS}^2\right) \qquad V_{DS} \ll 1 \Rightarrow V_{DS}^2 \approx 0$$

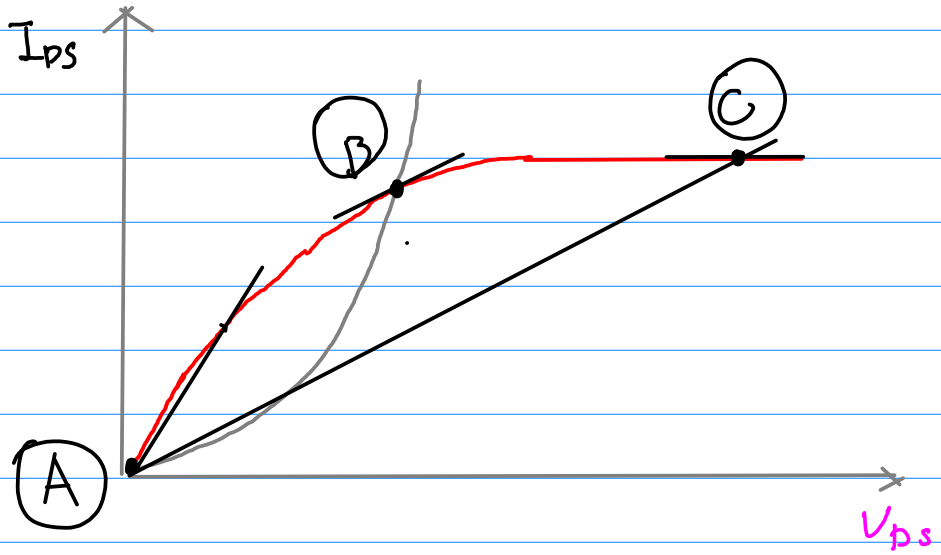
$$\simeq \beta\left(V_{GS}-V_t\right)V_{DS}$$

$$R_n = \frac{V_{DS}}{I_{DS}} \Rightarrow \qquad R_n = \frac{1}{\beta\left(V_{GS}-V_t\right)}$$

SAT (C)

$$I_{DS} = \frac{\beta}{2}\left(V_{GS}-V_t\right)^2$$

$$R_n = \frac{V_{DS}}{I_{DS}} \Rightarrow \qquad R_n = \frac{2 \cdot V_{DS}}{\beta\left(V_{GS}-V_t\right)^2}$$

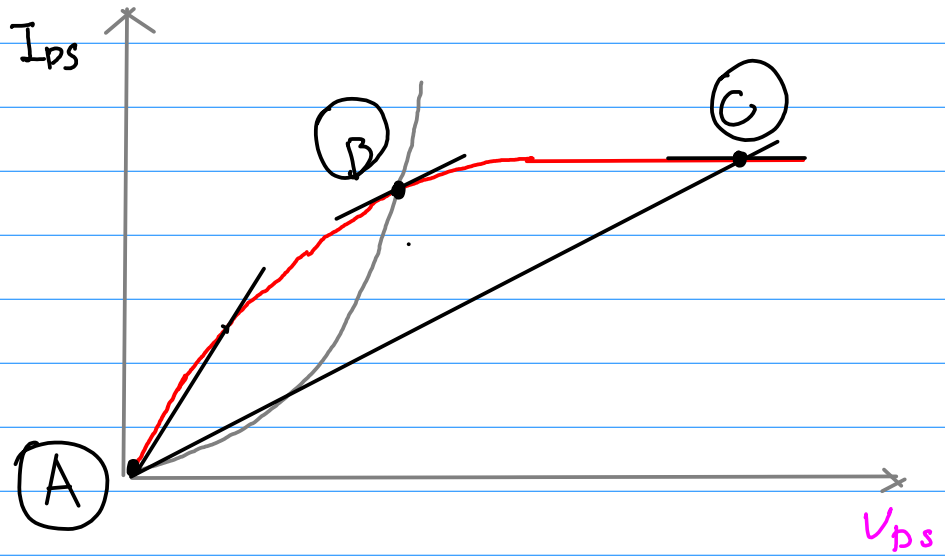


LIN

(B) $$I_{DS} = \frac{\beta}{2}\left(2(V_{GS}-V_t)V_{DS} - V_{DS}^2\right)$$

$$\frac{1}{R_n} = \frac{\partial I_{DS}}{\partial V_{DS}} = \frac{\beta}{2}\left(2(V_{GS}-V_t) - 2V_{DS}\right)$$ tangent

$$R_n = \frac{V_{DS}}{I_{DS}} \Rightarrow R_n = \frac{2}{\beta\left(2(V_{GS}-V_t) - 2V_{DS}\right)}$$



(A) $$R_n = \frac{1}{\beta (V_{GS} - V_t)}$$

(B) $$R_n \simeq \frac{2}{\beta \left(2(V_{GS} - V_t) - 2V_{DS} \right)}$$

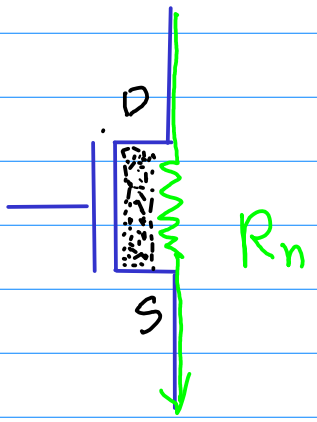
(C) $$R_n = \frac{2 \cdot V_{DS}}{\beta (V_{GS} - V_t)^2}$$

$$R_n \propto \frac{1}{\beta} = \frac{1}{k' \left(\frac{W}{L} \right)}$$

$$R_n = \frac{\eta}{\beta (V_{DD} - V_t)} \qquad \eta = 1 \sim 6$$

Rule of thumb $$R_n = \frac{1}{\beta (V_{DD} - V_t)}$$

nMOS Resistance



$$R_n = \frac{1}{\beta (V_{DD} - V_t)}$$

Device Transconductance Parameter

$$\beta = k' \left(\frac{W}{L}\right)$$

Process Transconductance Parameter

$$k' = \mu C_{ox}$$

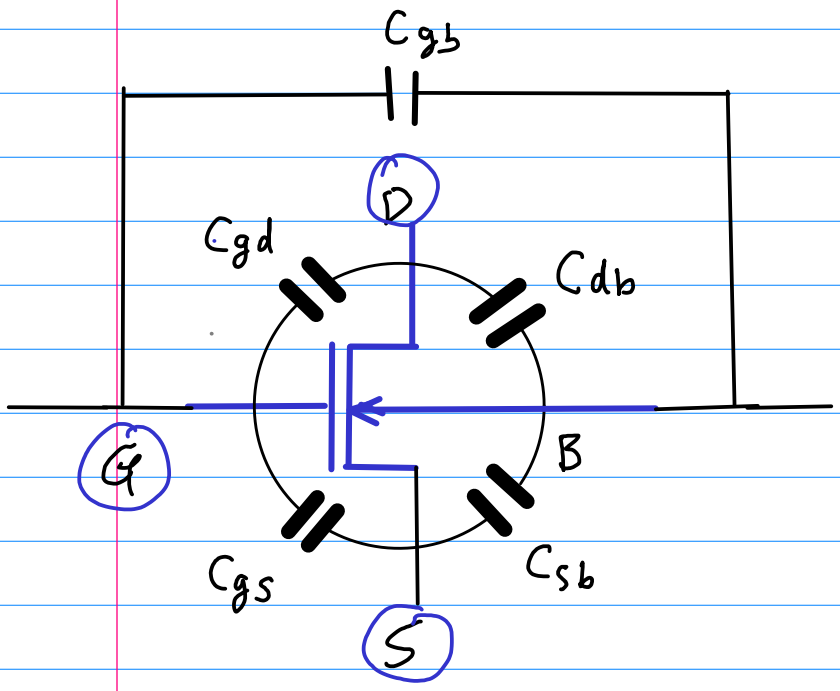
Oxide Capacitance per unit area

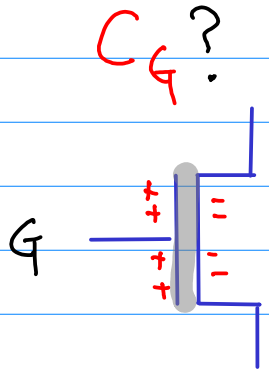
$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$k' = \frac{\mu \varepsilon_{ox}}{t_{ox}}$$

$$\beta = \frac{\mu \varepsilon_{ox}}{t_{ox}} \left(\frac{W}{L}\right)$$

nMOS Gate Capacitance





C_G

oxide related capacitance

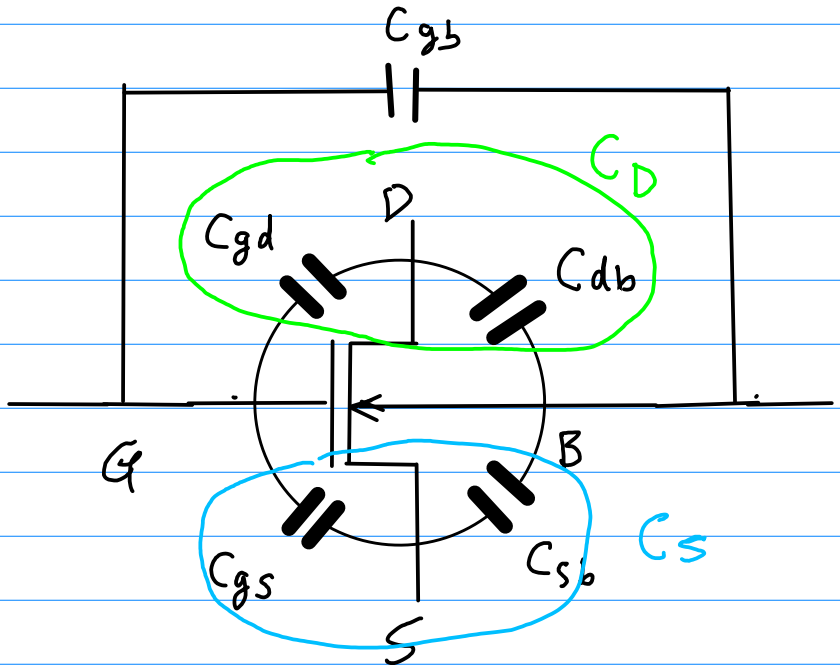
overlap capacitance

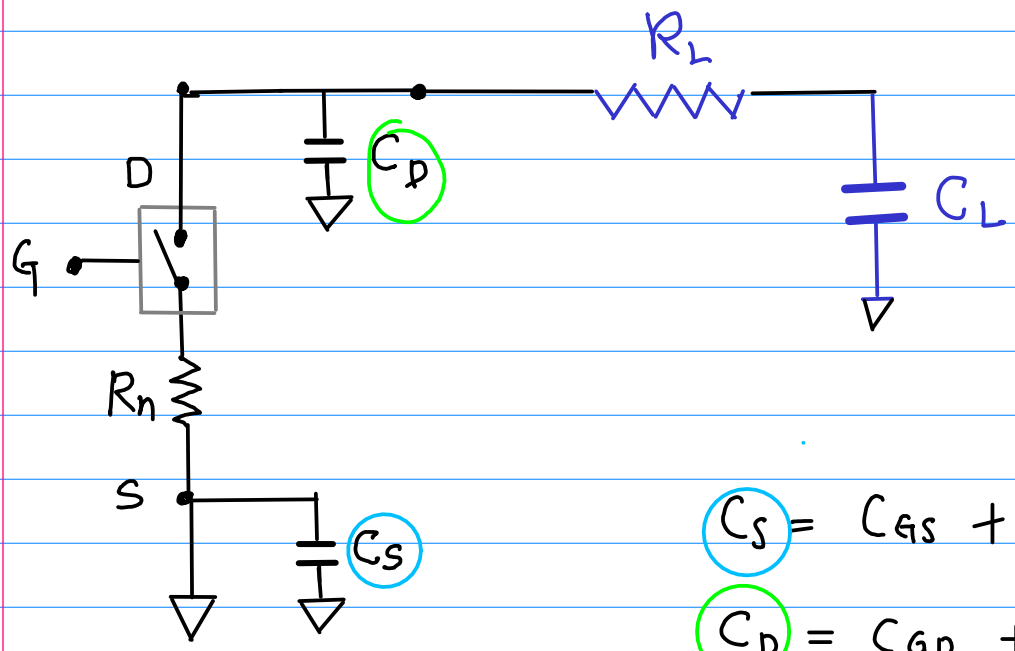
① Cut off	② Linear	③ saturation
$C_{ox} \cdot W \cdot L$	$C_{ox} \cdot W \cdot L$	$\frac{2}{3} C_{ox} \cdot W \cdot L$
$+ C_{GS0}$	$+ C_{GS0}$	$+ C_{GS0}$
$+ C_{GD0}$	$+ C_{GD0}$	$+ C_{GD0}$
$+ 2 C_{GB0}$	$+ 2 C_{GB0}$	$+ 2 C_{GB0}$

$$C_G = C_{ox} \cdot W \cdot L$$

$$C_{GS} = \frac{1}{2} C_G$$

$$C_{GD} = \frac{1}{2} C_G$$





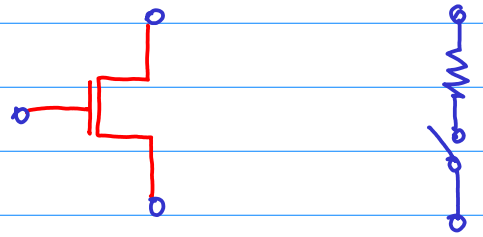
$C_S = C_{GS} + C_{SB}$

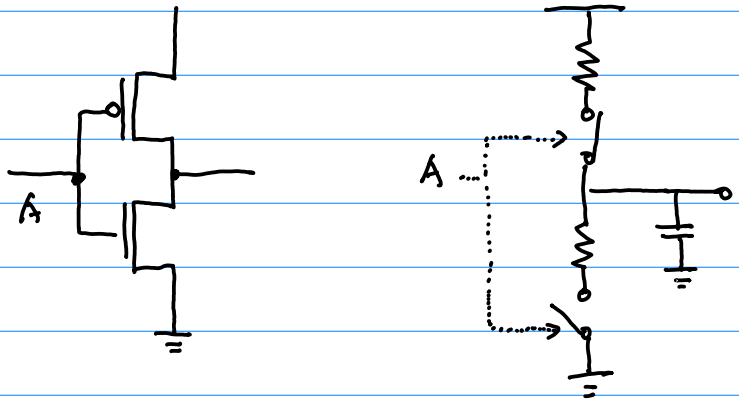
$C_D = C_{GD} + C_{DB}$

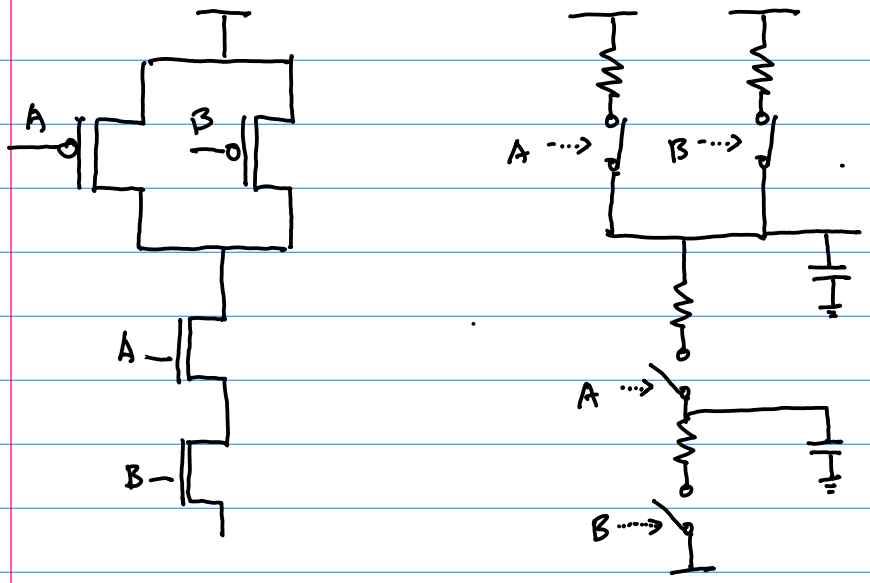
Junction Capacitance
(Diffusion, depletion)

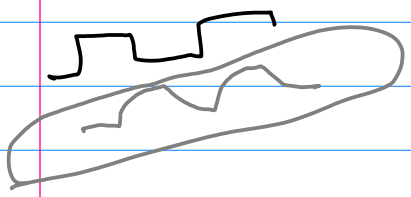
Linear Model of nMOS

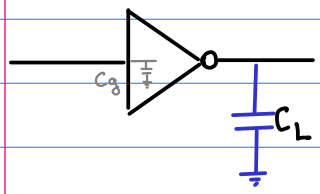
Switch Delay Model

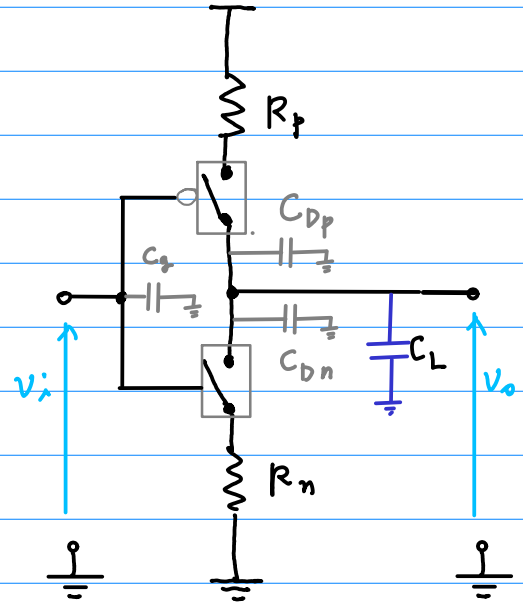


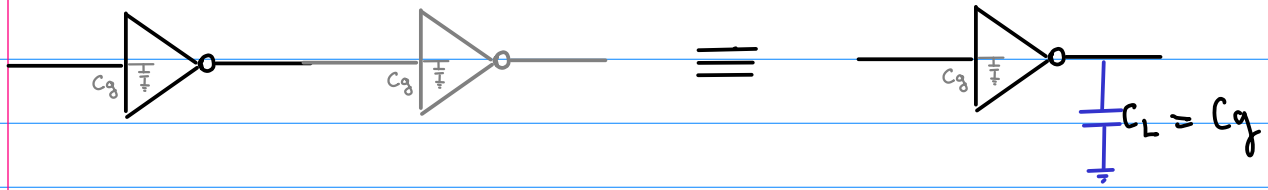


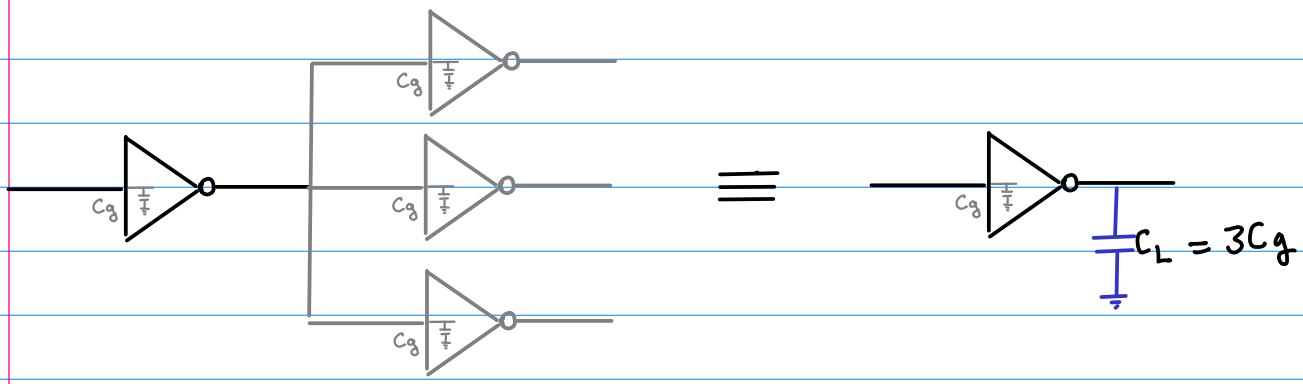


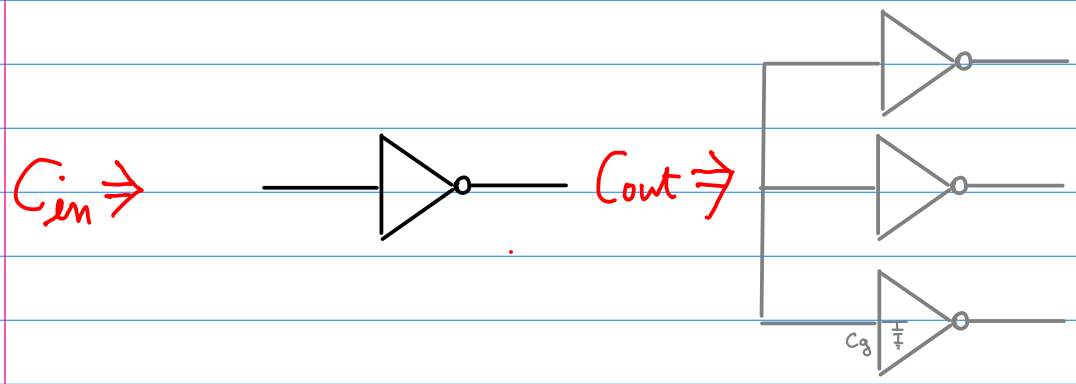


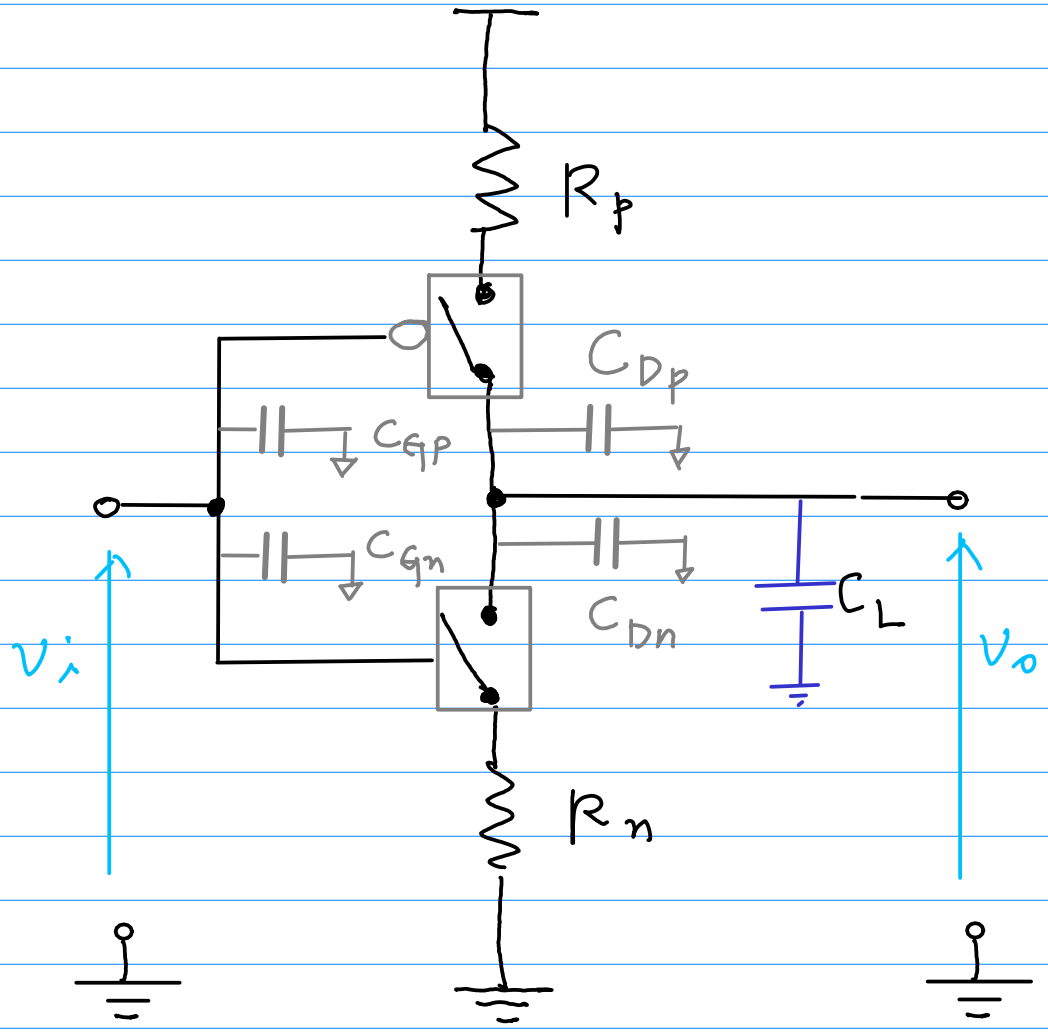

C_g
C_L


R_p
C_{Dp}
C_g
C_{Dn}
C_L
V_i
V_o
R_n


C_g
C_g
C_g
$C_L = C_g$


C_g
C_g
C_g
C_g
C_g
$C_L = 3C_g$

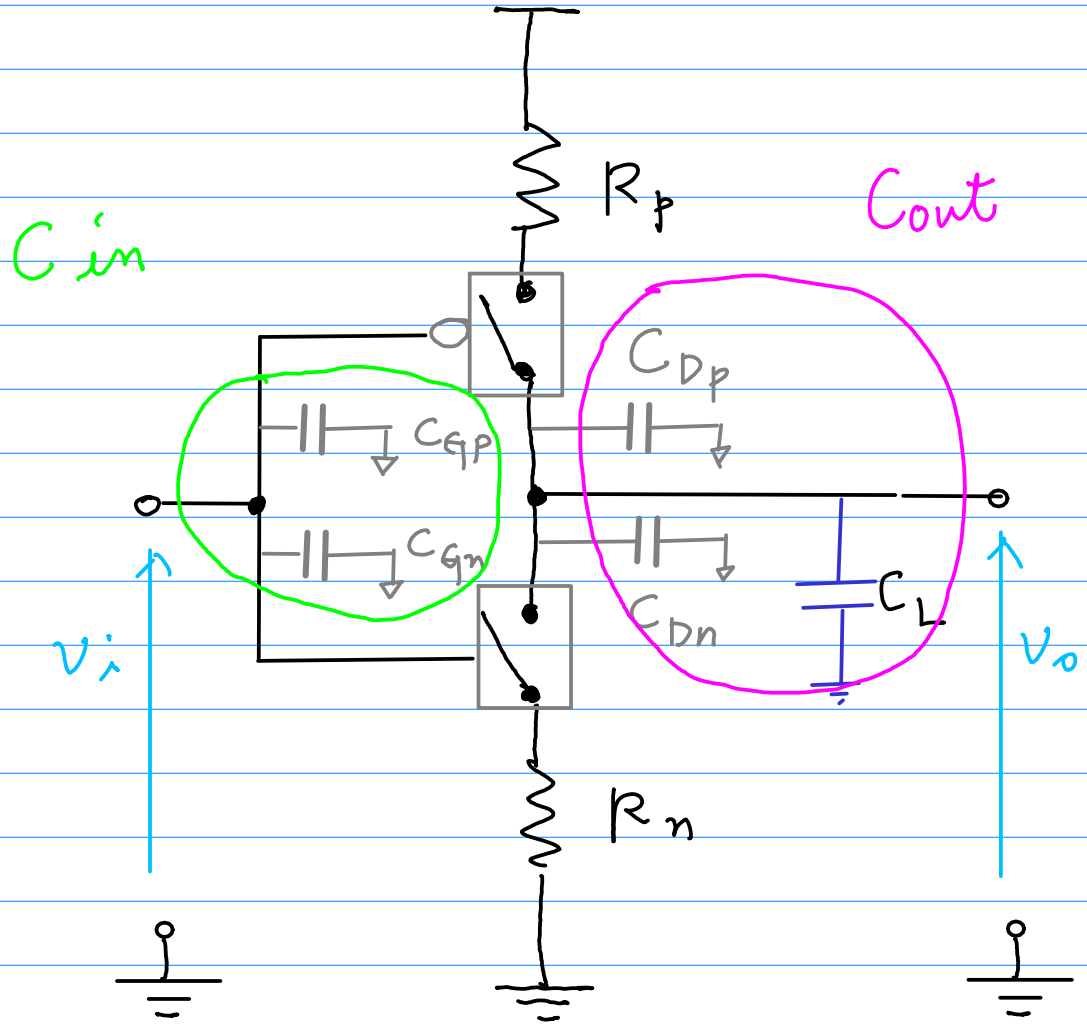




$C_{in} = C_{Gp} + C_{Gn}$

$C_{out} = C_{FET} + C_L$

$= (C_{Dp} + C_{Dn}) + C_L$



$C_G = C_{ox} W L$

$C_{GS} = \frac{1}{2} C_G$

$C_{GD} = \frac{1}{2} C_G$

$C_S = C_{GS} + C_{SB}$

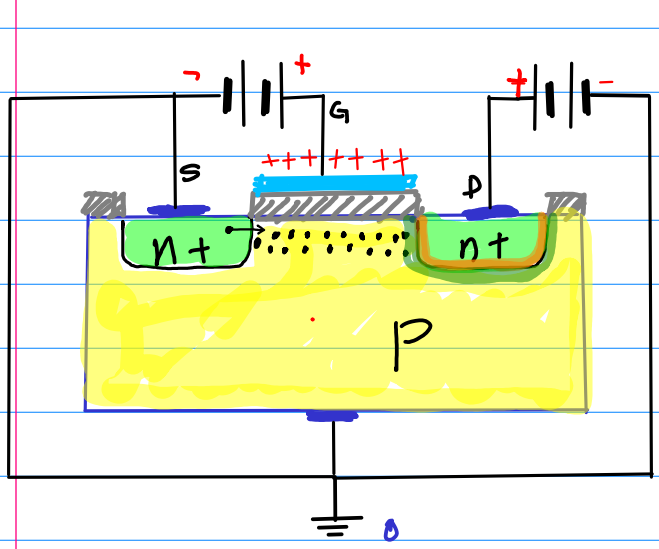
$C_D = C_{GD} + C_{DB}$

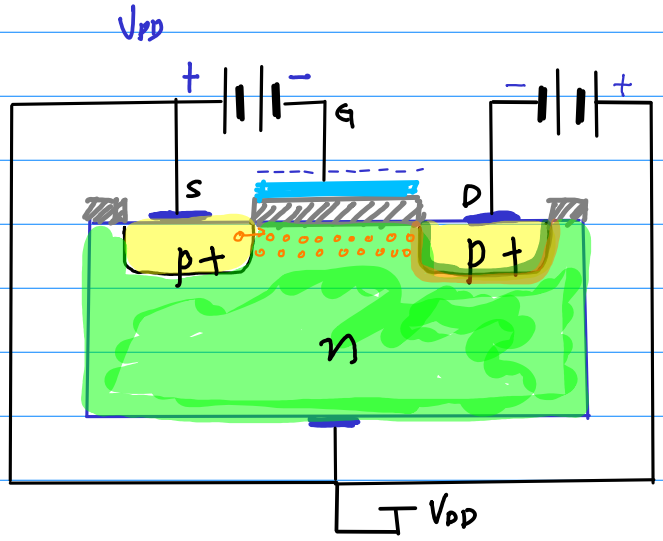
$C_{in} = C_{Gp} + C_{Gn}$

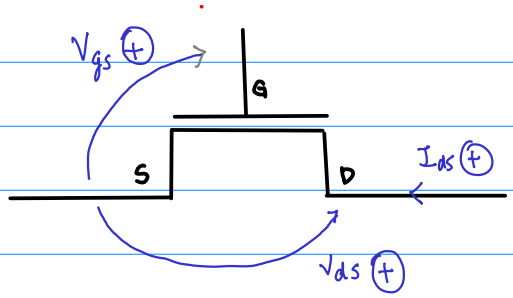
$C_{out} = C_{FET} + C_L$

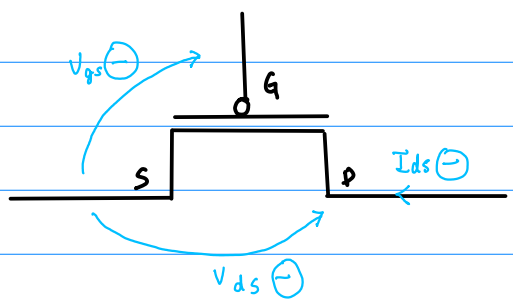
$= (C_{Dp} + C_{Dn}) + C_L$

Reverse-biased Junction Capacitance

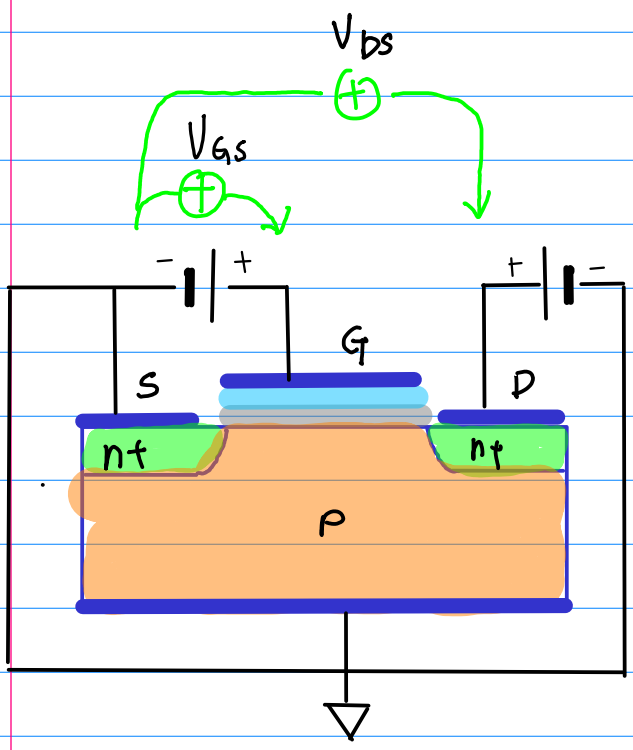


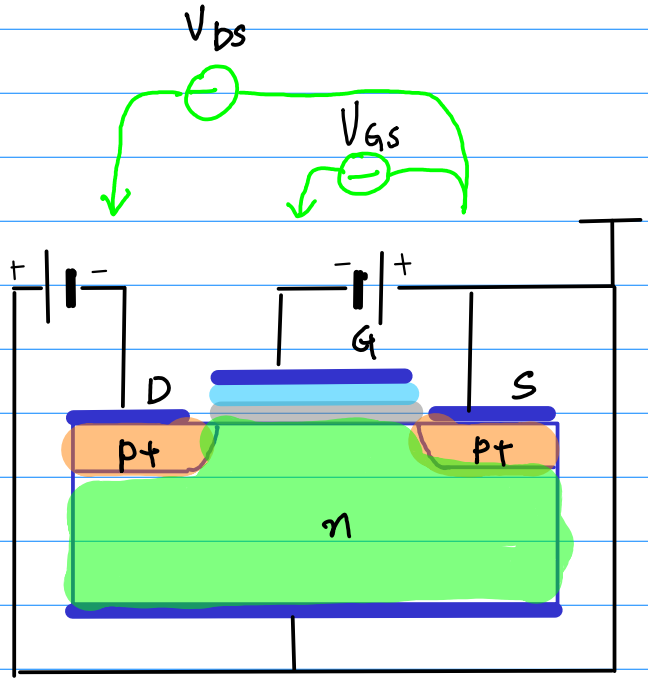






Linear Mode Bias Condition (2)





$V_{GD} = V_{GS} - V_{DS} > V_{Tn}$

$V_{GS} - V_{Tn} > V_{DS}$

$V_{GD} \simeq V_{GS} - V_{DS} < V_{Tp}$

$V_{GS} - V_{Tp} < V_{DS}$

$V_{GS} > V_{Tn}$,

$V_{DS} < V_{GS} - V_{Tn}$

$V_{GS} < V_{Tp}$,

$V_{DS} > V_{GS} - V_{Tp}$

$-V_{SD} > -V_{SG} - V_{Tp}$

$V_{SD} < V_{SG} + V_{Tp}$

$V_{GS} < V_{Tp}$,

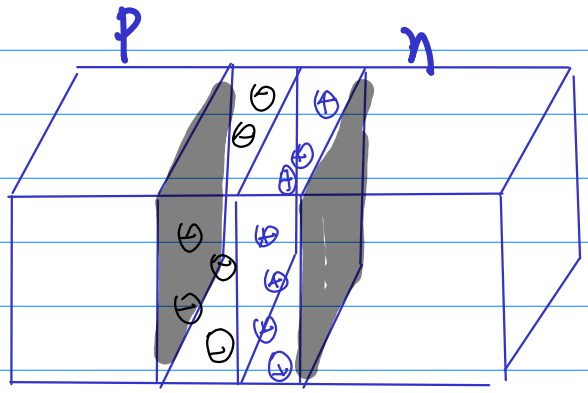
$V_{SD} < V_{SG} + V_{Tp}$

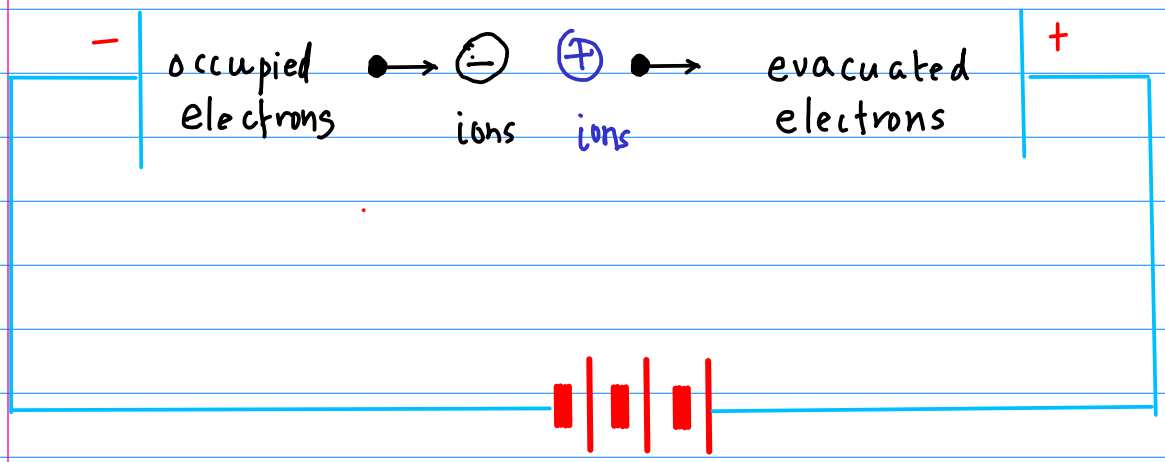
$V_{SG} > |V_{Tp}|$

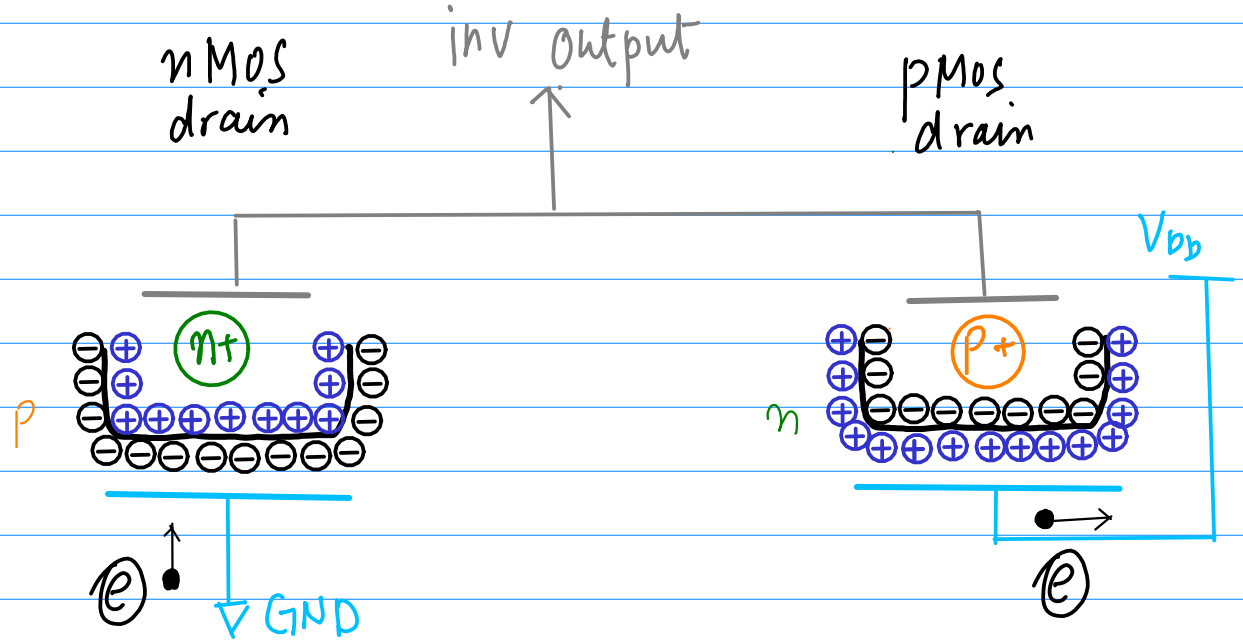
$V_{SD} < V_{SG} - |V_{Tp}|$

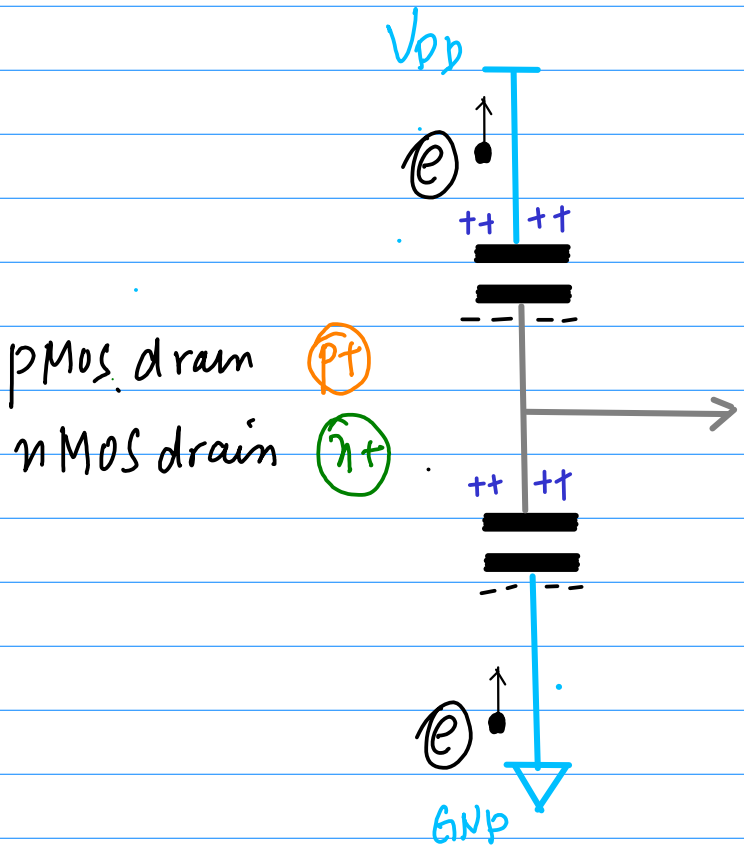
Space charge

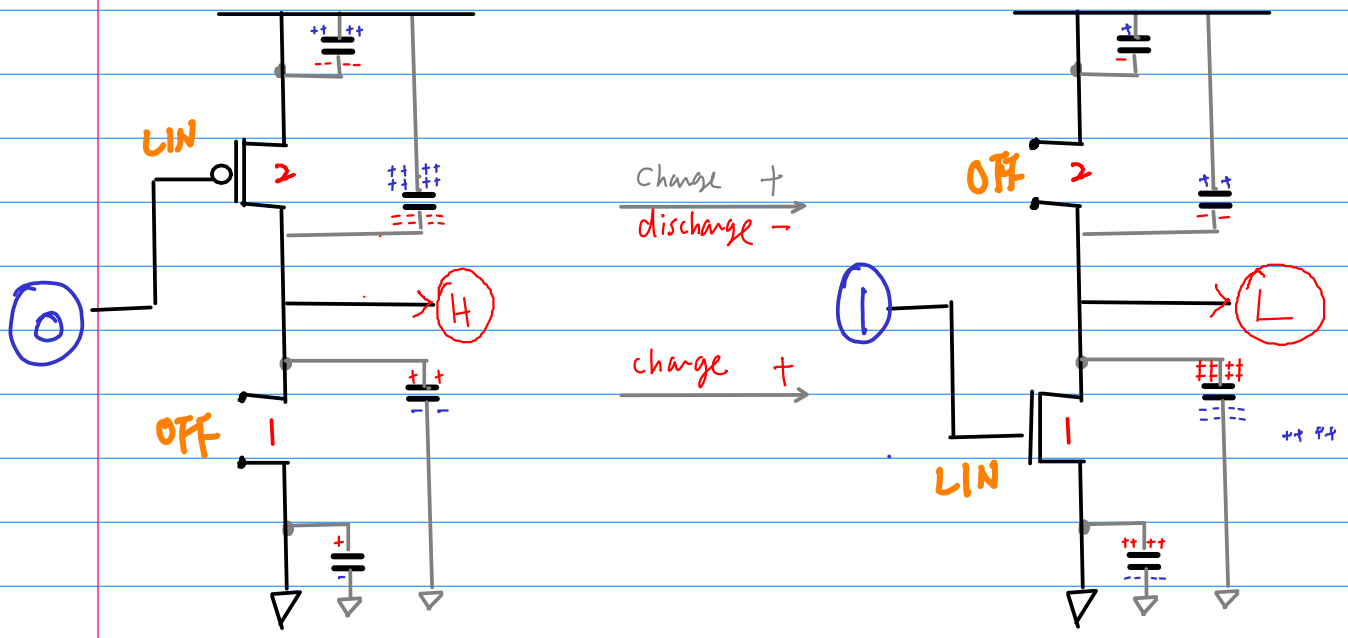
fixed, immobile






nMOS drain
inv output
pMOS drain
V_{DD}
$n+$
$p+$
p
n
GND


V_{DD}
pMOS drain
nMOS drain
$p+$
$n+$
GND


LIN
2
0
H
OFF
1
Charge +
discharge −
charge +
OFF
2
1
L
LIN

Conceptual Parallel Connection