CMOS Inverter (H.1)

20170329

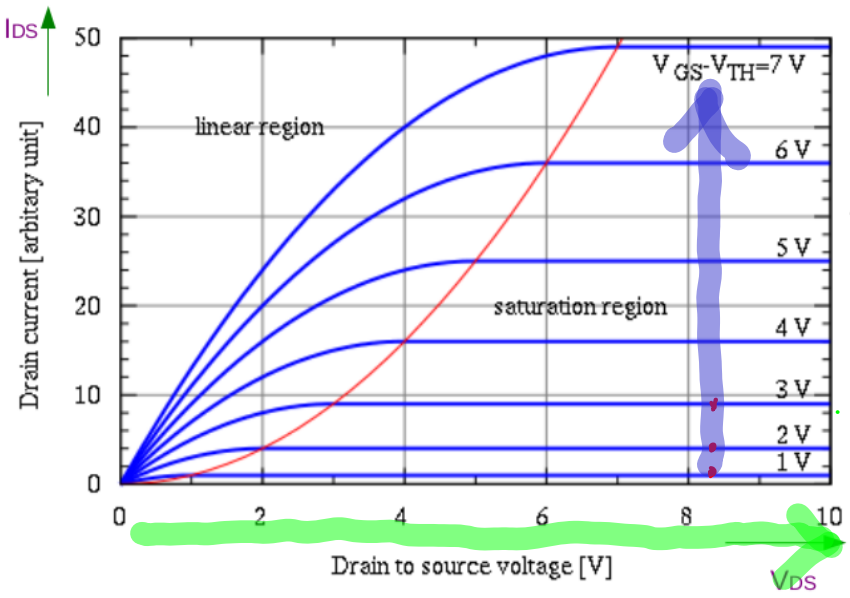
Common Source Mode (Inverter)
Votage Transfer Characteristic (VTC)
Noise Margin

References

Some Figures from the following sites

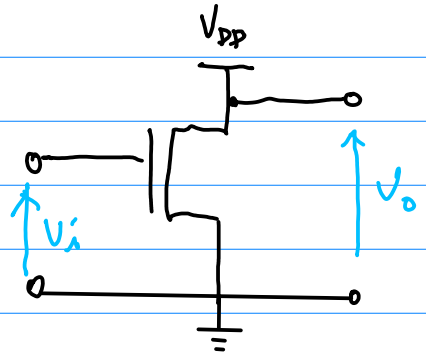
[1] http://pages.hmc.edu/harris/cmosvlsi/4e/index.html
Weste & Harris Book Site

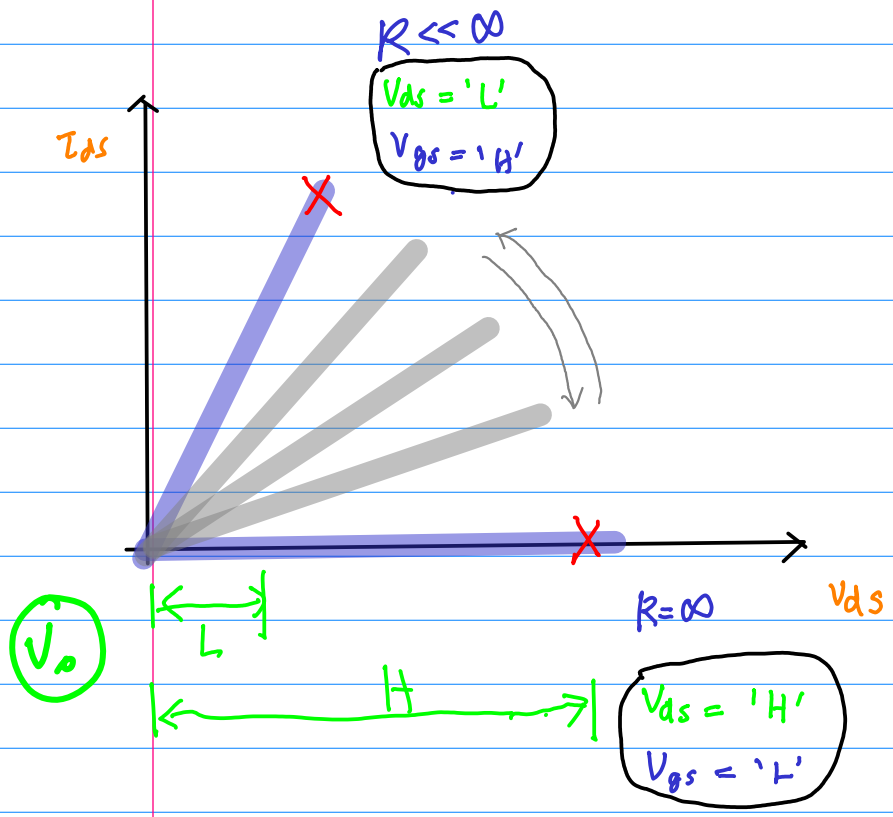
[2] en.wikipedia.org

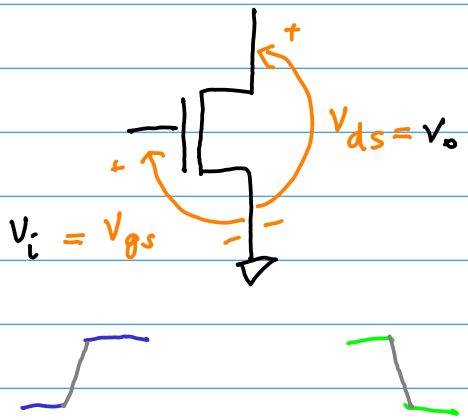


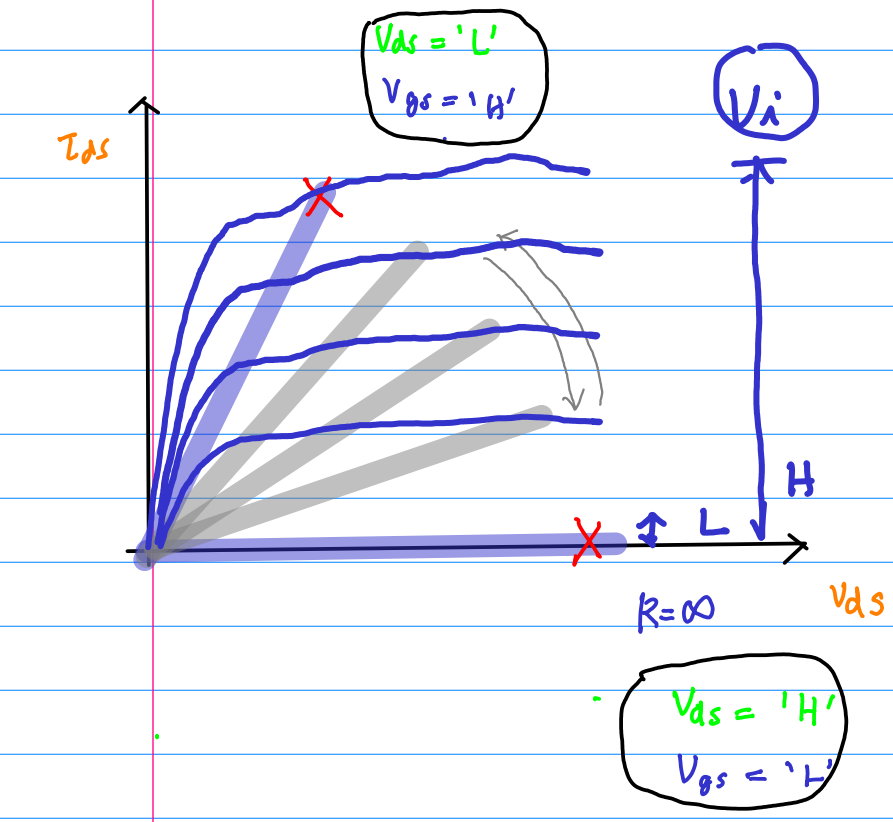
increasing input voltage V_i

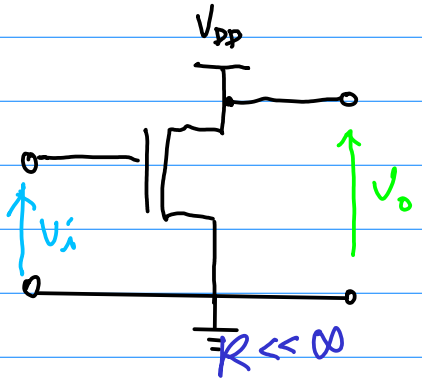
increasing output voltage. V_o



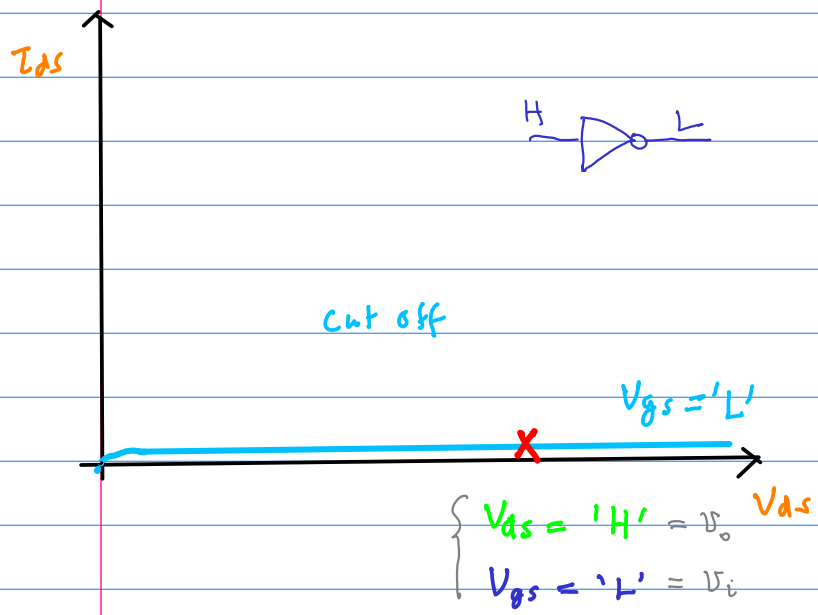

R << ∞
Vds = 'L'
Vgs = 'H'
Ids
Vds
R=∞
Vo
L
H
Vds = 'H'
Vgs = 'L'

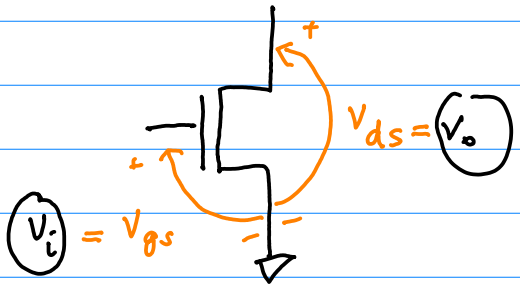

+
Vds = Vo
-
Vi = Vgs
-

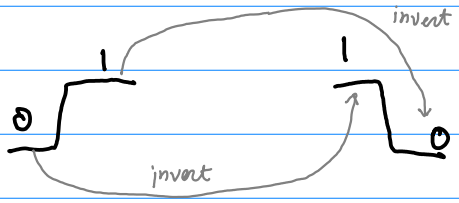

Vds = 'L'
Vgs = 'H'
Vi
Ids
H
L
R=∞
Vds
Vds = 'H'
Vgs = 'L'

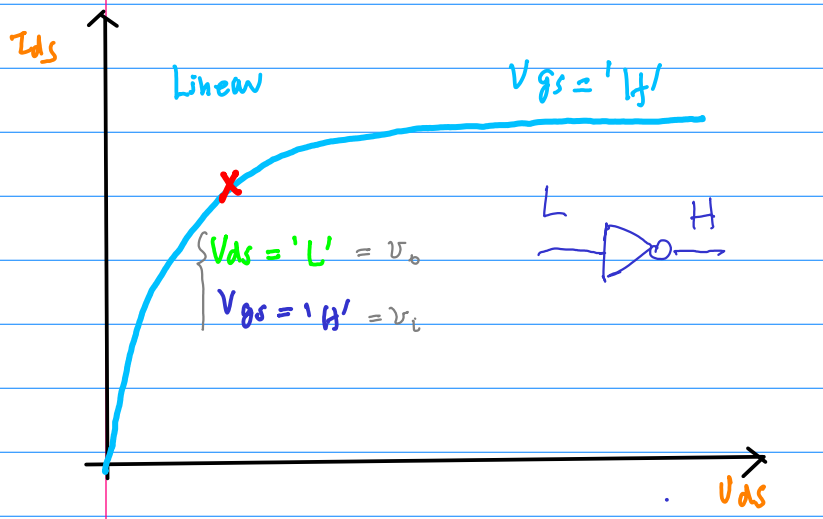

VDD
Vo
Vi
R << ∞

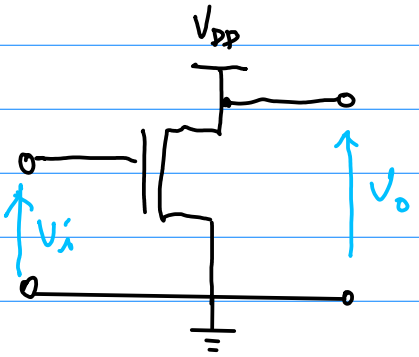
Inverter

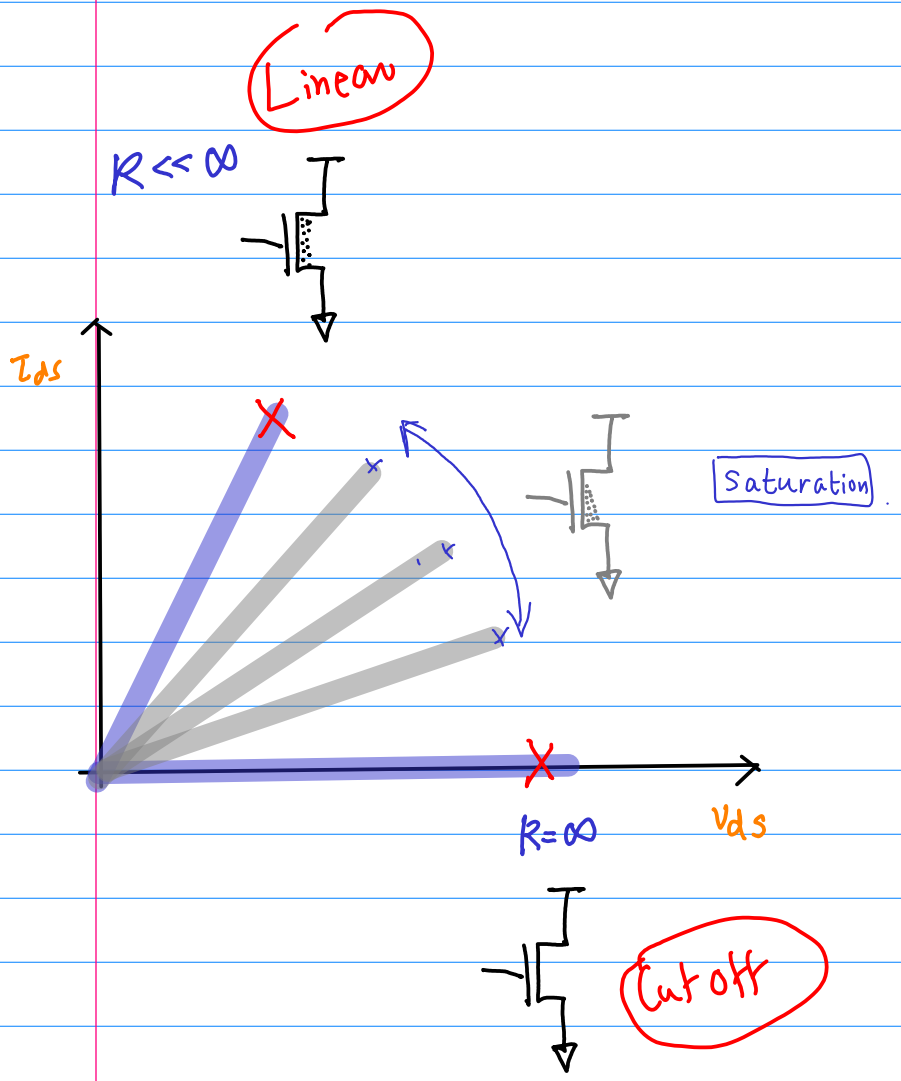

I_{ds}
H
L
cut off
V_{gs} = 'L'
V_{ds}
V_{ds} = 'H' = v_o
V_{gs} = 'L' = v_i

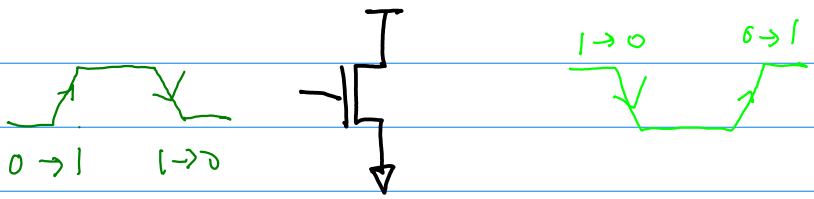

+
$V_{ds} = V_o$
-
$V_i = V_{gs}$

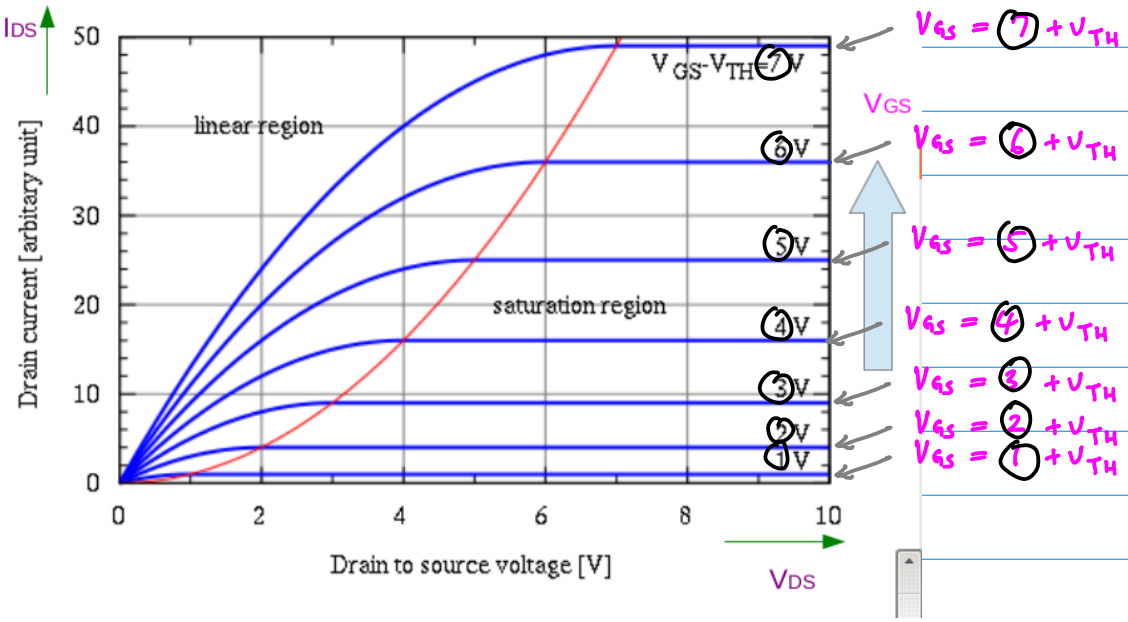

invert
1
1
0
0
invert

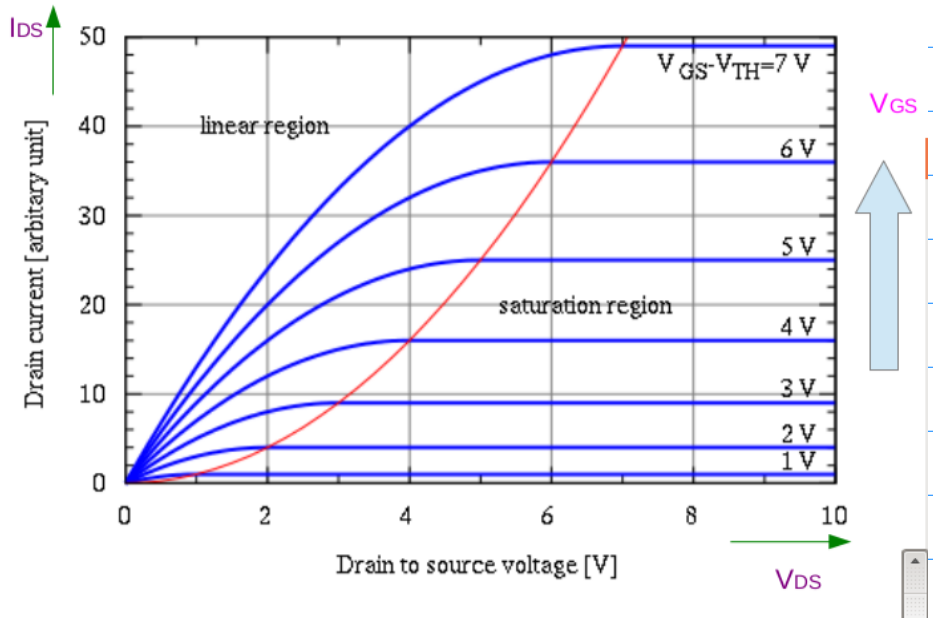

I_{ds}
Linear
V_{gs} = 'H'
V_{ds} = 'L' = v_o
V_{gs} = 'H' = v_i
L
H
V_{ds}

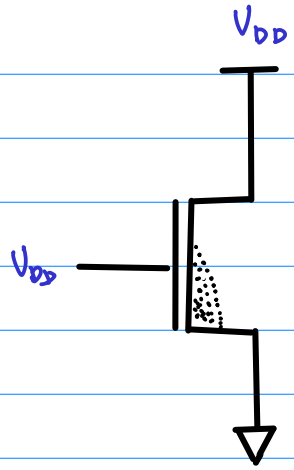

V_{DD}
V_i
V_o

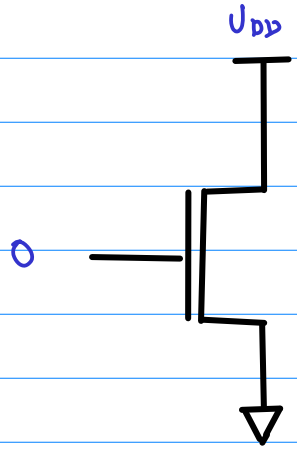

Linear
R << ∞
Ids
Saturation
R=∞
Vds
Cut off


0 → 1
1 → 0
1 → 0
0 → 1


IDS
Drain current [arbitary unit]
50
40
30
20
10
0
linear region
saturation region
VGS-VTH=7 V
6 V
5 V
4 V
3 V
2 V
1 V
0
2
4
6
8
10
Drain to source voltage [V]
VDS
VGS
VGS = 7 + VTH
VGS = 6 + VTH
VGS = 5 + VTH
VGS = 4 + VTH
VGS = 3 + VTH
VGS = 2 + VTH
VGS = 1 + VTH


IDS
Drain current [arbitary unit]
50
40
30
20
10
0
linear region
saturation region
VGS-VTH=7 V
6 V
5 V
4 V
3 V
2 V
1 V
0
2
4
6
8
10
Drain to source voltage [V]
VDS
VGS





$V_{gs} = V_{DD}$

$V_{ds} = V_{DD} > V_{DD} - V_T$

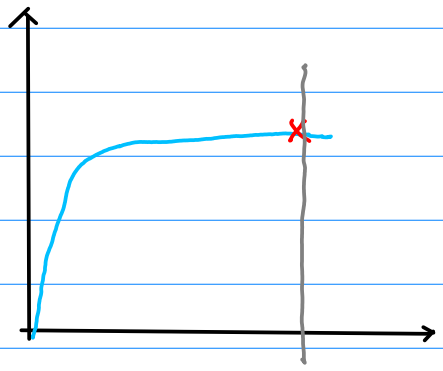
$V_{ds} > V_{gs} - V_T$

SAT

$V_{gs} = 0 < V_T$

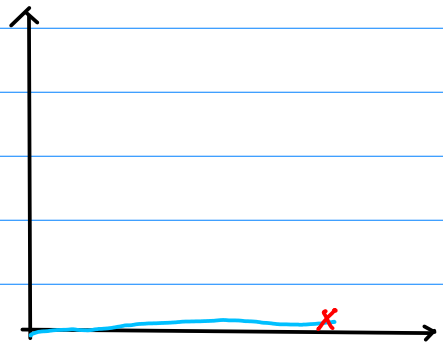
OFF

$> V_{gs} - V_T$



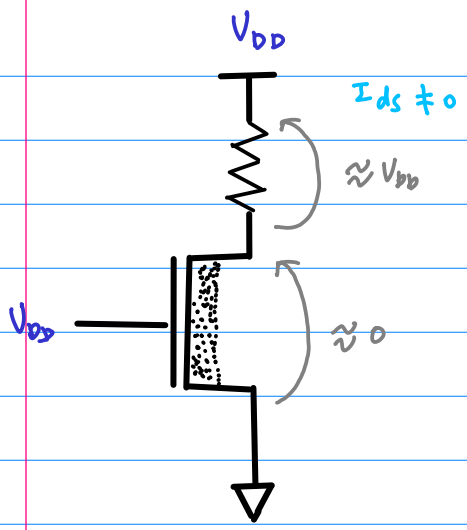
$V_{gs} = V_{DD}$

$V_{ds} = V_{DD} \rightarrow 0$



$V_{gs} = 0$

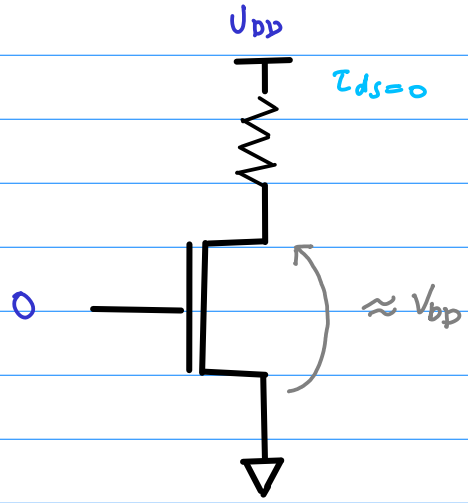
$V_{ds} = V_{DD}$



$V_{gs} = V_{DD}$

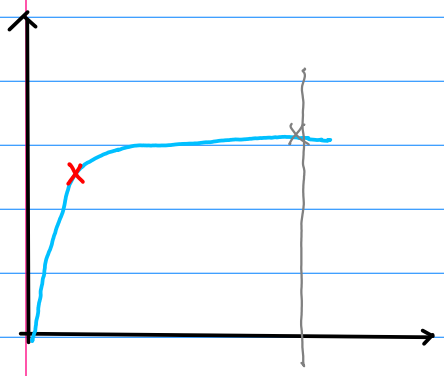
$V_{ds} = 0 < V_{gs} - V_T$

LIN



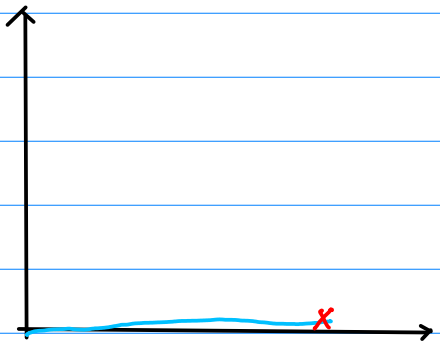
$V_{gs} = 0 < V_T$

OFF



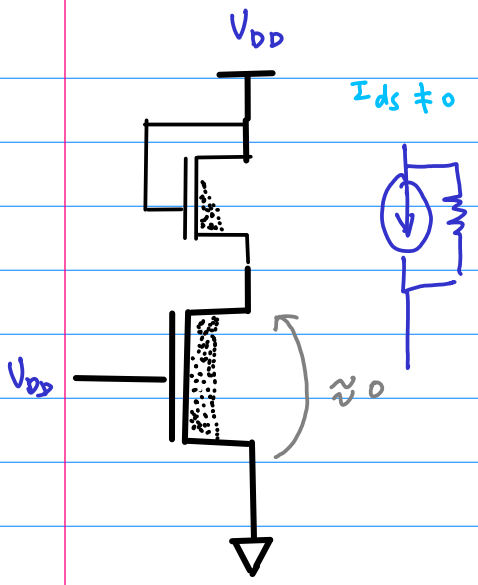
$V_{gs} = V_{DD}$

$V_{ds} = 0$



$V_{gs} = 0$

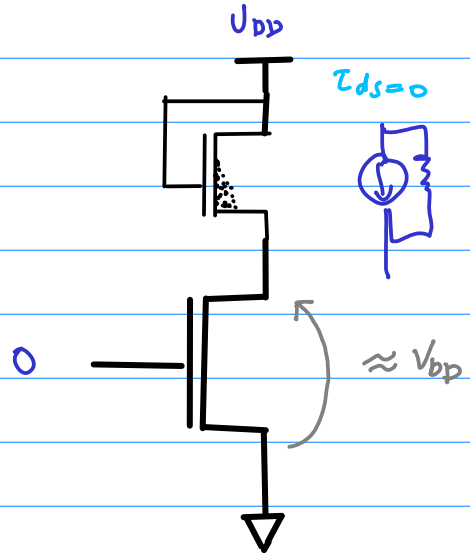
$V_{ds} = V_{DD}$



$V_{gs} = V_{DD}$

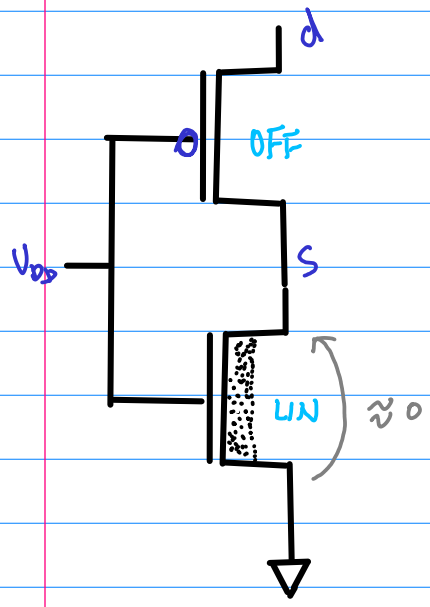
$V_{ds} = 0 < V_{gs} - V_T$

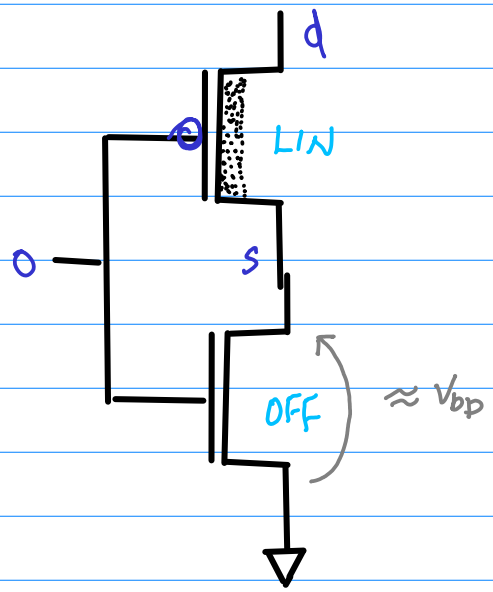
LIN



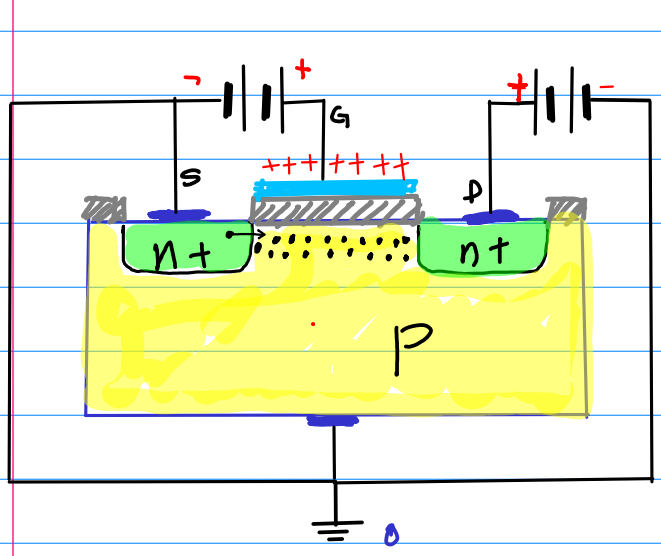
$V_{gs} = 0 < V_T$

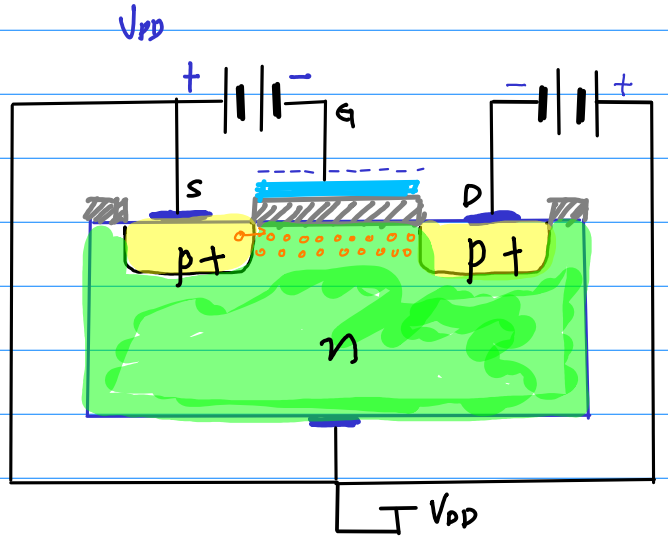
OFF

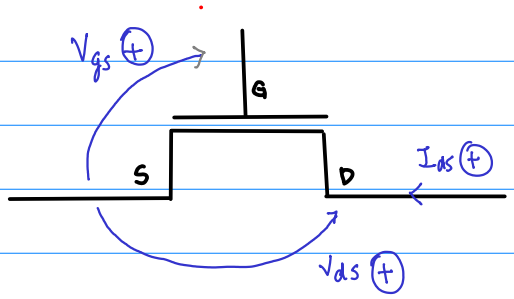

d
OFF
V_{DD}
S
LIN
≈ 0

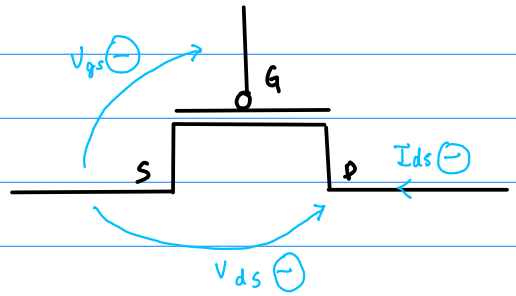

d
LIN
0
S
OFF
$\approx V_{DD}$

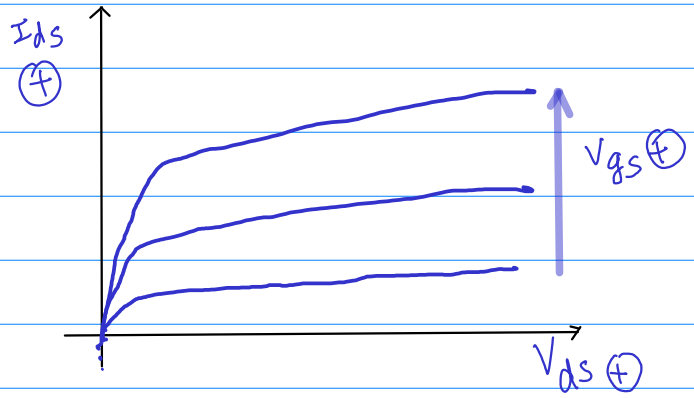
nMOS & pMOS

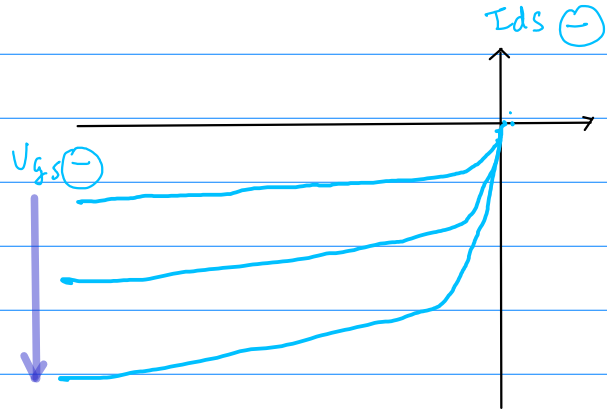

G
S
D
n+
n+
p
0

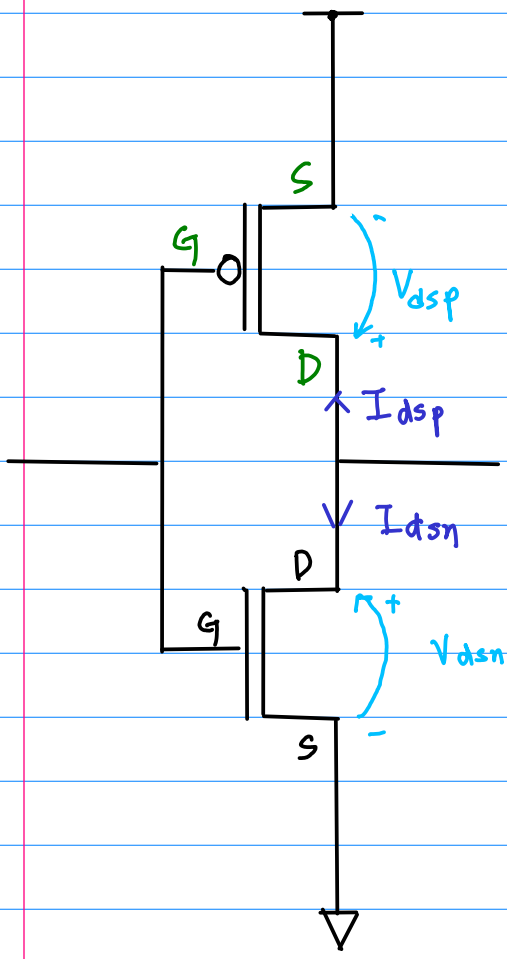

VDD
G
S
D
p+
p+
n
VDD


Vgs +
G
S
D
Ids +
Vds +

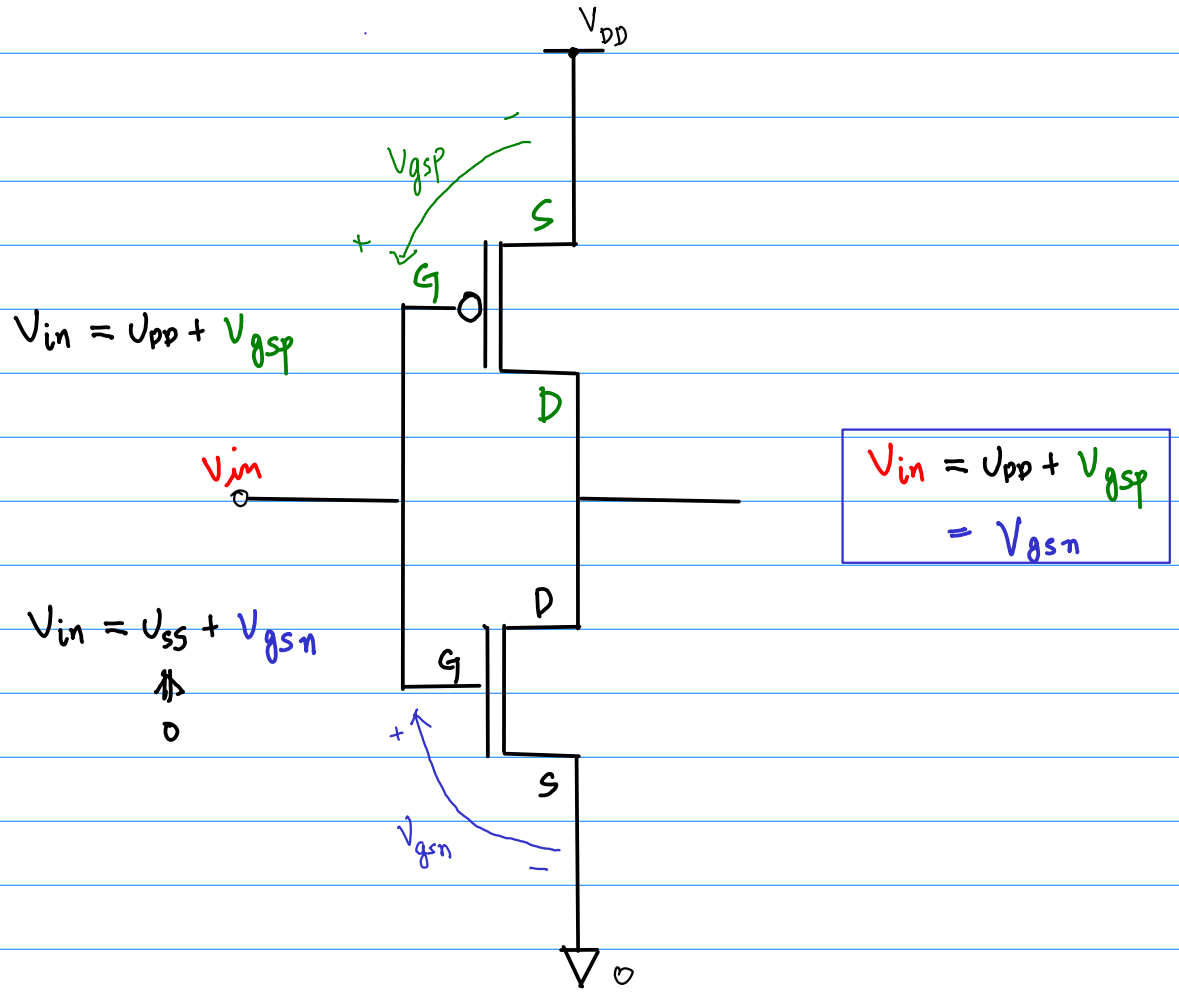

Vgs −
G
S
D
Ids −
Vds −


Ids +
Vgs +
Vds +


Ids −
Vgs −



$$I_{dsn} = -I_{dsp}$$



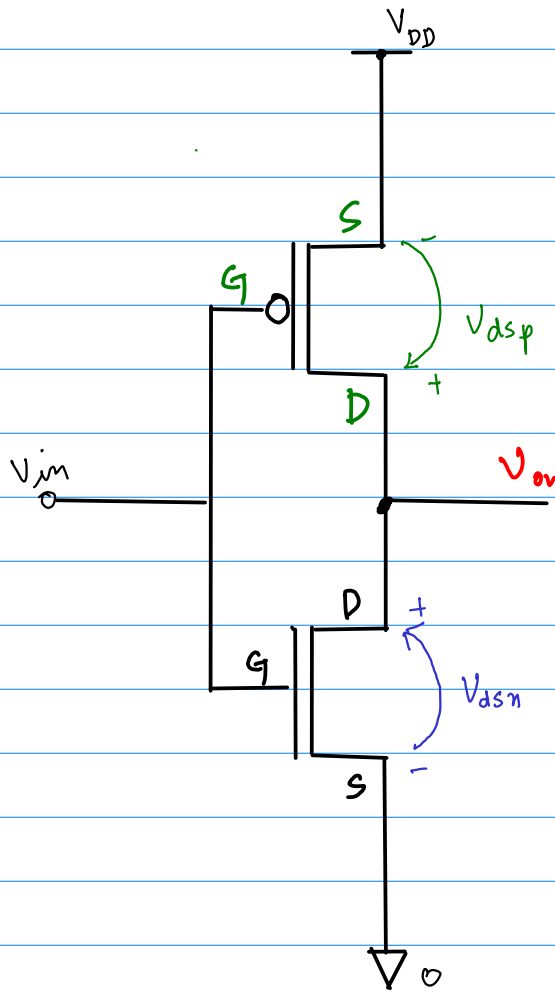
$V_{in} = V_{DD} + V_{gsp}$

$V_{in} = V_{SS} + V_{gsn}$

0

$V_{in} = V_{DD} + V_{gsp}$

$= V_{gsn}$

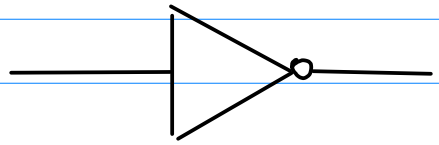


$V_{out} = V_{DD} + V_{dsp}$

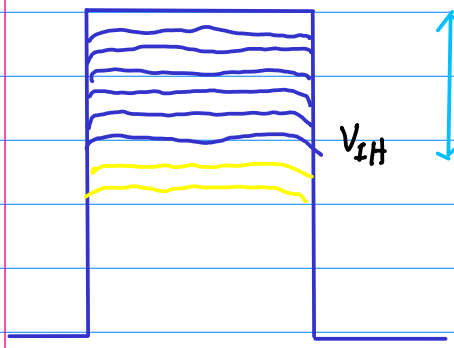
$V_{out} = V_{DD} + V_{dsp}$

$= V_{dsn}$

$V_{out} = V_{SS} + V_{dsn}$

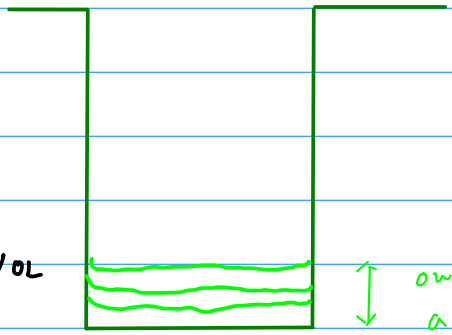


H



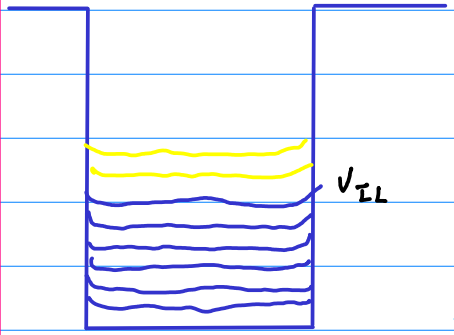
to be considered as High input

L



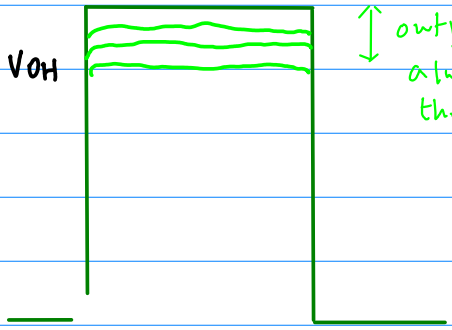
output Low always in this range

L



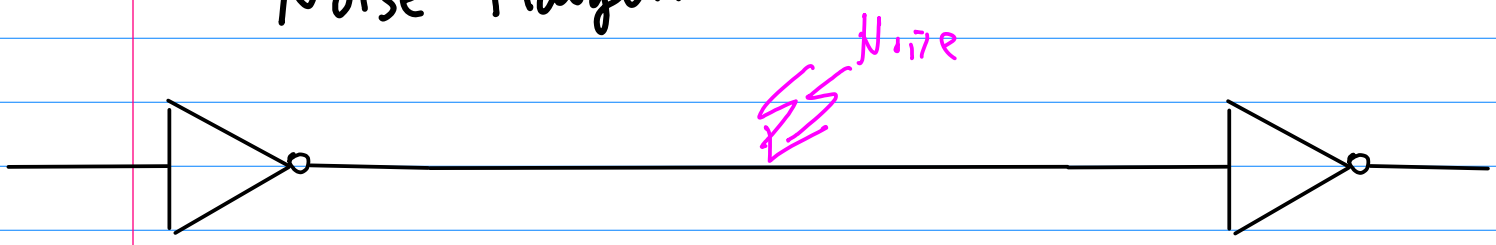
to be considered as Low input

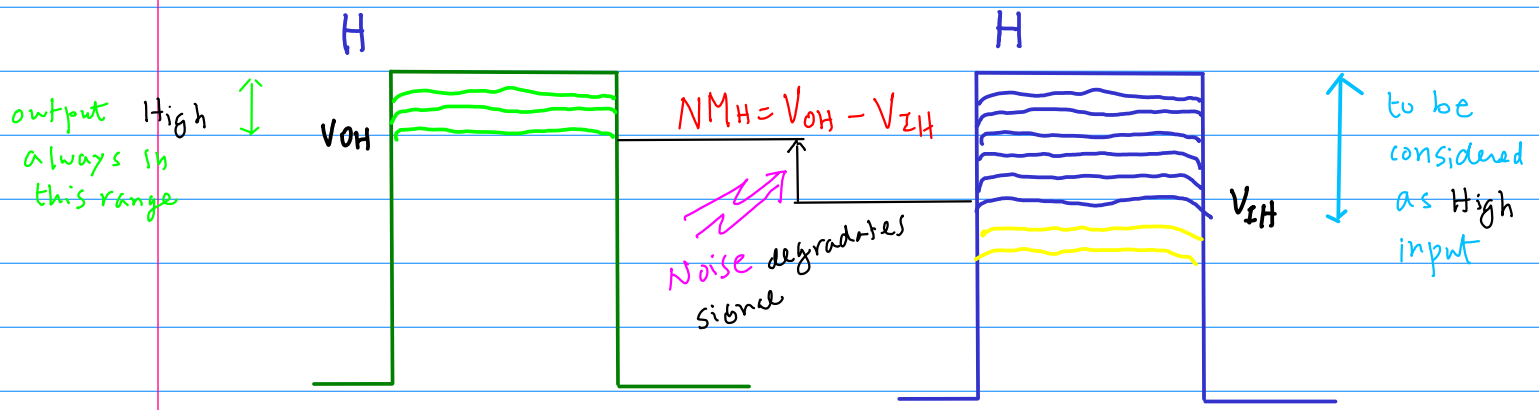
H

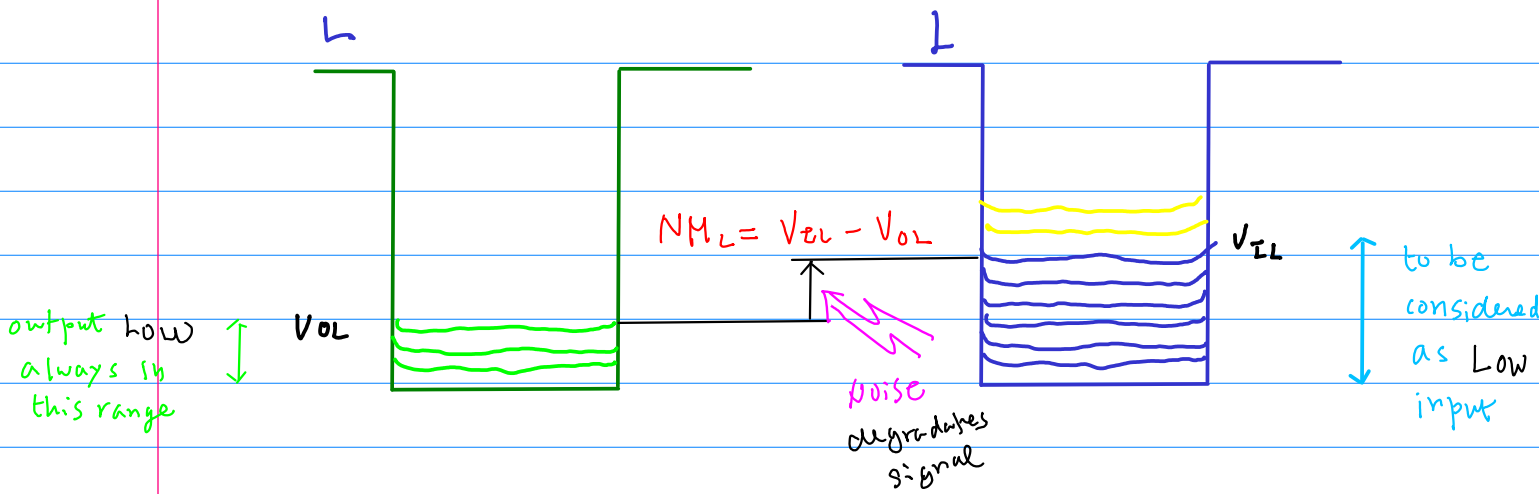


output High always in this range

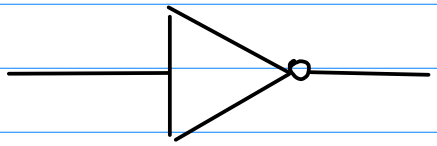
Noise Margin

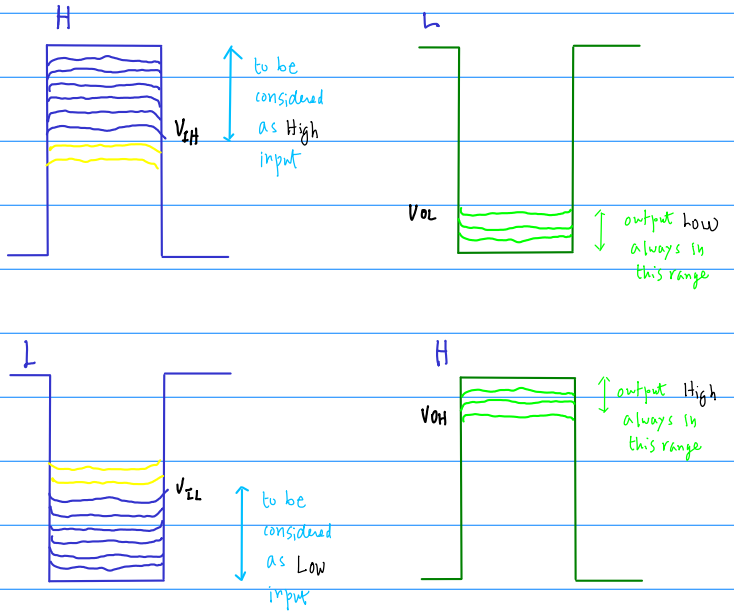


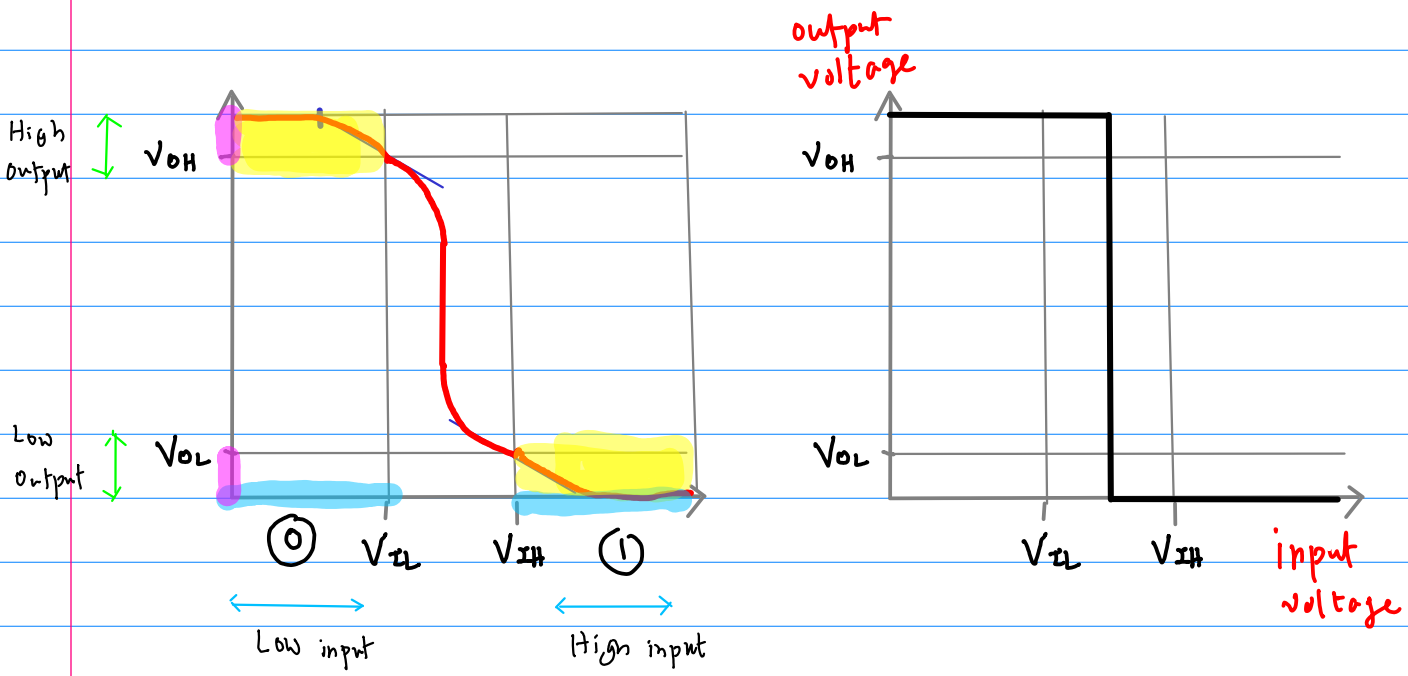


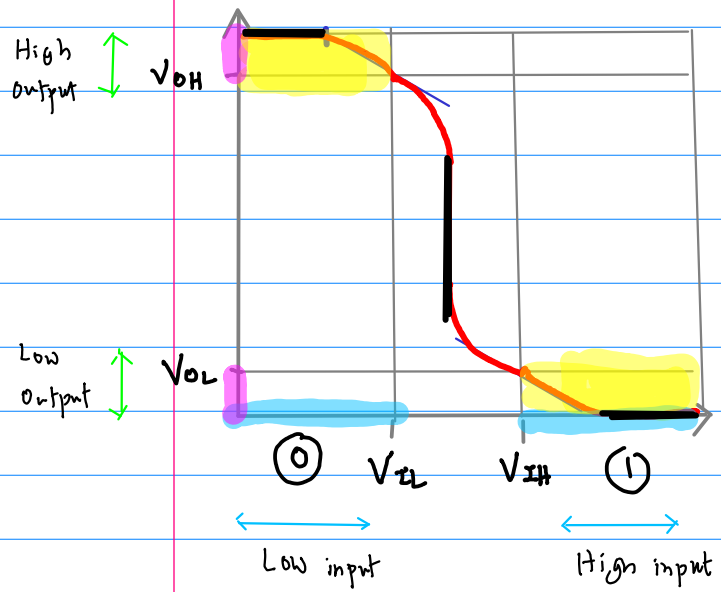


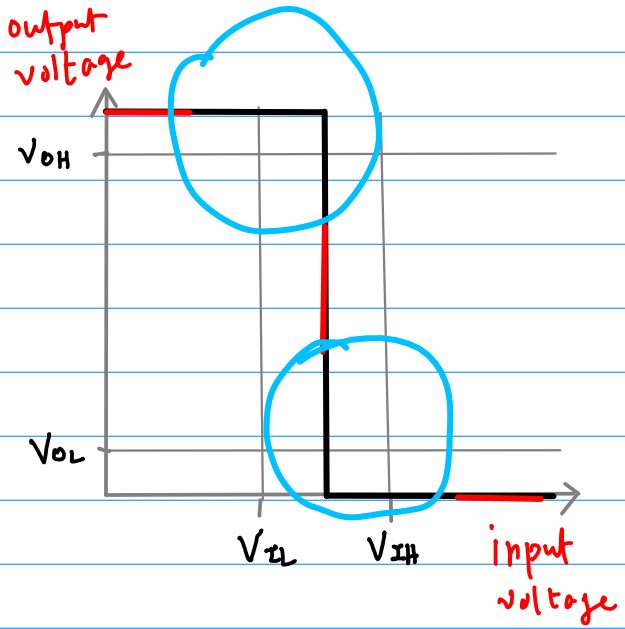
VTC Voltage Transfer characteristic

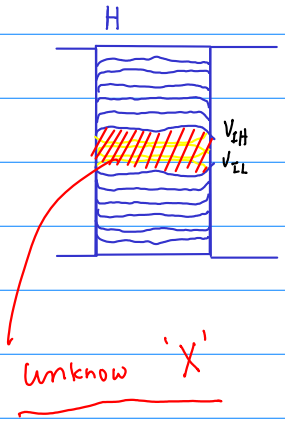


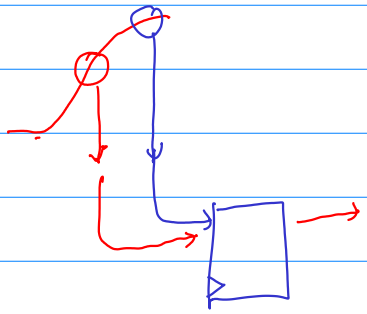






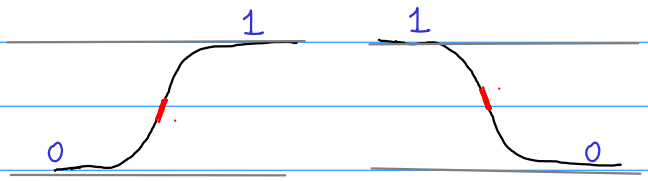






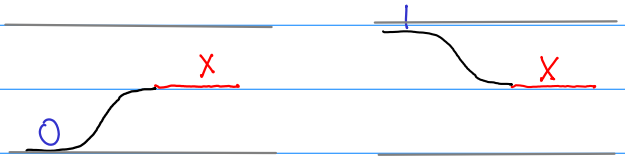
Transient

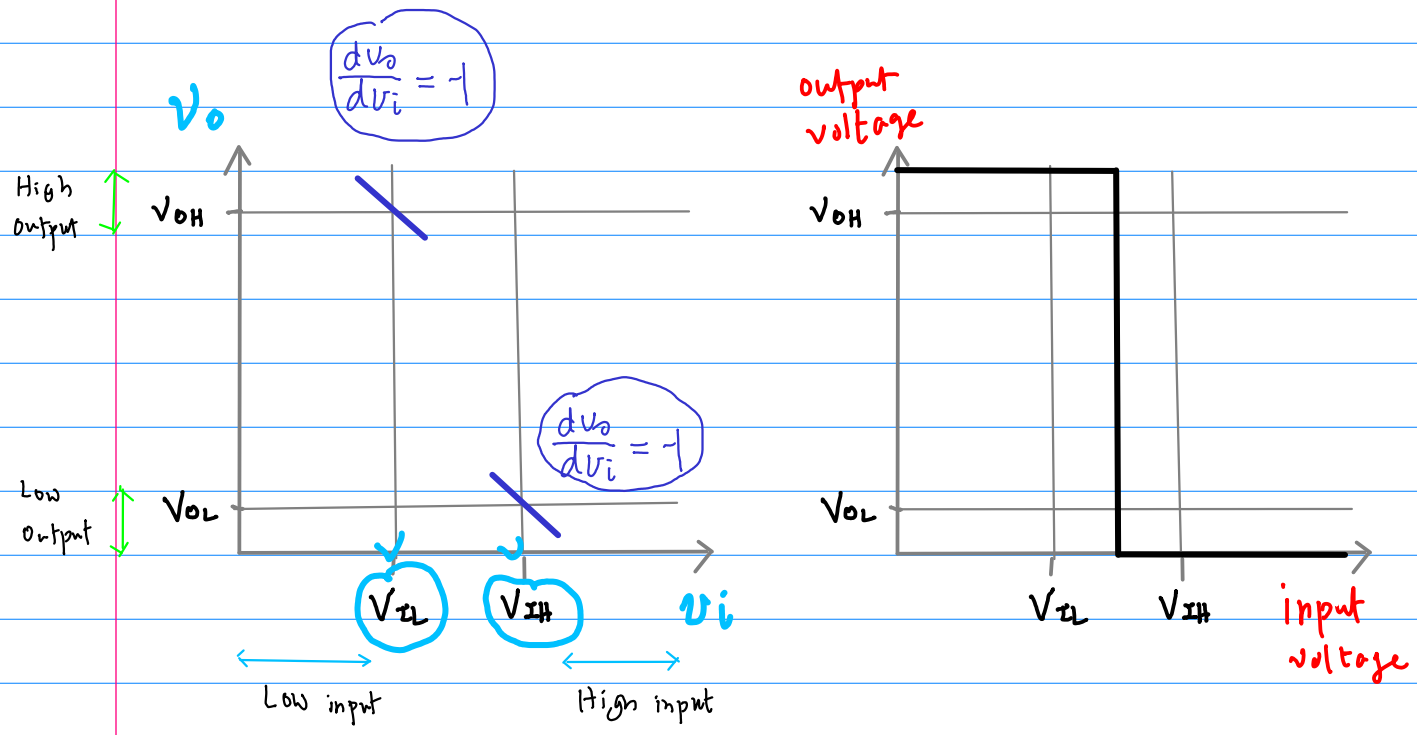
it is ok to have an unknown state for a short period time

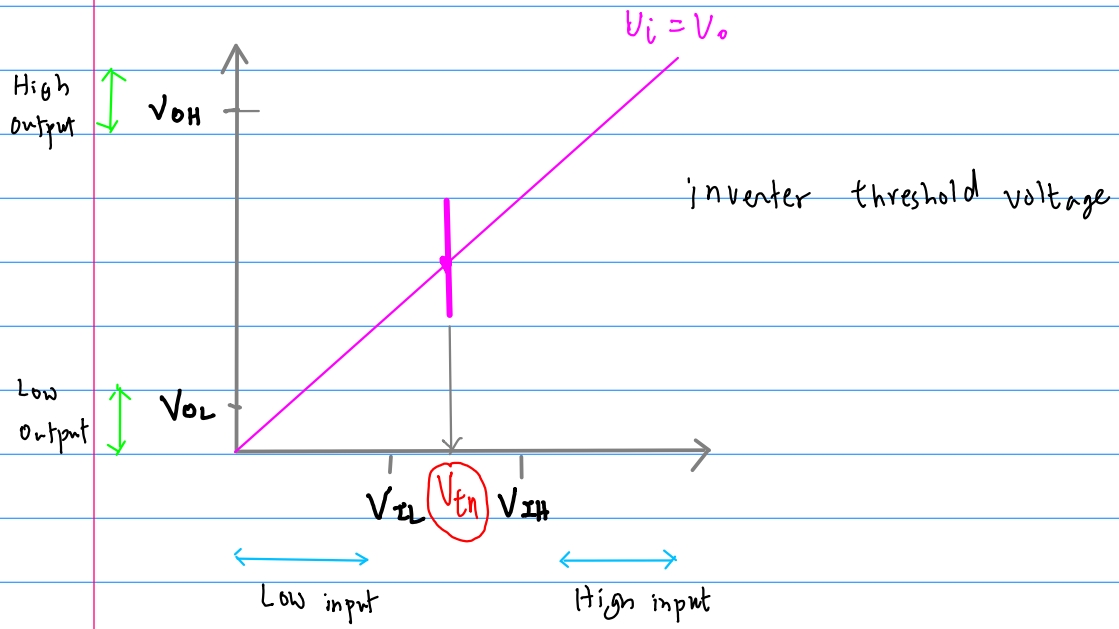


Steady State

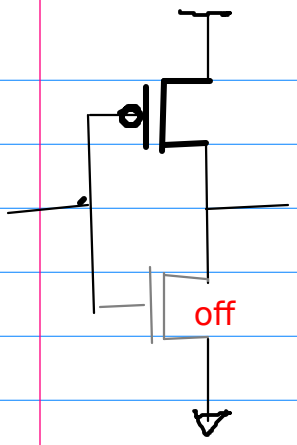
not allowed to have an unknown state as a steady state.







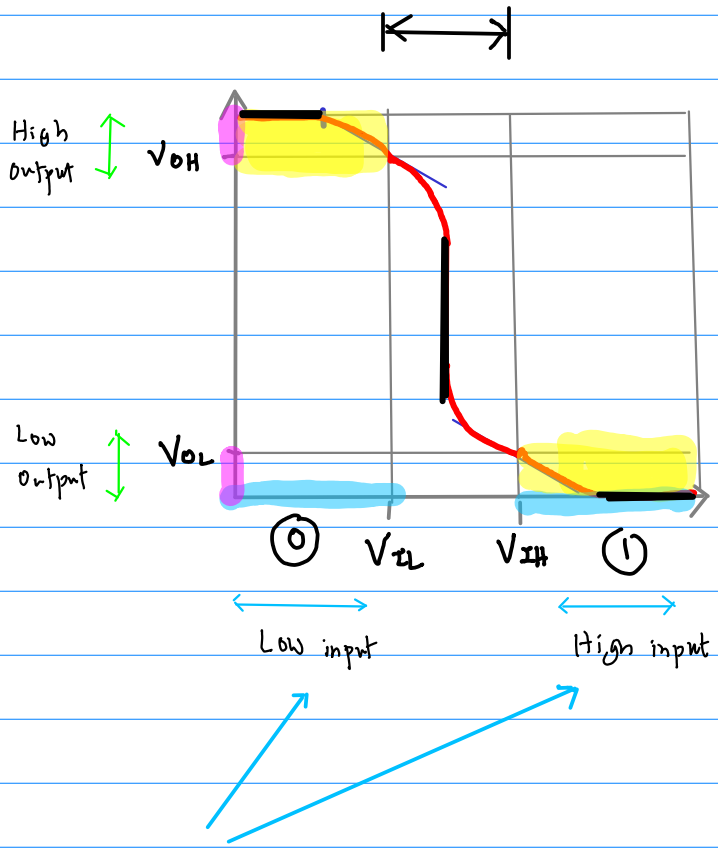
inverter threshold voltage



transient

high gain

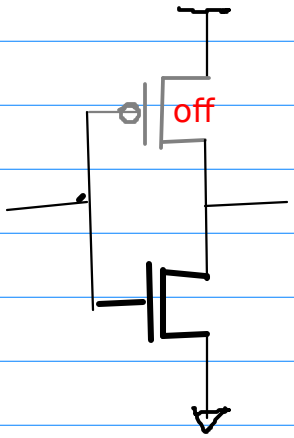
small input change
large output change

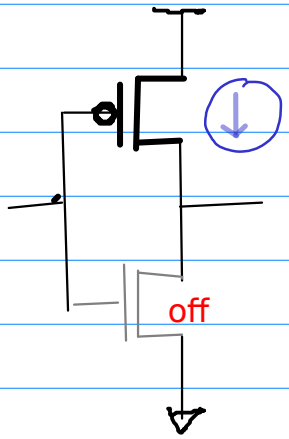


steady state

gain < 1

large input change
small output change

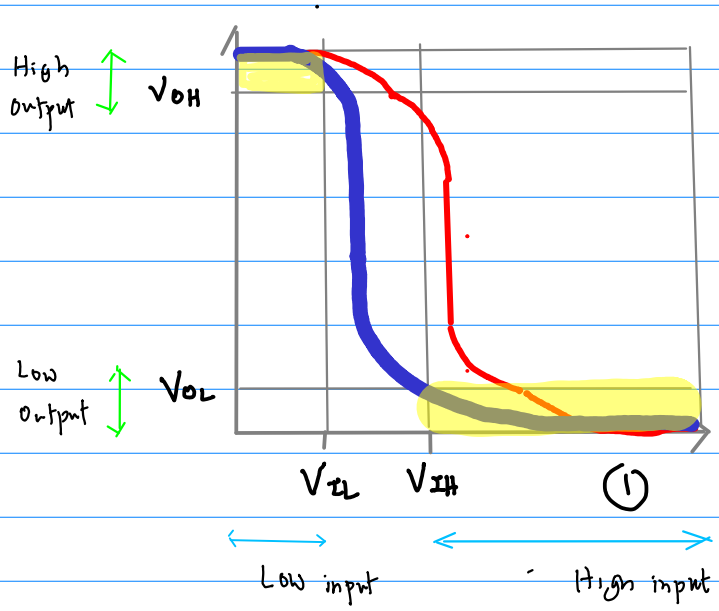




pullup R > pulldown R

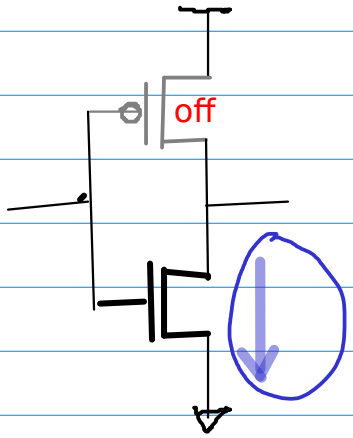
supplies less current

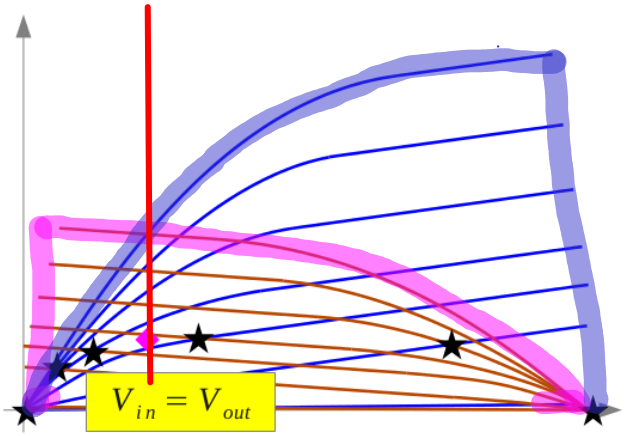
the same size nMOS & pMOS

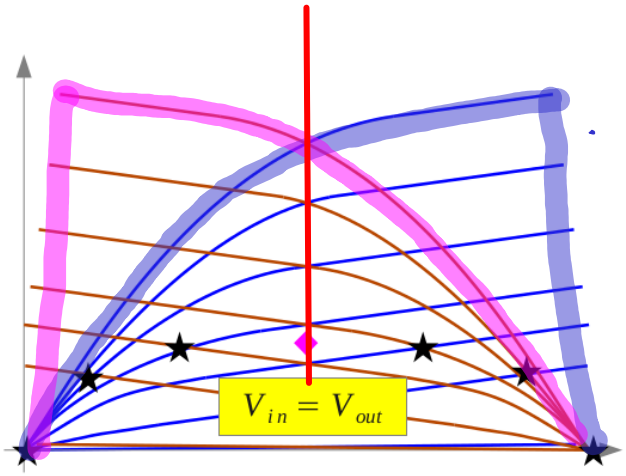


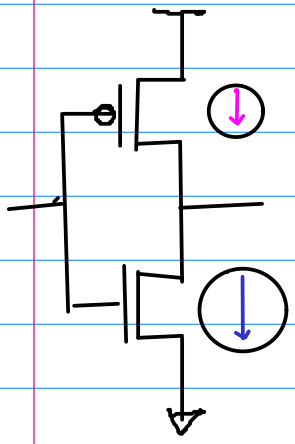
pulldown R < pullup R

supplies more current

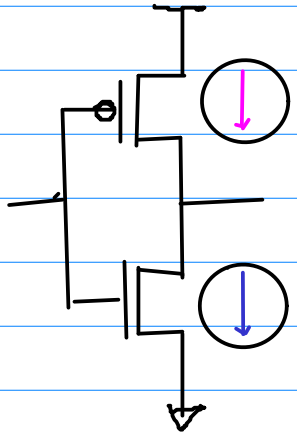




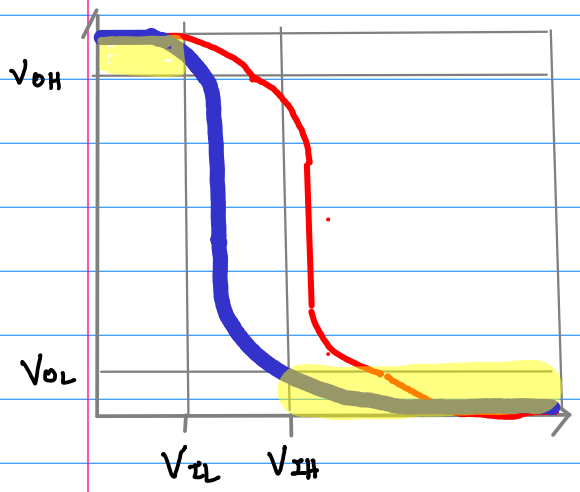


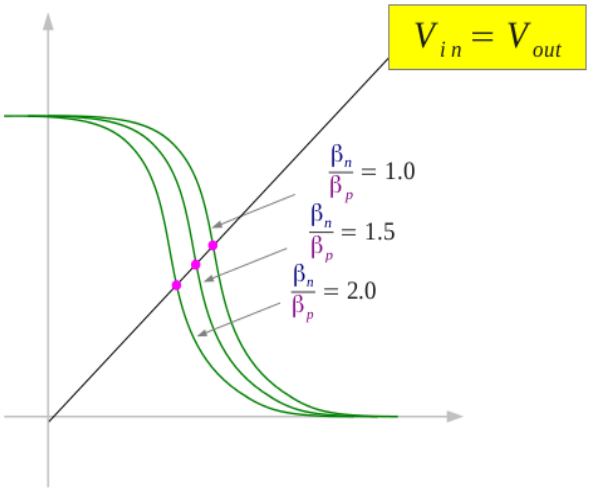


the same size
pMOS, nMOS



double size pMOS
minimum size nMOS

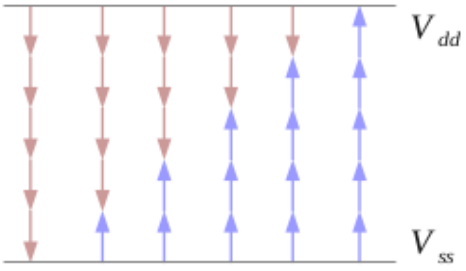


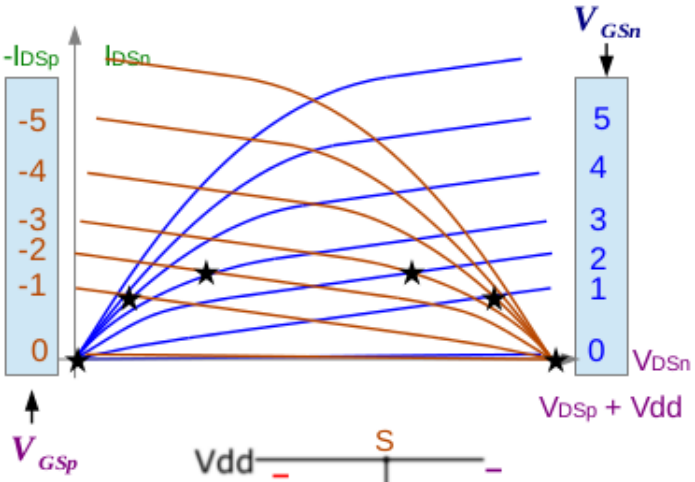


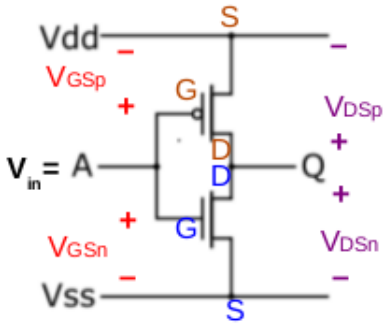
$$V_{in} = V_{GSp} + V_{dd} = V_{GSn} \quad \bigstar$$

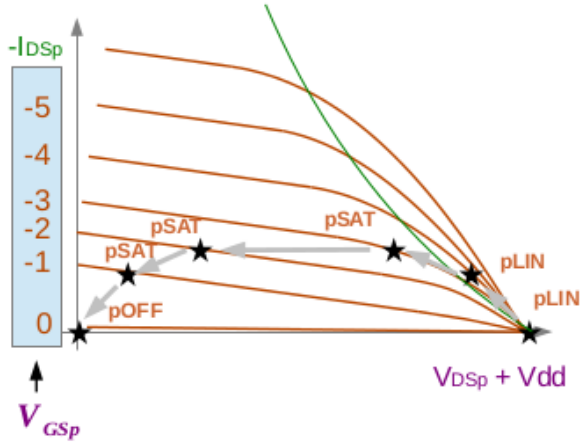
$$V_{out} = V_{DSp} + V_{dd} = V_{DSn}$$

V_{in}	0	1	2	3	4	5
V_{GSp}	-5	-4	-3	-2	-1	0
V_{GSn}	0	1	2	3	4	5



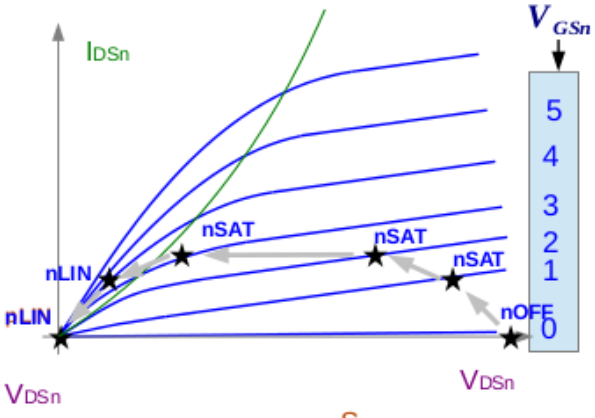


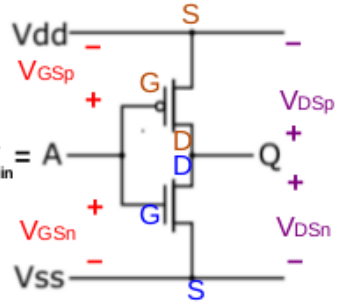




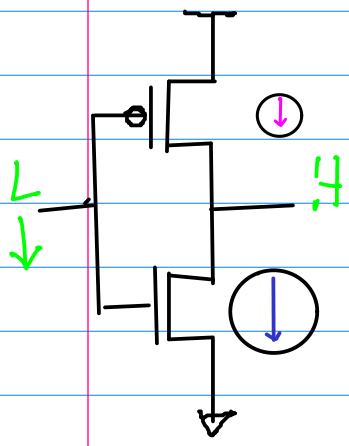
V_{in}	0	1	2	3	4	5
V_{GSp}	-5	-4	-3	-2	-1	0
V_{GSn}	0	1	2	3	4	5

pLIN nOFF	pLIN nSAT	pSAT nSAT	pSAT nSAT	pSAT nLIN	pOFF nLIN





the same size
pMOS, nMOS



Weak pMOS

hard to become "H"

NM $_{L}$

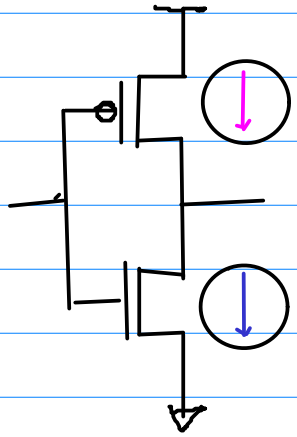
decreased input Vth

to turn off nMOS
Vin have to be
closer to GND

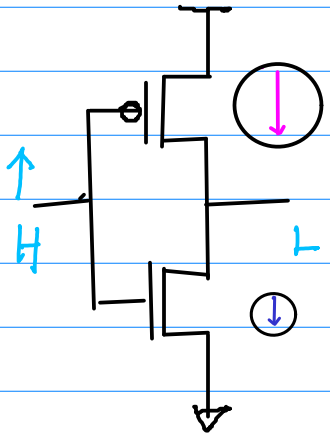
Low Skewed Inverter

fast fall time

double size pMOS
minimum size nMOS



a Unit Inverter



Strong pMOS

hard to become "L"

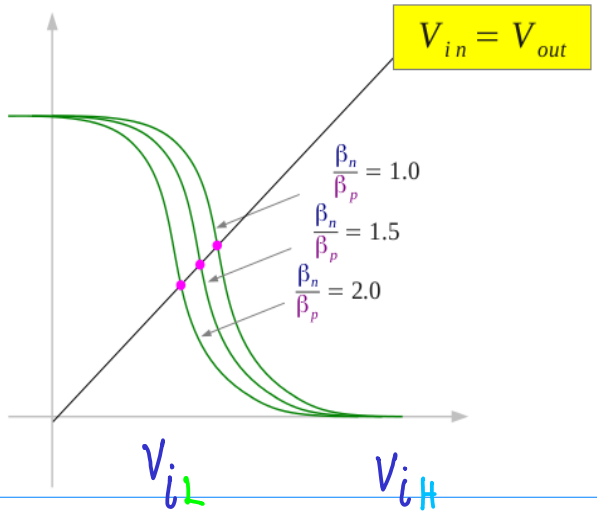
NM $_{H}$

increased input Vth

to turn off pMOS
Vin have to be
closer to Vdd

High Skewed Inverter

fast rising time



large beta_n

Strong PDN

hard to turn off
nMOS transistor

lower input voltage

VTC shifts to the right

large beta_p

Strong PUN

hard to turn off
pMOS transistor

higher input voltage

VTC shifts to the right