Non-volatile Memory based FPGAs (4A)

Young Won Lim
2/15/19

Please send corrections (or suggestions) to youngwlim@hotmail.com.

This document was produced by using LibreOffice.

Young Won Lim
2/15/19

Based on

The VLSI Handbook, edited by Wai-Kai Chen, CRC

Non-volatile Memory based FPGAs

Altera
Based on non-volatile memory for connecting lines

Input/Output control block
Logic block
PIA (Programmable Interconnect Array)

The inputs and outputs of each logic block
Can be connected to bus lines (PIA)

Delays on PIAs are more predictable
Than those of multi-line segments

Logic Block

A logic block contains 16 logic macro cells

Logic array
Programmable Interconnect signals
16 expander product terms
Parallel logic expanders (from other macro cells)
Shared logic expander
Global clear
Global clock
Clear Select, Clock / enable select
Programmable register
To PIA

Using PALs

AMD and Lattice Semiconductor
A different type of non-volatile memory
Using PALs as logic blocks
That can be connected with switch matrices similar to Alter's

References

[1] ftp://ftp.geoinfo.tuwien.ac.at/navratil/HaskellTutorial.pdf
[2] https://www.umiacs.umd.edu/~hal/docs/daume02yaht.pdf