# FPGA Structure (1A)

Young Won Lim 2/6/19 Copyright (c) 2019 Young W. Lim.

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The VLSI Handbook, edited by Wai-Kai Chen, CRC

Fuses or anti-fuses : logic function cannot be changed once realized

RAM to FPGA hardware:

logic function can be easily changed by changing information stored in the RAM

not a straightforward extension to the gate arrays

programmability of an FPGA is comparable to that of a CPU

an FPGA performs much faster than software on computer but slower than ASICs

The layout of a unit is repeated in a matrix form

The unit is consisting of

- PLDs
- Logic gates
- Random access memory
- Non-volatile memory
- Other types of component

A logic block or a logic cell A large number of pre-laid connecting lines

Some call these LBA (Logic Block Array)

# Routing channels in a LBA

- Similar to a gate array
- Similar to sea-of-gate array
- Similar to standard cells
- Bus lines
- Other types of component

A logic block or a logic cell A large number of pre-laid connecting lines

Some call these LBA (Logic Block Array)

# Routing channel similar to gate arrays

#### Routing channel similar to sea-of-gate arrays

### Routing channel similar to standard cell arrays

#### Routing channel similar to bus-based arrays

# Logic Block Structure

- SRAMs for look-up tables
- PALs
- NAND gates
- Multiplexers
- Flip-flops

pre-laid vertical and horizontal lines (short line segments) are connected to the inputs and output of logic blocks by **programmable switches** 

- Fuses, Anti-fuses
- RAM
- Non-volatile memory

Each programmable switch consists of many switching elements typically hundreds of thousands or more switching elements arranging these elements effects the performance, cost, and size Blocks for inputs to receive signals from the outside of the FPGA Blocks for outputs to send signals to the outside Blocks for inputs to receive signals from the outside of the FPGA Blocks for outputs to send signals to the outside Logic functions can be realized by writing design information into SRAM and flip-flops

Complex logic functions requires a large number of logic gates PALs and other types of FPGA are suitable

Quick realization of complex logic function is possible with SRAM based FPGAs

If the power supply is turned off all the information is lost

the design information must be re-written each time the power is turned on

Compared to the mask programmable gate arrays the chip size is larger the speed is slower

Compared to software run on the general computer the speed is faster

#### References

- [1] ftp://ftp.geoinfo.tuwien.ac.at/navratil/HaskellTutorial.pdf
- [2] https://www.umiacs.umd.edu/~hal/docs/daume02yaht.pdf