Latch Based Design (1A)

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Latch vs Flipflop (1)

[Latch] less gates, less area, less power
[F/F] more gates, more area, more power

[Latch] for non-timing critical design ← less gates & less power
[F/F] for non-power aware design

Latch vs Flipflop (2)

[Latch] it is an asynchronous block
must ensure its input is race free otherwise glitch, hazard
[F/F] synchronous block

[Latch] weak to noise, specially noisy “enable” input disrupts output
[F/F] robust to noise

[Latch] difficult timing analysis
[F/F] easy timing analysis

[Latch] difficult DFT
Lockup state needed at the clock domain crossing
[F/F] Scanned F/F

Latch vs Flipflop (3)

[Latch] soft barrier – sensitive to the pulse duration
Signals propagates on the transparent period
[F/F] hard barrier – sensitive to the pulse transition
Signals propagates only on the pos. or neg. edge

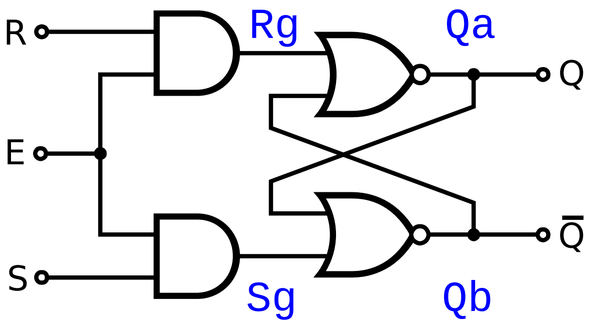
[Latch] pipeline with master-slave latches
logic can be added between both of edges
[F/F] logic can be added between the same single edge

[Latch] Cycle-borrowing can be used to extend setup time
[F/F] time may be wasted because of

[Latch] insensitive to clock skews, wire load model, PVT models
[F/F] sensitive to clock skews, wire load model, PVT models

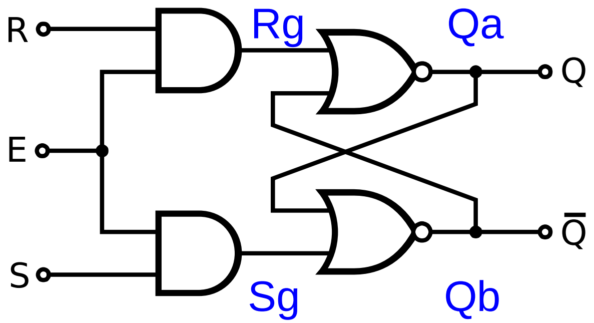
Latch vs Flipflop (1)

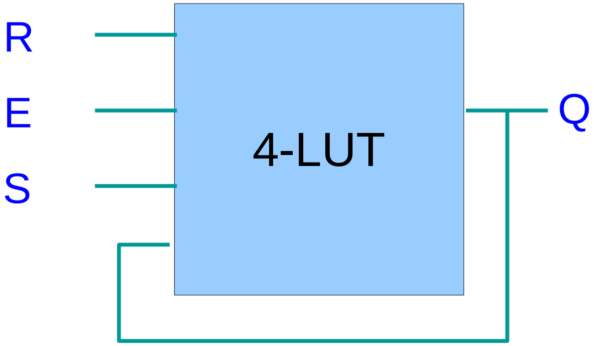
```
- - A gated RS latch
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY RSLatch IS
PORT ( E, R, S      : IN    STD_LOGIC;
       Q            : OUT   STD_LOGIC );
END part1;


ARCHITECTURE Structural OF RSLatch IS
    SIGNAL Rg, Sg, Qa, Qb : STD_LOGIC ;
    ATTRIBUTE keep : boolean;
    ATTRIBUTE keep of Rg, Sg, Qa, Qb : SIGNAL IS
true;
BEGIN
    Rg <= R AND E;
    Sg <= S AND E;
    Qa <= NOT (Rg OR Qb);
    Qb <= NOT (Sg OR Qa);

    Q <= Qa;
END Structural;
```

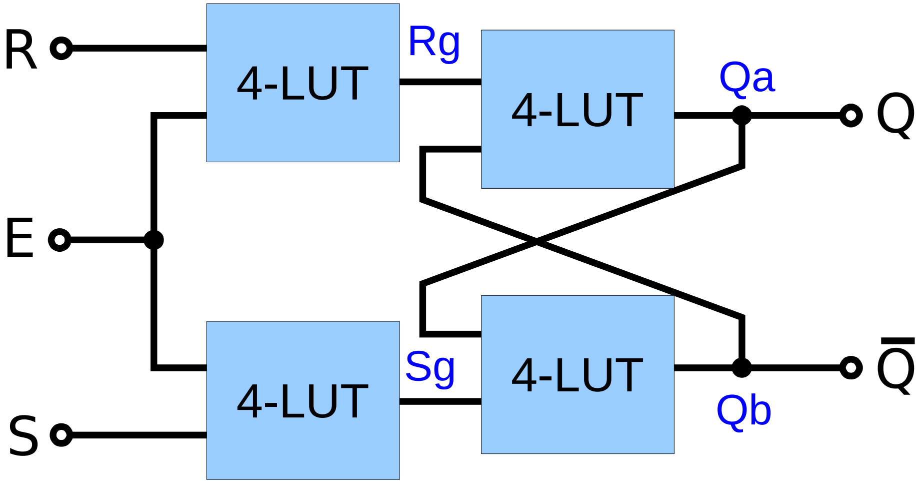


ftp://ftp.altera.com/up/pub/Altera_Material/10.1/Laboratory_Exercises/Digital_Logic/DE2/vhdl/lab3_VHDL.pdf
https://en.wikipedia.org/wiki/File:SR_%28Clocked%29_Flip-flop_Diagram.svg

Gate Level RS Latch – FPGA realization







Impulse Matching (N>M) (1)

```
- - A gated RS latch
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY RSLatch IS
PORT ( Clk, R, S   : IN    STD_LOGIC;
       Q           : OUT   STD_LOGIC );
END part1;


ARCHITECTURE Structural OF RSLatch IS
    SIGNAL Rg, Sg, Q, Qb : STD_LOGIC ;
    ATTRIBUTE keep : boolean;
    ATTRIBUTE keep of Rg, Sg, Qa, Qb : SIGNAL IS
true;
BEGIN
    Rg <= R AND Clk;
    Sg <= S AND Clk;
    Qa <= NOT (Rg OR Qb);
    Qb <= NOT (Sg OR Qa);

    Q <= Qa;
END Structural;
```

Latch Modeling in VHDL

```
--
-- Latch with Positive Gate
–

library ieee;
use ieee.std_logic_1164.all;

entity latch is
  port(G, D : in std_logic;
          Q : out std_logic);
end latch;

architecture beh of latch is
begin
  process (G, D)
  begin
    if (G='1') then
      Q <= D;
    end if;
  end process;
end beh;
```

Latch Modeling in VHDL

```
--
-- Latch with Positive Gate and
–– Asynchronous Reset
--

library ieee;
use ieee.std_logic_1164.all;

entity latch_ar is
  port(G, D, CLR : in std_logic;
               Q : out std_logic);
end latch_ar;

architecture beh of latch_ar is
begin
  process (CLR, D, G)
  begin
    if (CLR='1') then
      Q <= '0';
    elsif (G='1') then
      Q <= D;
    end if;
  end process;
end beh;
```

Impulse Matching (N>M) (1)

```
- - A gated RS latch
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY RSLatch IS
PORT ( Clk, R, S   : IN    STD_LOGIC;
       Q           : OUT   STD_LOGIC );
END part1;


ARCHITECTURE Structural OF RSLatch IS
    SIGNAL Rg, Sg, Q, Qb : STD_LOGIC ;
    ATTRIBUTE keep : boolean;
    ATTRIBUTE keep of Rg, Sg, Qa, Qb : SIGNAL IS
true;
BEGIN
    Rg <= R AND Clk;
    Sg <= S AND Clk;
    Qa <= NOT (Rg OR Qb);
    Qb <= NOT (Sg OR Qa);

    Q <= Qa;
END Structural;
```

Impulse Matching (N>M) (1)

latches nominally "simpler" than flip-flops

in Xilinx FPGAs:

- 2 FFs/CLB which can be used
- latch requires FG function generator

* for FPGA targets, use flip-flops as sequential elements in VHDL description

http://www.ohio.edu/people/starzykj/network/class/ee690/slides/fpgasynth.pdf

References

[1] http://en.wikipedia.org/

[2] A.K. Rohilla, Latch is not that BAD - Latch Vs Flip-flop, http://electronicsforu.com/electronicsforu/

[3] lab3_VHDL.pdf, ftp://ftp.altera.com/up/pub/Altera_Material/10.1/Laboratory_Exercises