2. HW/SW Co-design

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Outline

Based on

"Software Engineering for Embedded Systems. . .", R Oshana and M Kraeling, 2013

Prototyping decision criteria

- time of availabiliy during a project
- speed
- accuracy
- capacity
- development cost and bring-up time
- replicaton cost
- software debug, hardware debug, and execution control
- system connections
- power analysis
- environment complexity

Choosing the right prototype
early availability speed hw accuracy hw debug sw debug execution
control effort of extra development cost of replication

A1

virtual prototyping rtl simulation acceleration emulation FPGA based prototyping silicon

A1

Traditional Sequential Design Flow integrate SW & HW, after HW prototype / devel board is available

A1

Virtual Prototype a part of architectural design easy dilivery of software devel prototype pre-silicon SW devel incremental refining of the virtual prototype

A1

- software functional description
- hardware design : single, multi core SoC, I/O, interface
- working on PC, workstation
- proper simulation speed
- detailed simulation of drivers, OS, applications

A1

- simulation speed $<$ 10 * actual exec time
- depends on the abstraction level
- affects the accuracy of a prototype

A1

- to be effective, use at the very early stage of design process
- virtual prototype for hw designer
- support mixed signal SoC design flow
- rtl design
- verification

A1

- simulation acceleration technique
- loop integration?
- low power design
- architecture selection
- good design
- debugger
- verification process

A1

- hw sw interface
- TI Code Composer Studio
- ARM Realview
- GNU tool chain
- other debugging environment

- software product binary compatibility
- cycle accurate modeling not necessary

History

- pre-silicon software
- virtualization of hardware
- to avoid bug in later stage
- to start sw devel as early as possible

-Proprietary

- AXYS
- VaST
- Virtuech
- Virtio
- Motorolla MOOSE
- EDA CoWare. Synopsys, Mentor, Cadence
- architecture exploration
- hw / sw co-design

A1

- initial functions of SystemC
- limited support for embedded sw devel
- OSCI Transaction Level Modeling Working Group
- various levels of abstraction

- 2006 Proprietary + OSCI SystemC
- ARM acquired AXYS
- Synopsys acquired Virtio
- CoWare
- no outstanding result
- slow response of the market
- compatible standardization
- virtual prototype

- Proprietery
- OSCI TLM Working Group
- TLM-2.0 API
- temporary decoupling
- DMA interface
- timing
- LT (Loosely Timed)
- AT (Approximately Timed)

A1

- LT Modeling - blocking interface - temporary decoupling
- blocking
- timing return
- Abstraction Level
- before silicon, enable SW development
- near real-time performance simulation
- requires abstraction for the unnecessary details
- quick generation of models
- high performance in simulation
- Classificaiton of TLM by timing accuracy
- Cycle Accurate
- AT
- LT

A1

- communication model
- instead of pins and wires
- describe inside transaction flow
- enhance the simulation speed

-AV (Applicaiton View) -LT (Loosely Timed) -AT (Approximately Timed) -CA (Cycle Accurate)

A1

- Virtual Prototyping
- FPGA-based Prototyping
- Emulation
- RTL Simulation
- Application SW Development (Platform Level)
- Firmware Development
- Speed, Visibility
- Accuracy
- System level
- Implementation level

A1

- Architecture Virtual Prototype
- initial phase
- proper level of accuracy
- performance parameters

A1

- Software Virtual Prototype
- OS booting
- Porting Application SW
- Boot loading routine
- OS model