Logic Families Dynamic-2 (H.2)

20151215

References

Some Figures from the following sites

[1] http://pages.hmc.edu/harris/cmosvlsi/4e/index.html
Weste & Harris Book Site

[2] en.wikipedia.org

[3] Digital Integrated Circuits : A Design Perspective,
Jan M. Rabaey,
(http://bwrcs.eecs.berkeley.edu/Classes/IcBook/)

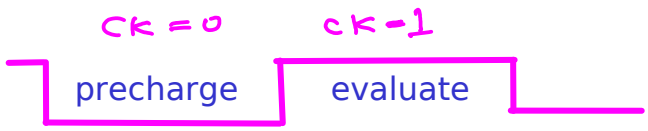
[4] Digital Electronics and Design with VHDL
Pedroni

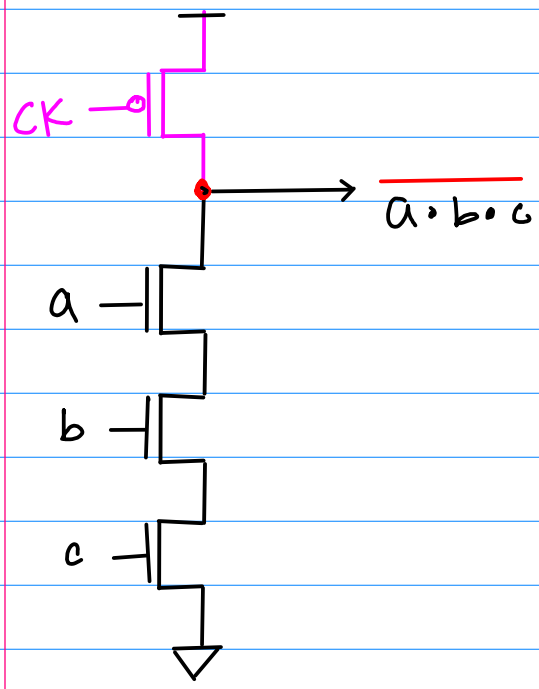
Other MOS Archtectures

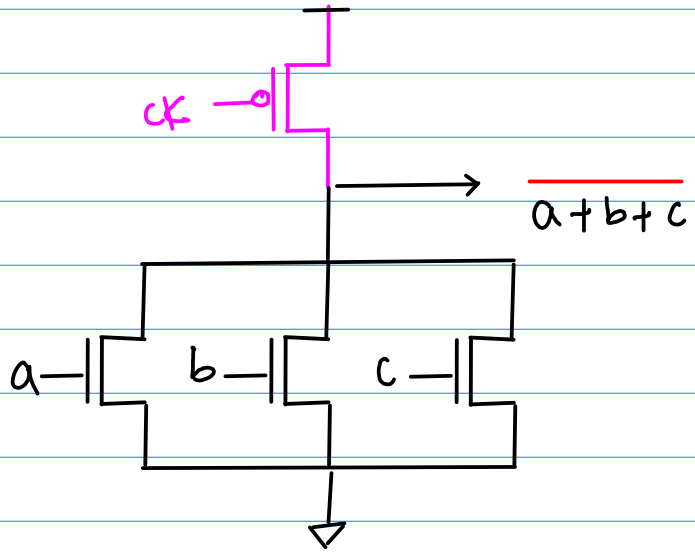
Static MOS
- Pseudo-nMOS Logic
- Transmission-gate Logic
- BiCMOS Logic

Dynamic MOS
- Dynamic Logic
- Domino Logic
- C2MOS Logic

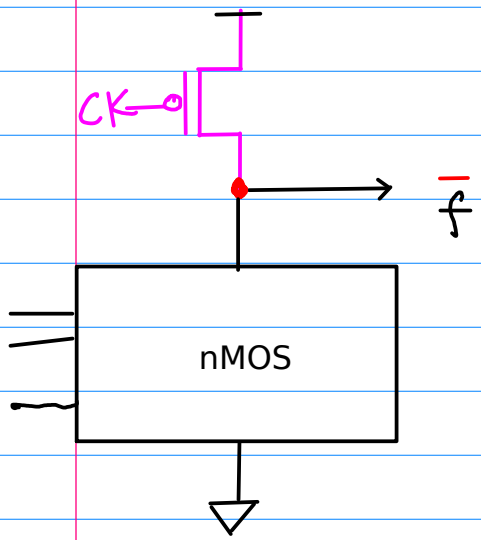
Dynamic Logic







a clocked strong pull-up pMOS



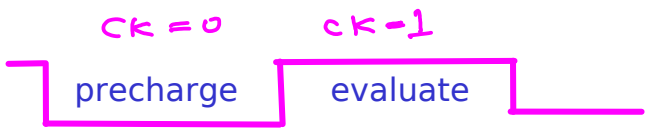
precharge
(clock=0)
pMOS ON
precharge output

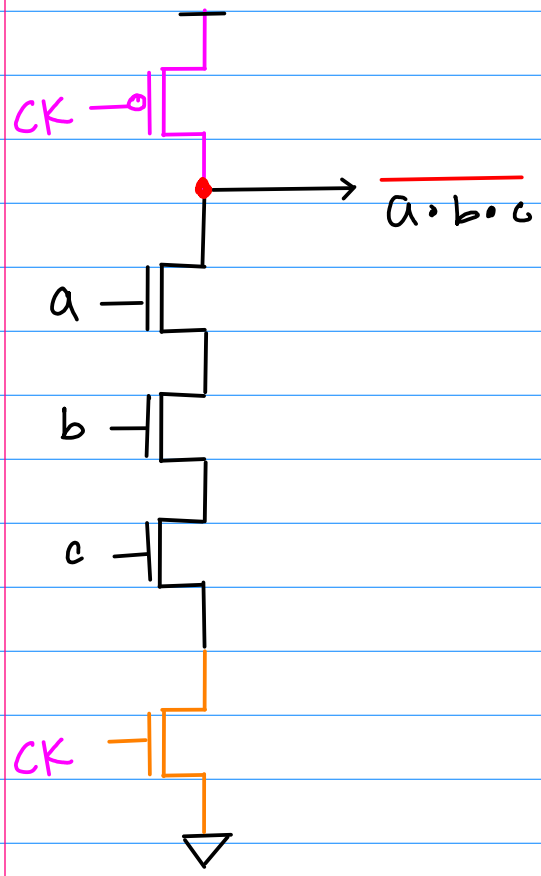
evaluation
(clock=1)
nMOS ON
conditionally
discharged

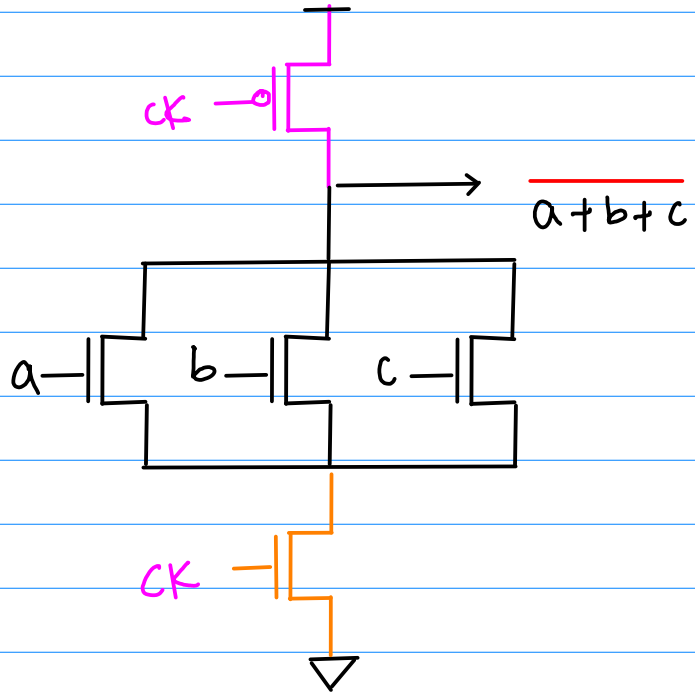
compared to pseudo-nMOS,

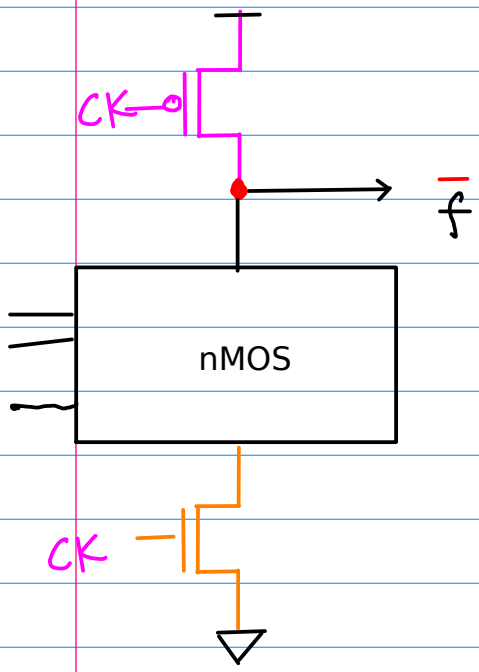
smaller static power consumption
pMOS ON only while clock=0
faster rising time
larger W/L, smaller R

Footed Dynamic Logic





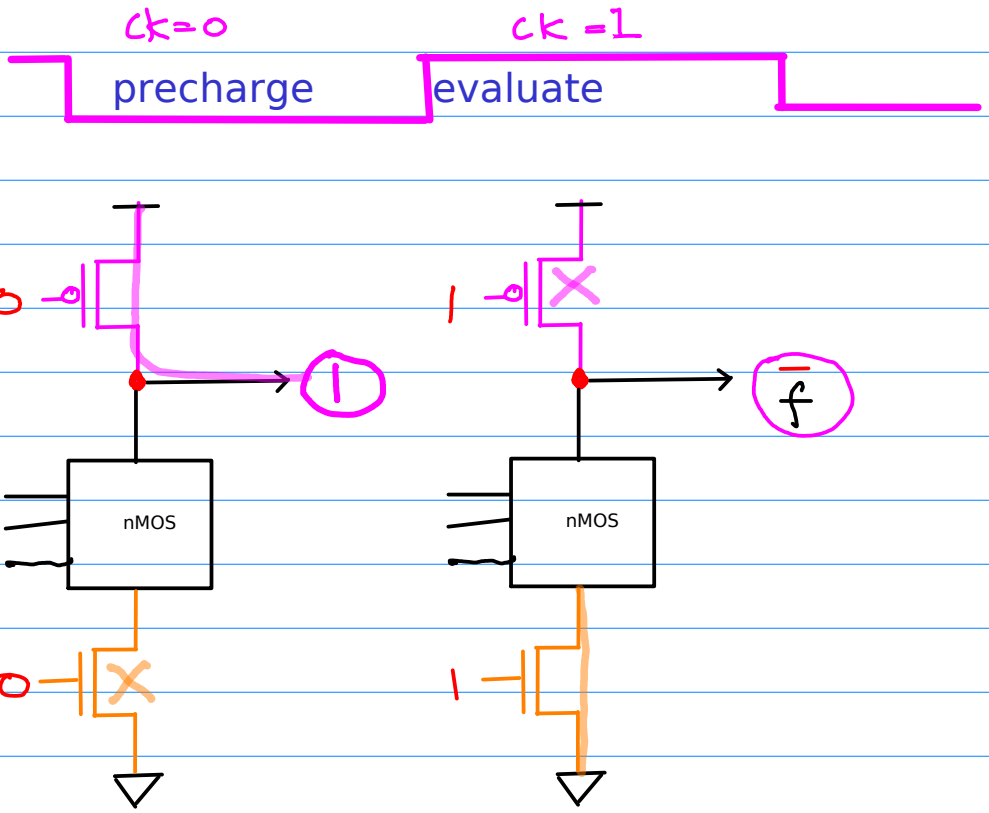




both power supply connections clocked

more faster output transition
nearly zero static power consumption

slightly more complex circuit
heavy loaded clock



every output will
be pulled up to Vdd
during precharge

since these outputs
feed the inputs of
other logic gates

all inputs are assumed
to be 'H' during precharge
but no conditional
discharge

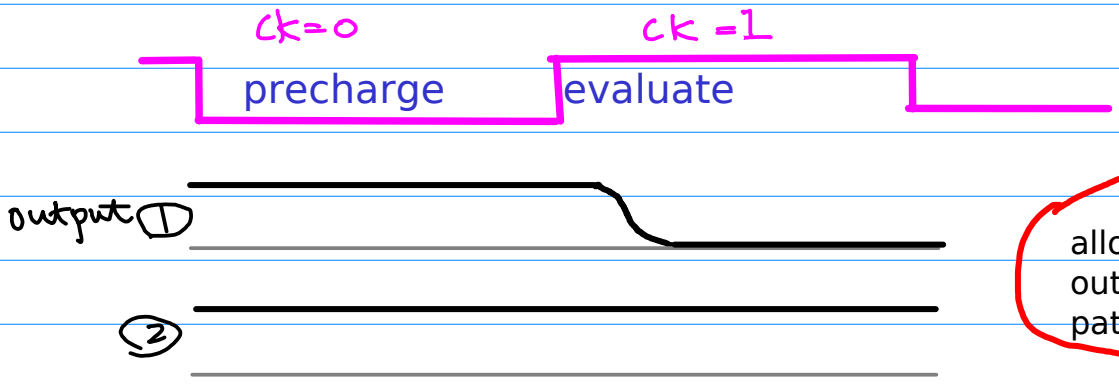
precharge pMOS : On
footed nMOS : Off

now every output that
were forced to be held as 'H'
during precharge,
evaluates their real values,
through conditional discharging
according to their inputs

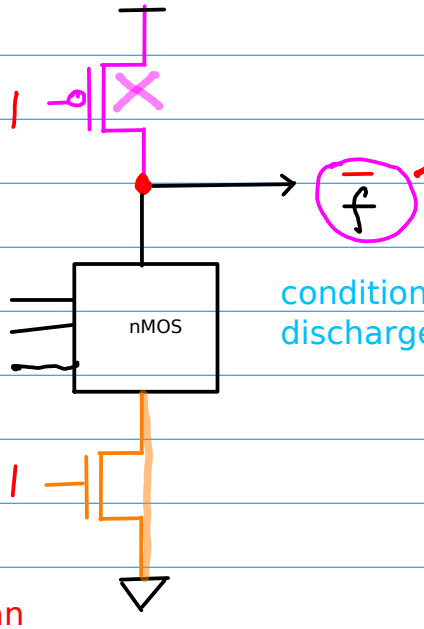
However, during evaluation
phase, no pulling up is allowed.

So the allowed output
transition is only 1->0 (falling)

0->1 transition is not possible



allowed output patterns



0 to 1 inputs are always OK

some inputs turns on nMOS to be connected to the ground

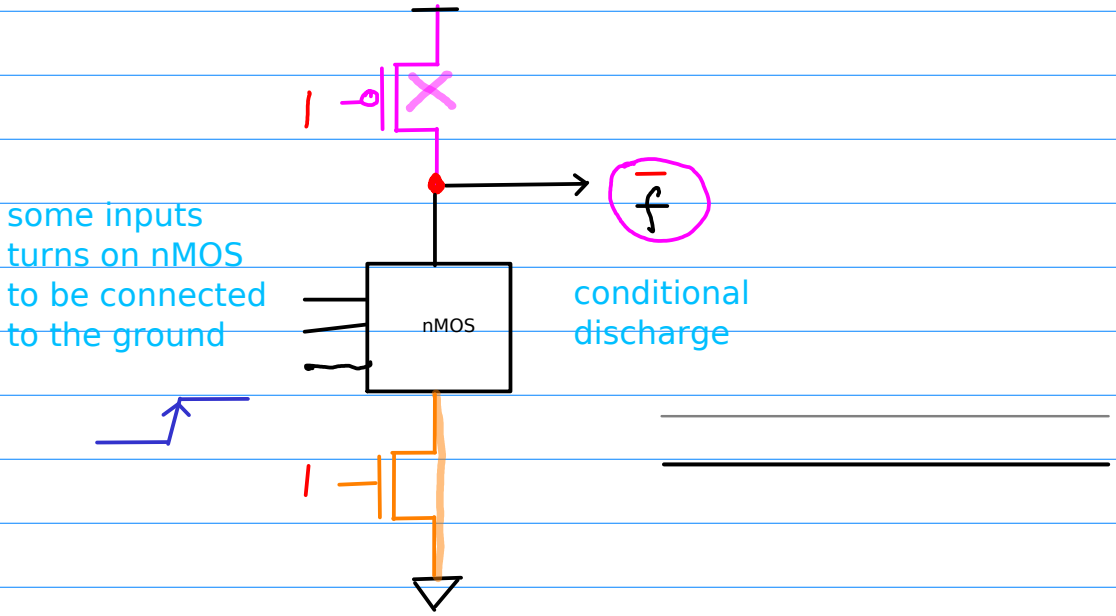
conditional discharge

normally the logic value will be pulled up by the pMOS during the precharge

1 to 0 inputs will turn off nMOS

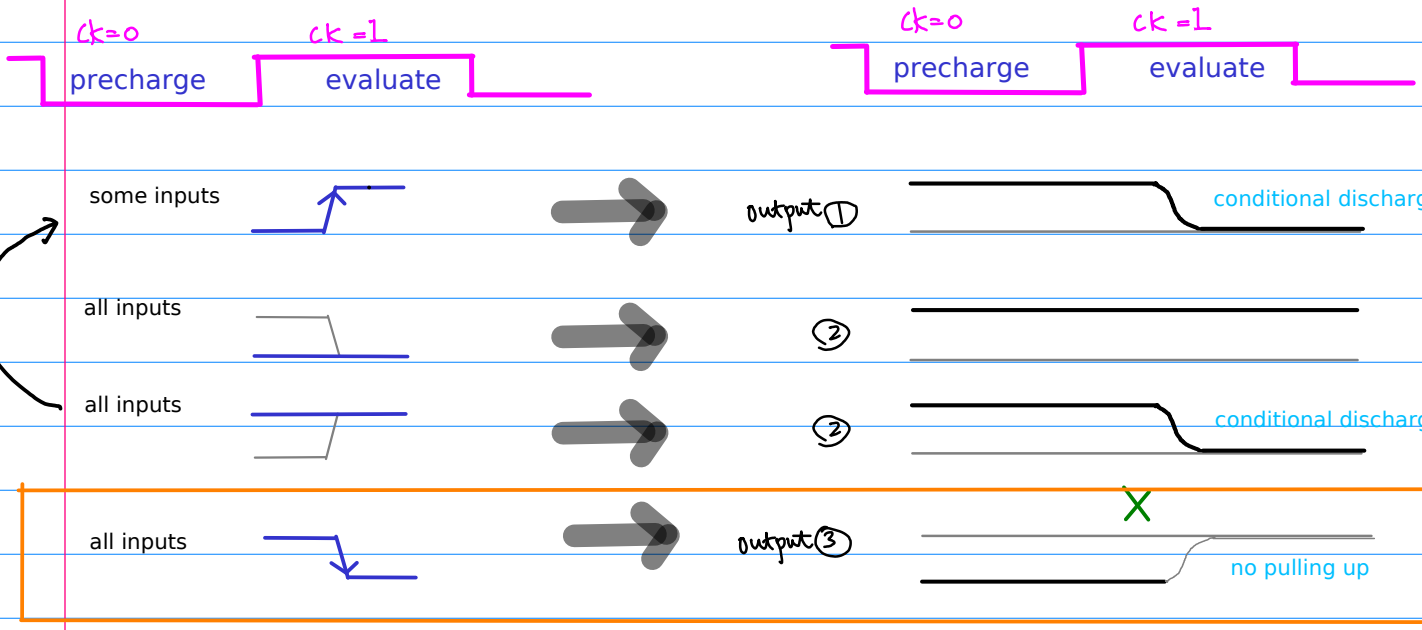
sometimes this can make 0->1 output transition that is not allowed

but the evaluate phase of the Domino Logic, pMOS is always turned off, thus no pulling up possible

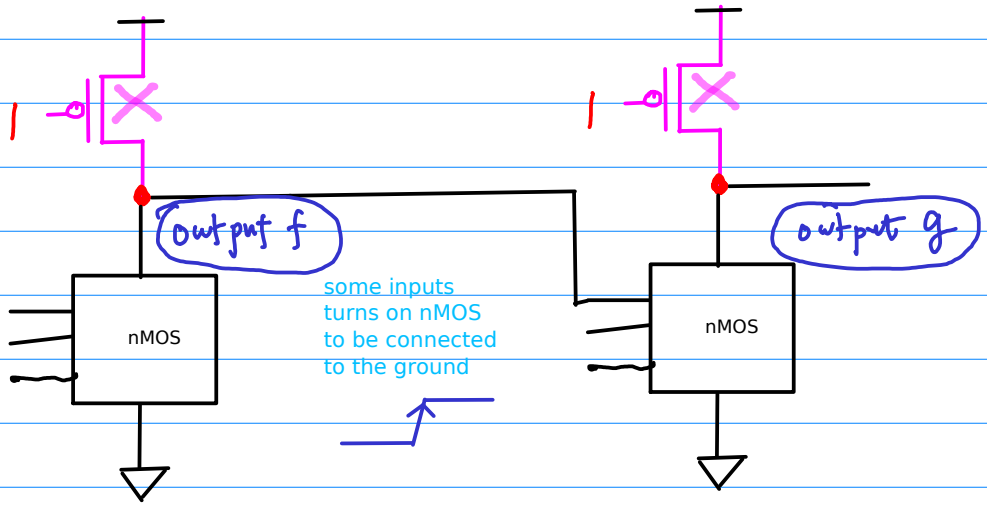


input transitions

output transitions

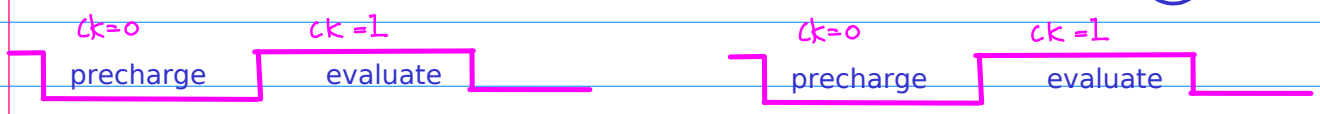


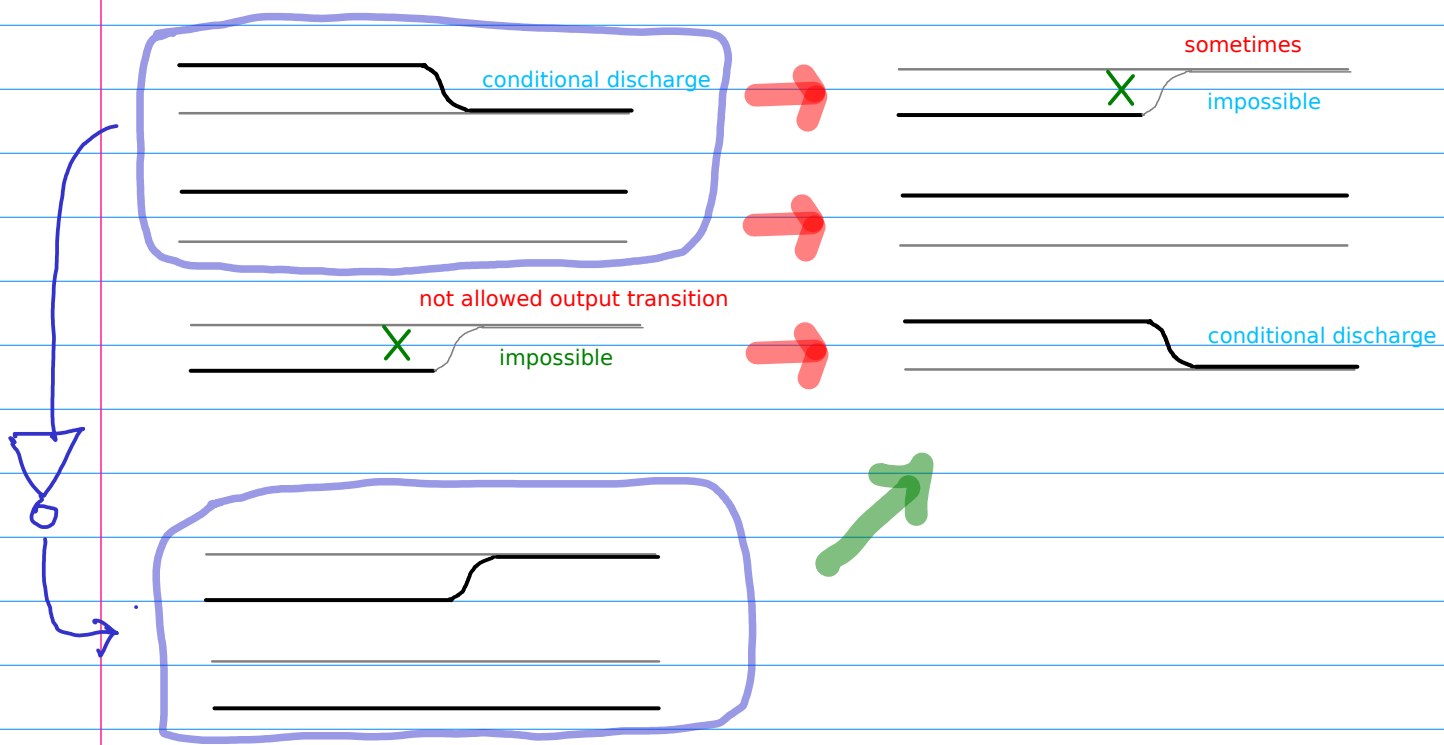
therefore, prevent the last case

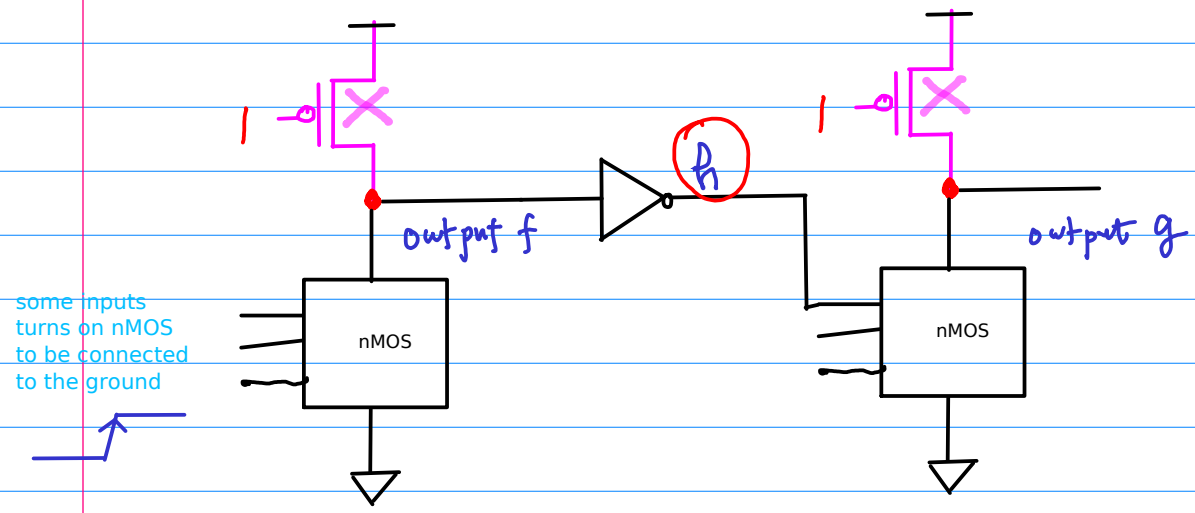


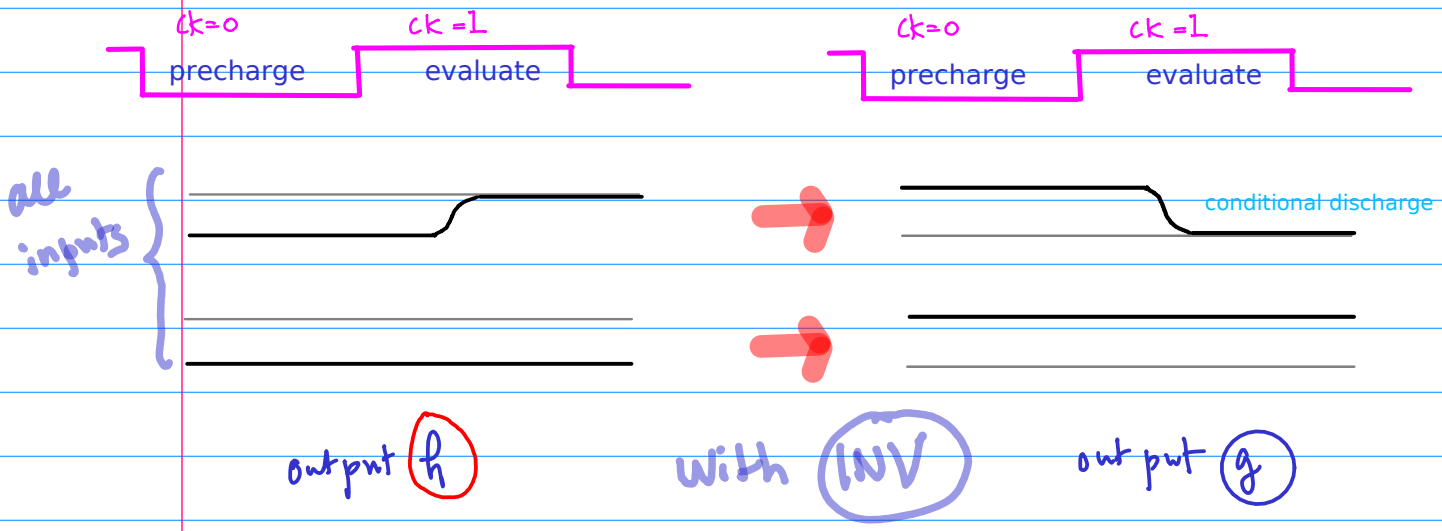
output f

output g

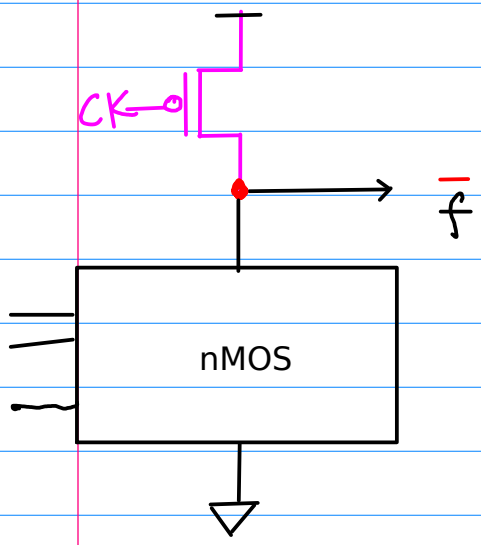





1
output f
h
1
output g
nMOS
nMOS
some inputs
turns on nMOS
to be connected
to the ground


ck=0
precharge
ck=1
evaluate
ck=0
precharge
ck=1
evaluate
all inputs
conditional discharge
output h
with INV
output g

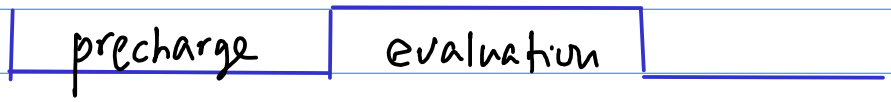
Monotonicity Condition

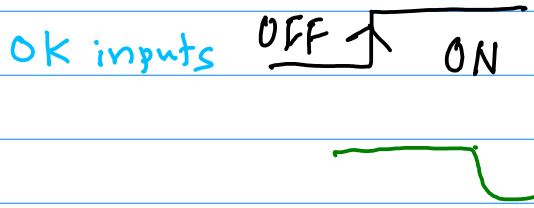


foot, unfoot

both dynamic logic has a problem when the output of the one gate must be connected to the input of another

-- use domino logic



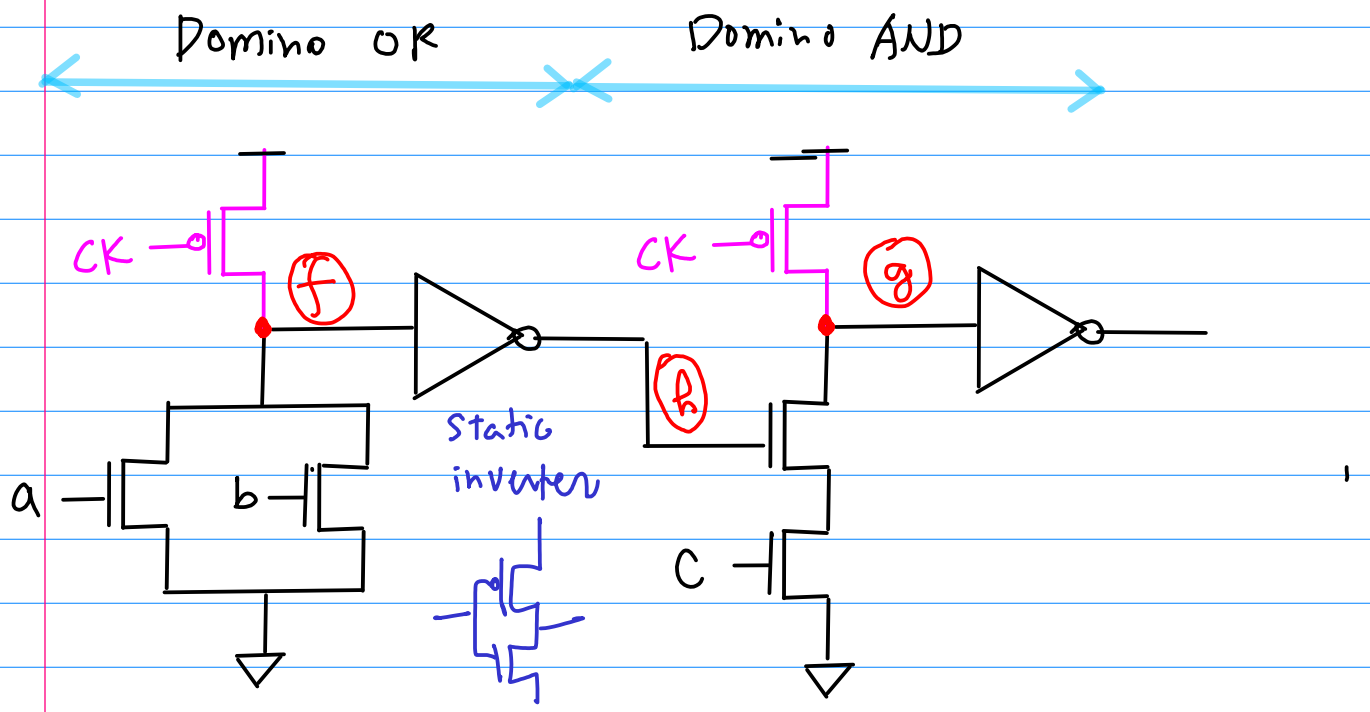


Domino Logic

Never allow input transition from H to L
Then only the allowed output transitions will result

Monotonicity Condition
the inputs are required to be monotonically rising

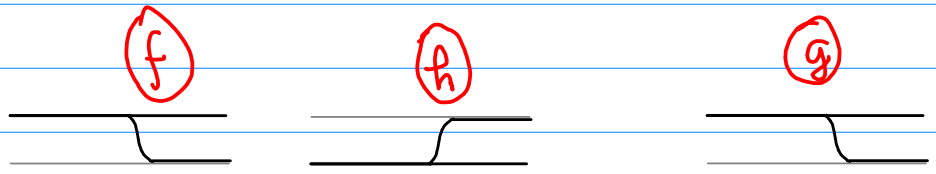
Domino Logic



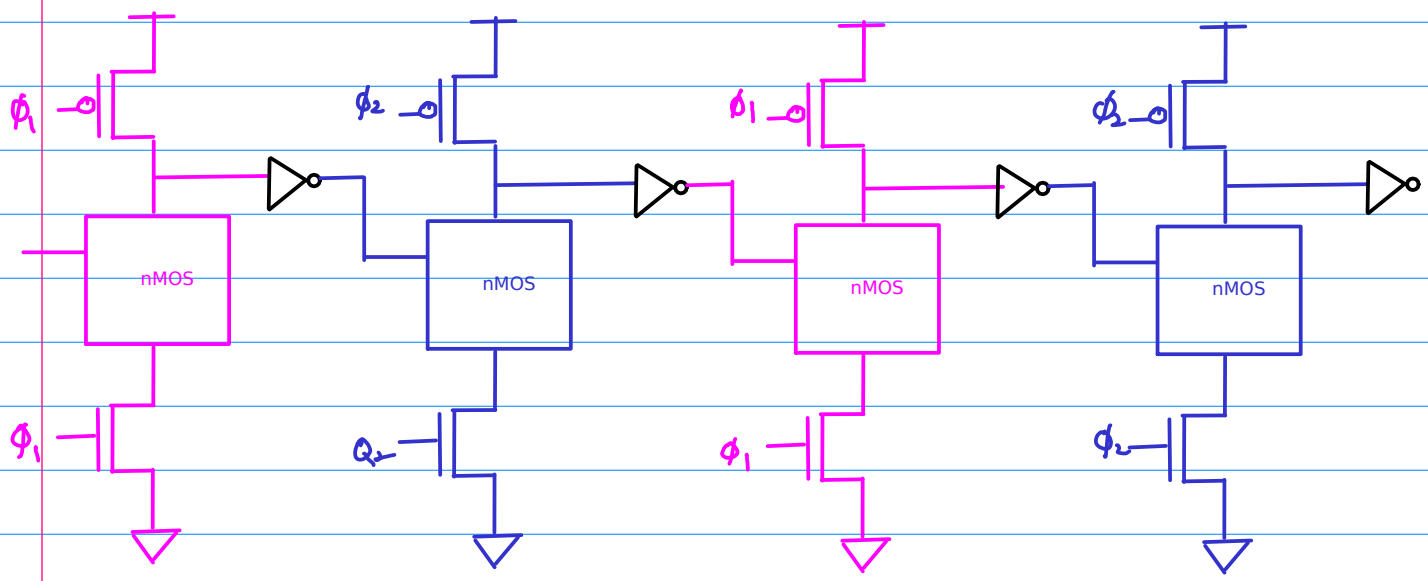
static inverters between dynamic stages

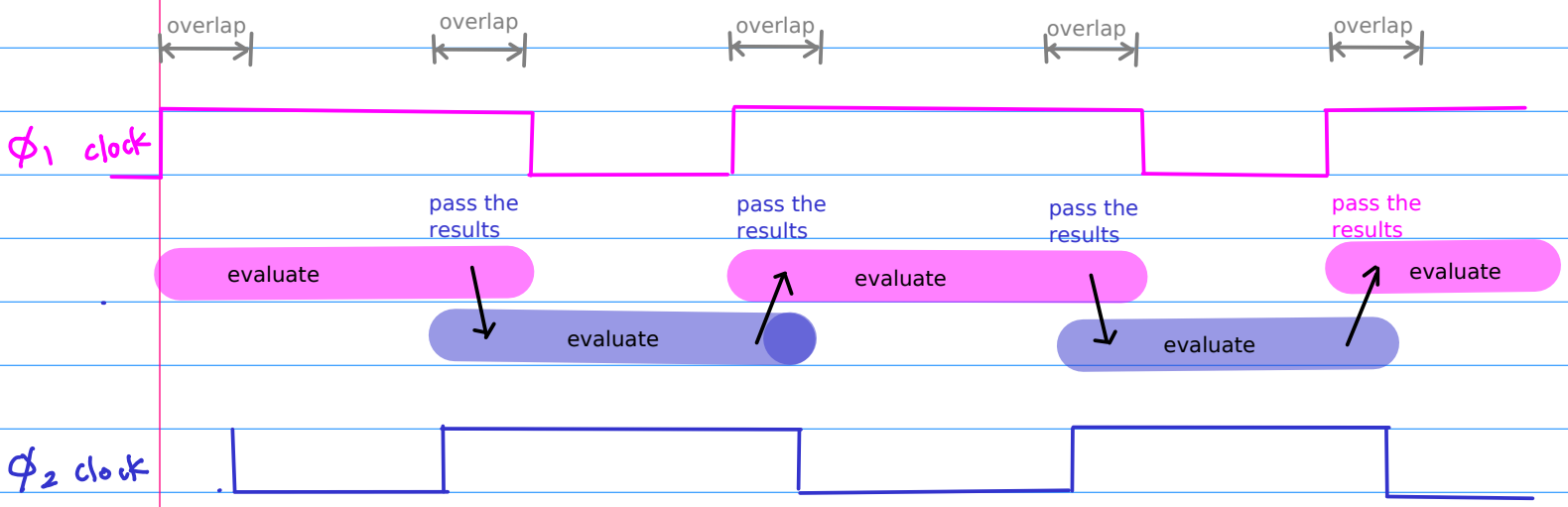
during precharge phase, the output becomes H by the pull-up transistor, and the inverter's output becomes L

this L stays or change to H during evaluation phase
therefore, the undesirable H-to-L transition is avoided



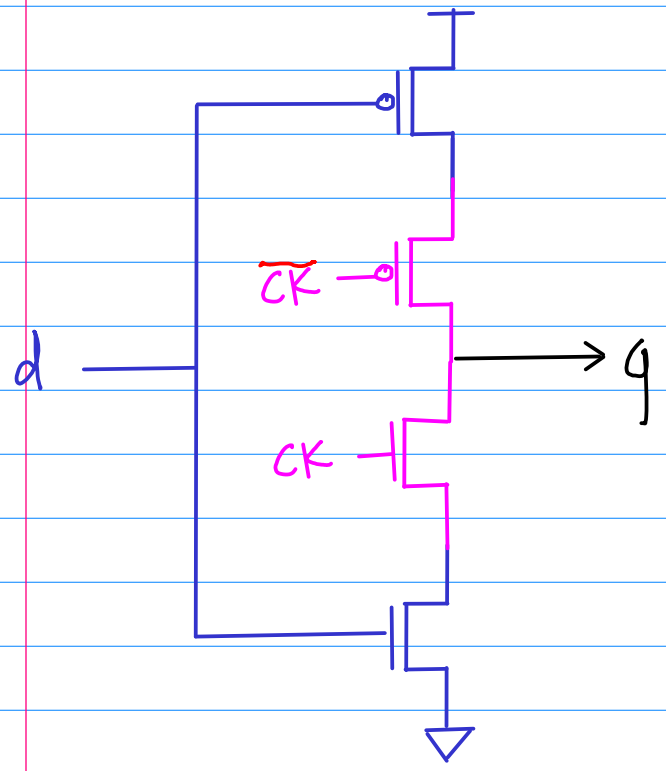
Pipeline





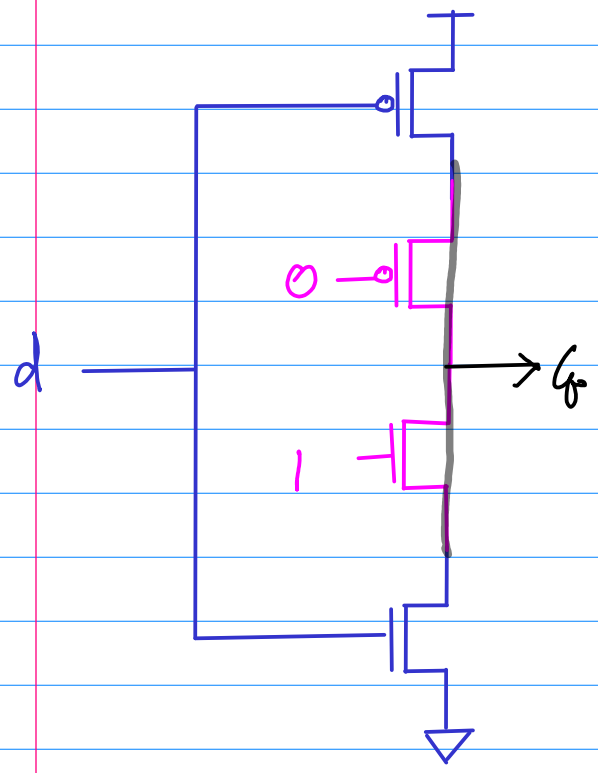
Without FF's & latches, a pipeline can be constructed

Clocked CMOS Logic (C^2MOS)



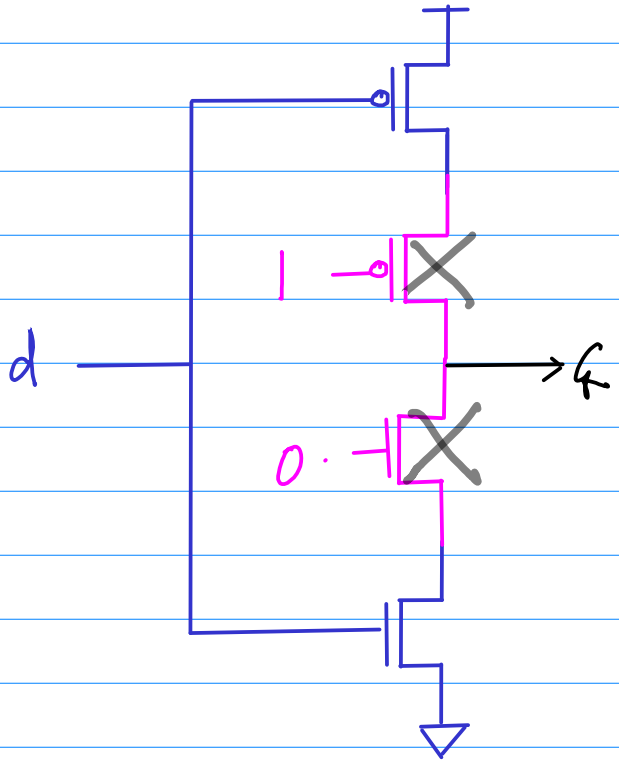
similar to the 3-state buffer

output node cannot be shared with other circuits



$q_f = \overline{d}$

transparent



$q_f = Z$ float

opaque