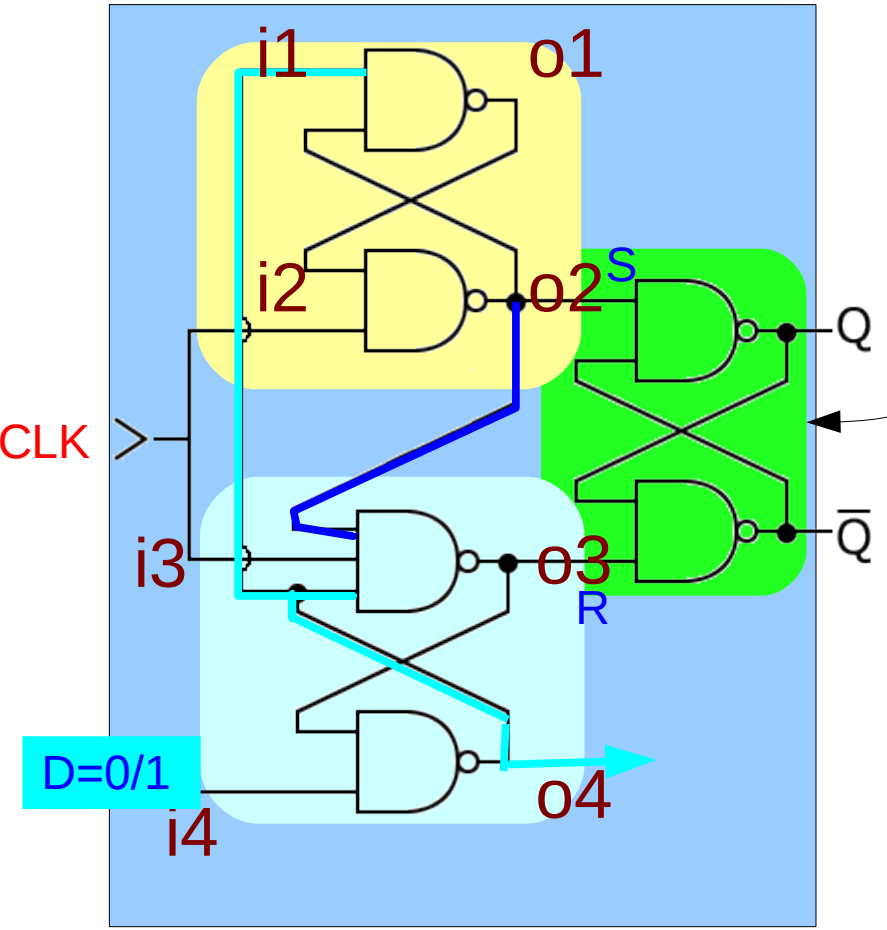
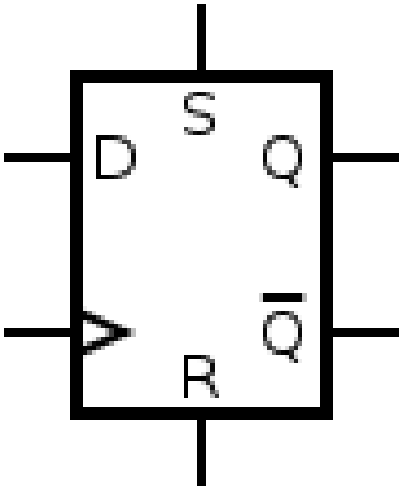
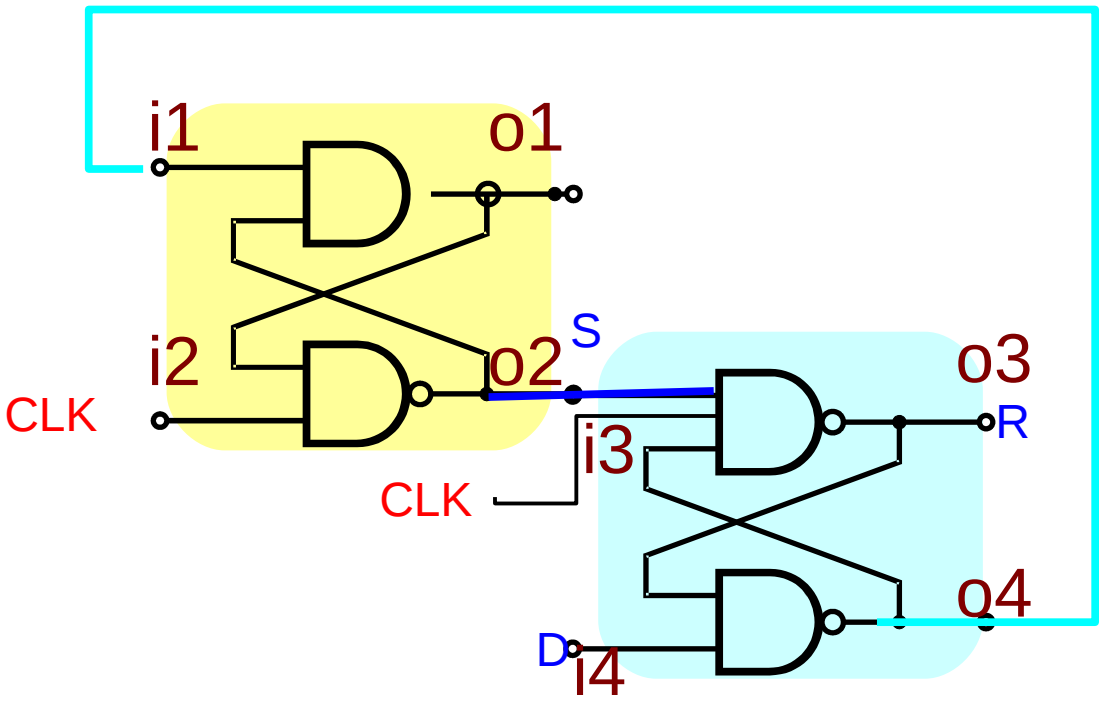
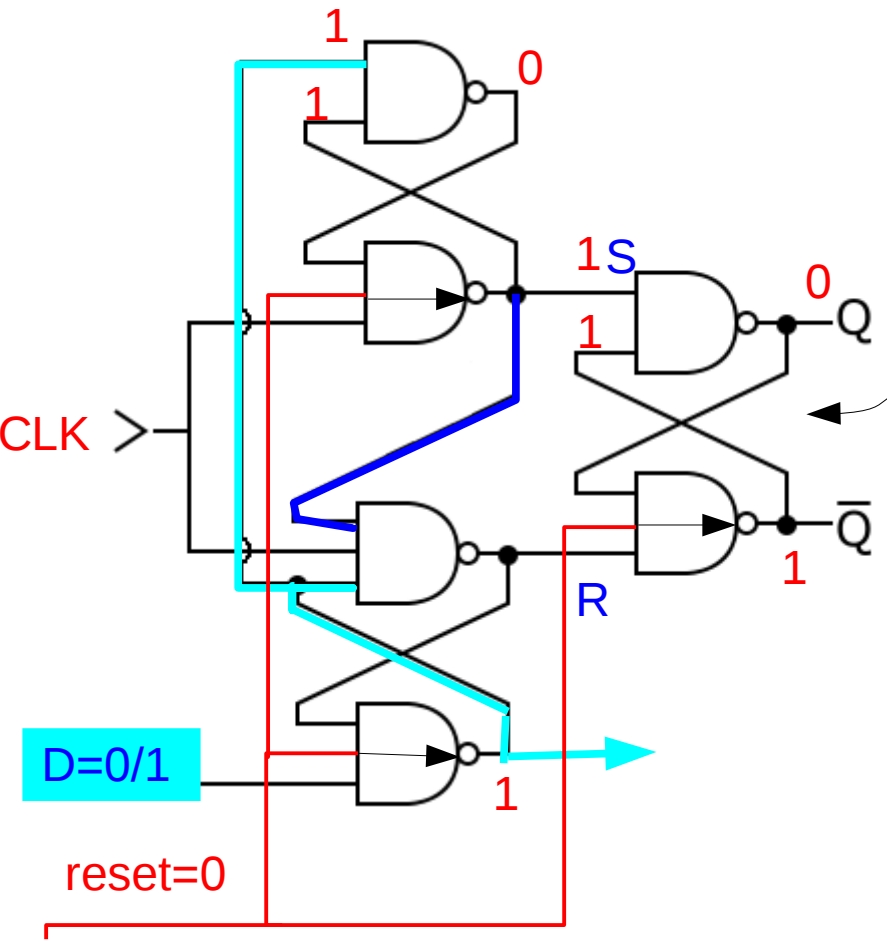


Output Stage Latch

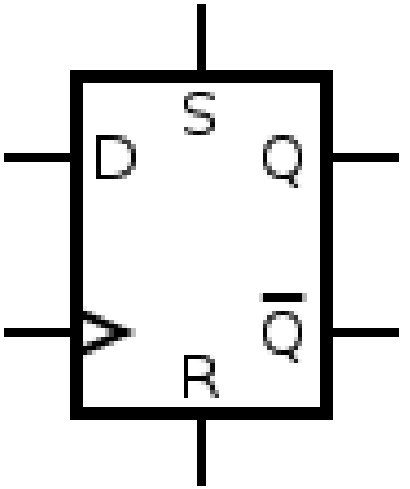


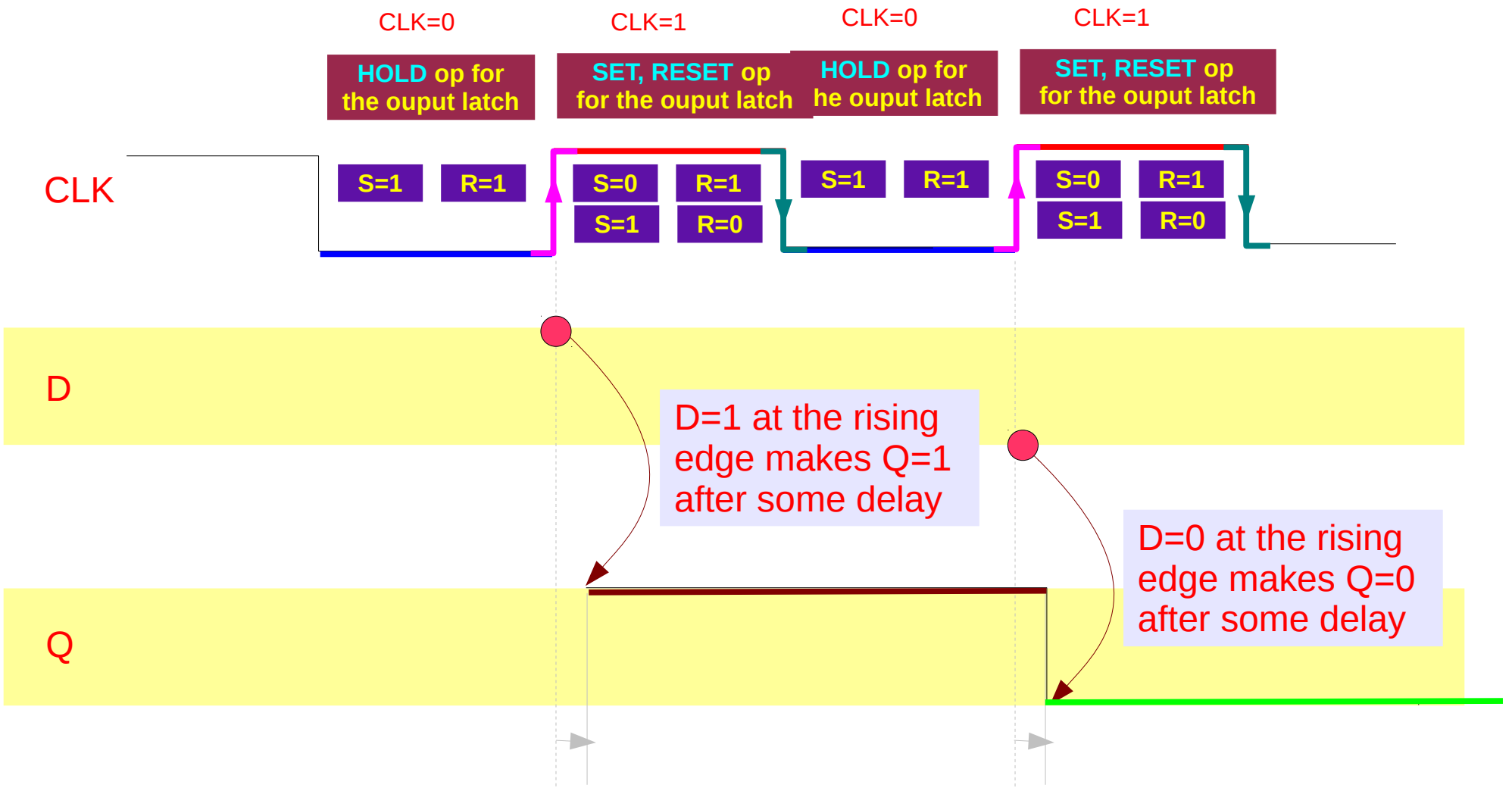
Input Stage Latch

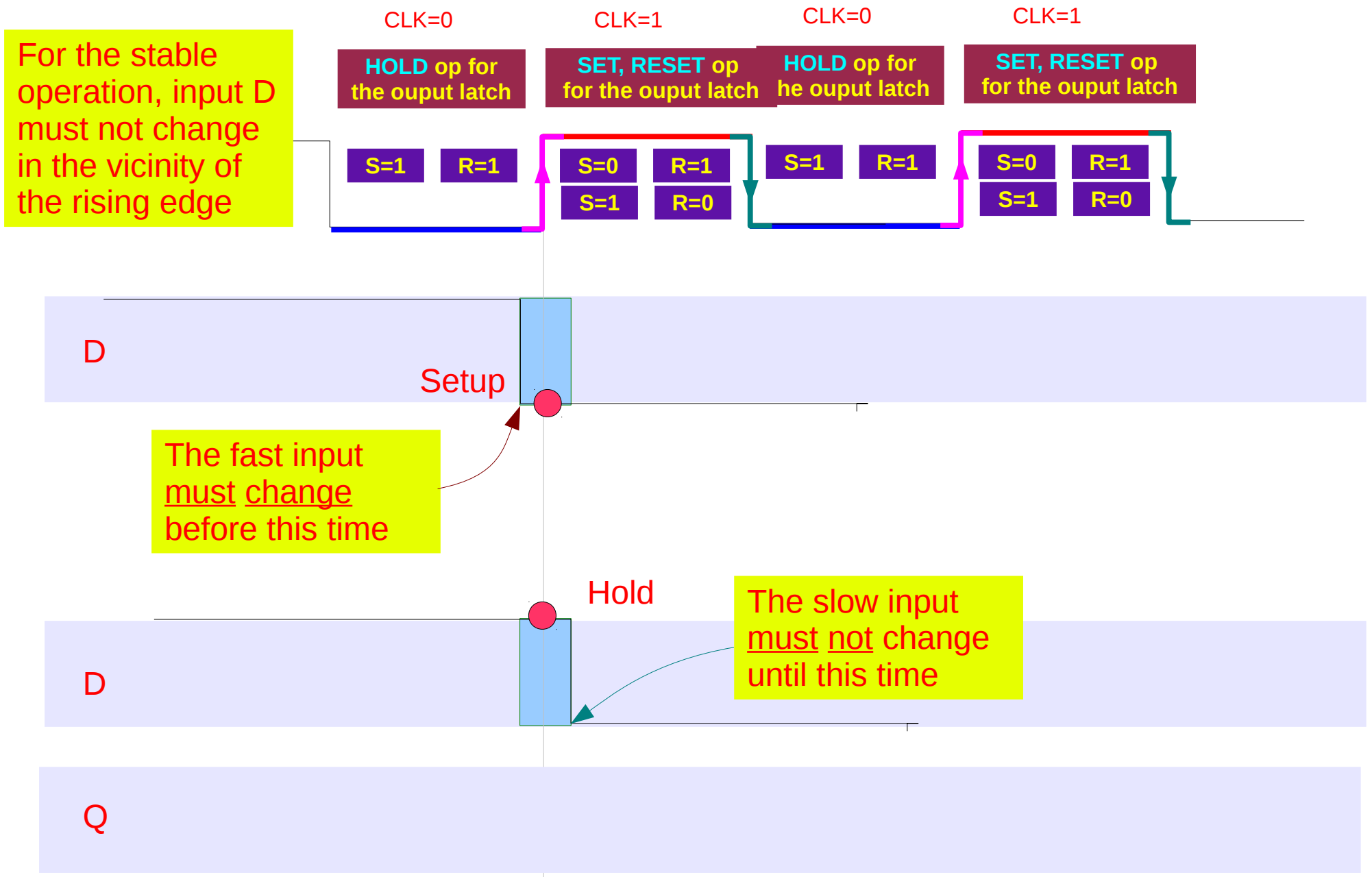


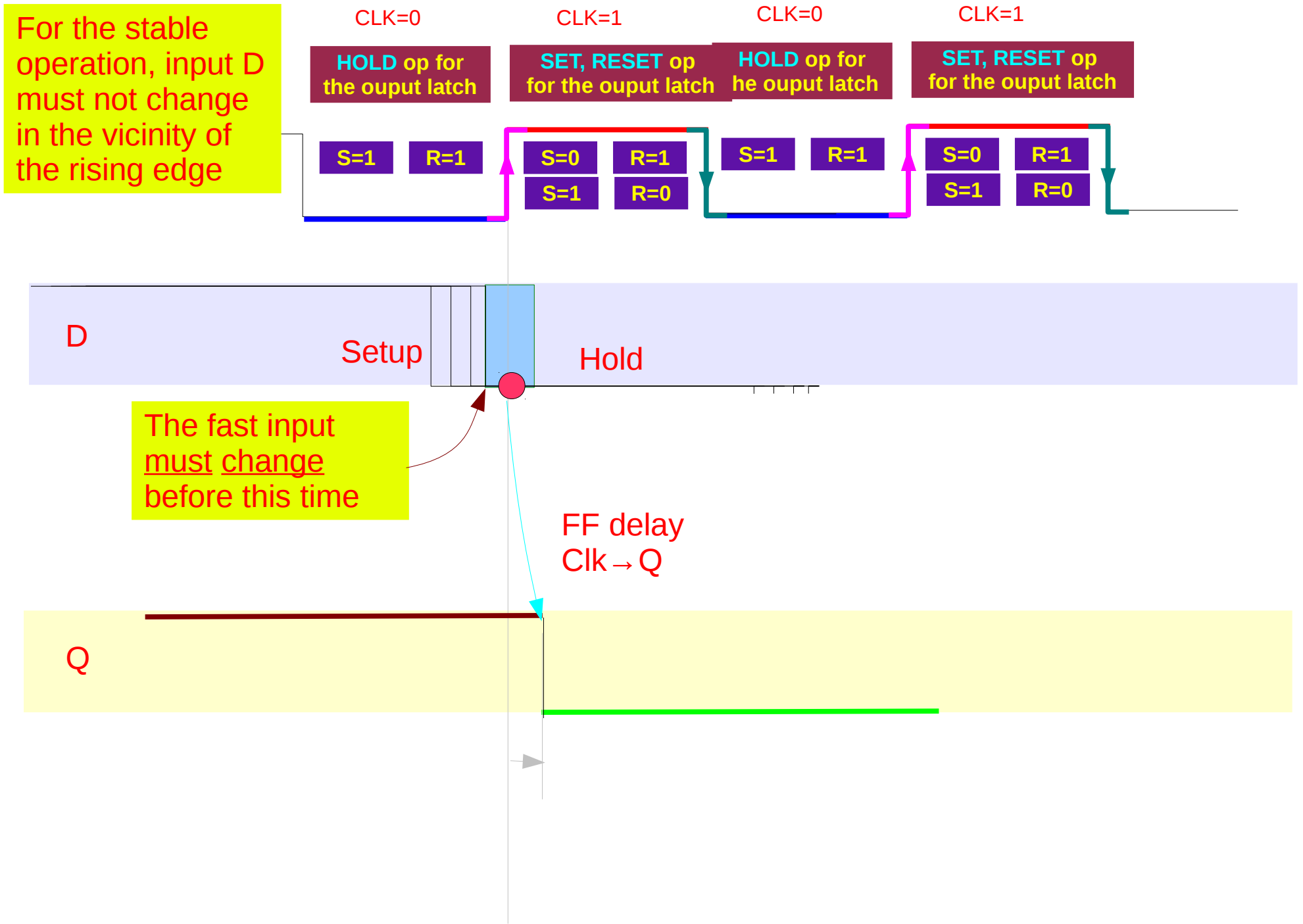


Output Stage Latch

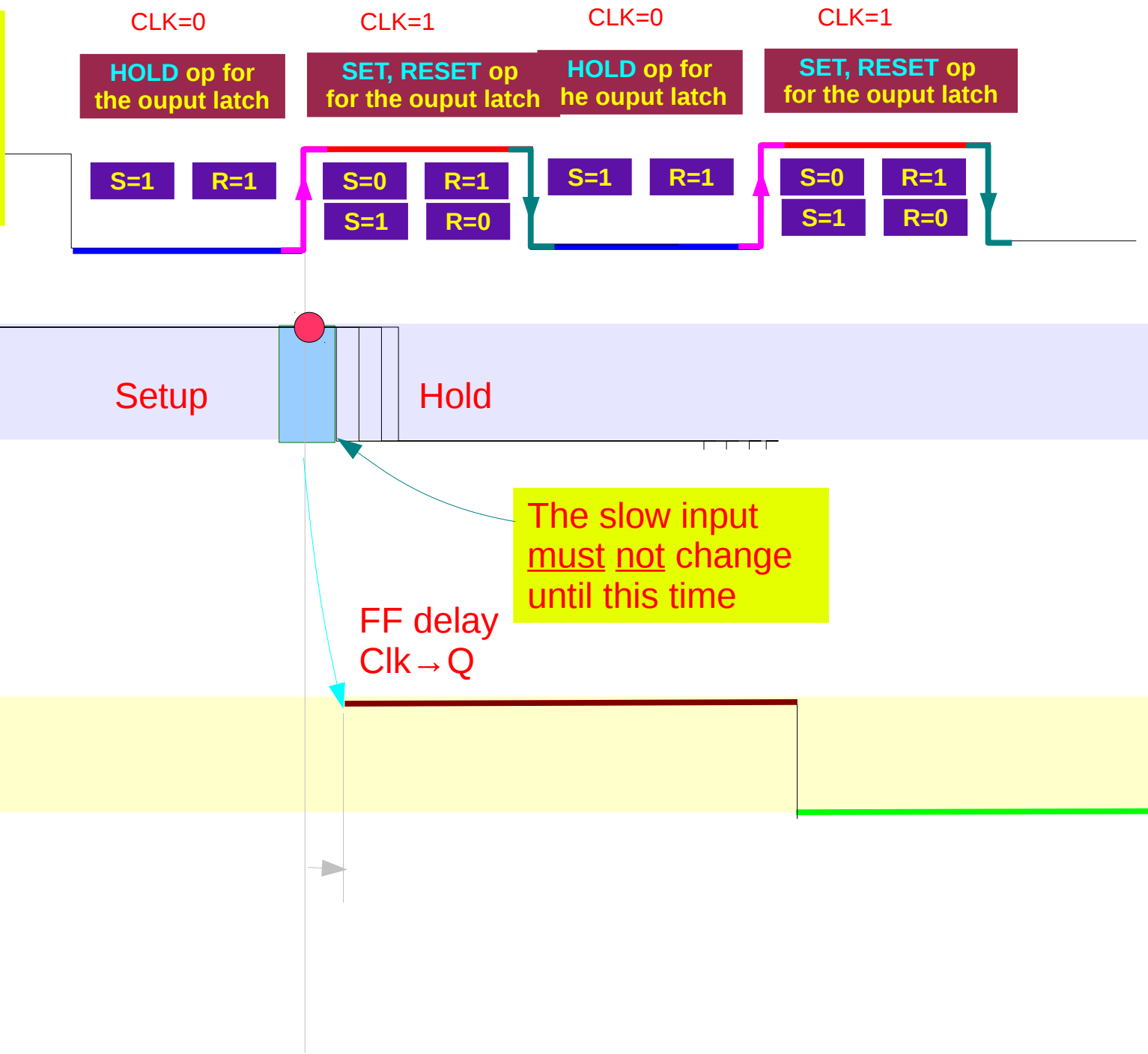



CLK=0
CLK=1
CLK=0
CLK=1
HOLD op for the ouput latch
SET, RESET op for the ouput latch
HOLD op for he ouput latch
SET, RESET op for the ouput latch
CLK
S=1
R=1
S=0
R=1
S=1
R=0
S=1
R=1
S=0
R=1
S=1
R=0
D
D=1 at the rising edge makes Q=1 after some delay
D=0 at the rising edge makes Q=0 after some delay
Q


For the stable operation, input D must not change in the vicinity of the rising edge
CLK=0
CLK=1
CLK=0
CLK=1
HOLD op for the ouput latch
SET, RESET op for the ouput latch
HOLD op for he ouput latch
SET, RESET op for the ouput latch
S=1
R=1
S=0
R=1
S=1
R=0
S=1
R=1
S=0
R=1
S=1
R=0
D
Setup
The fast input must change before this time
Hold
The slow input must not change until this time
D
Q

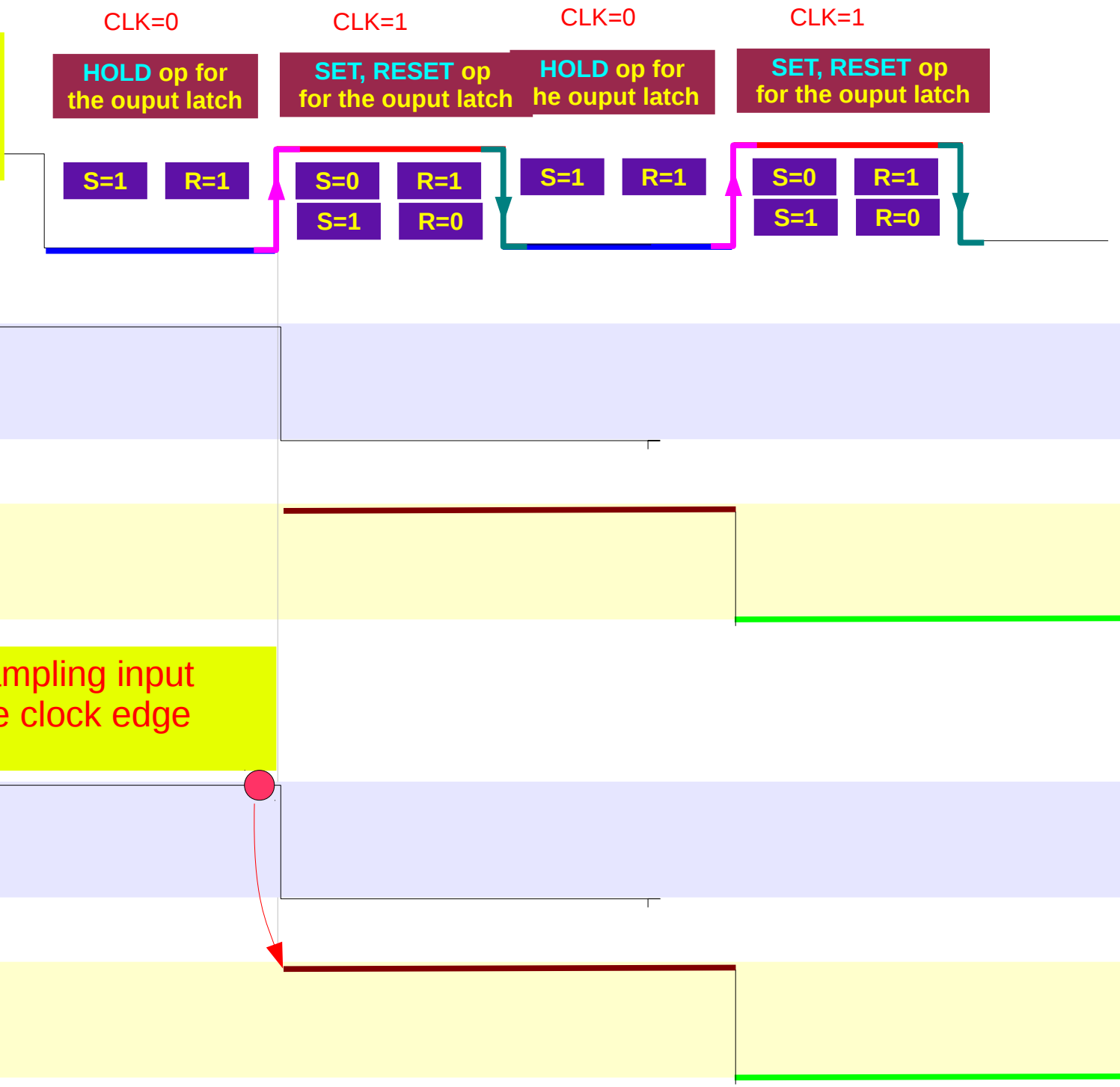

For the stable operation, input D must not change in the vicinity of the rising edge
CLK=0
CLK=1
CLK=0
CLK=1
HOLD op for the ouput latch
SET, RESET op for the ouput latch
HOLD op for he ouput latch
SET, RESET op for the ouput latch
S=1
R=1
S=0
R=1
S=1
R=0
S=1
R=1
S=0
R=1
S=1
R=0
D
Setup
Hold
The fast input must change before this time
FF delay
Clk → Q
Q

For the stable operation, input D must not change in the vicinity of the rising edge



Ideal Case

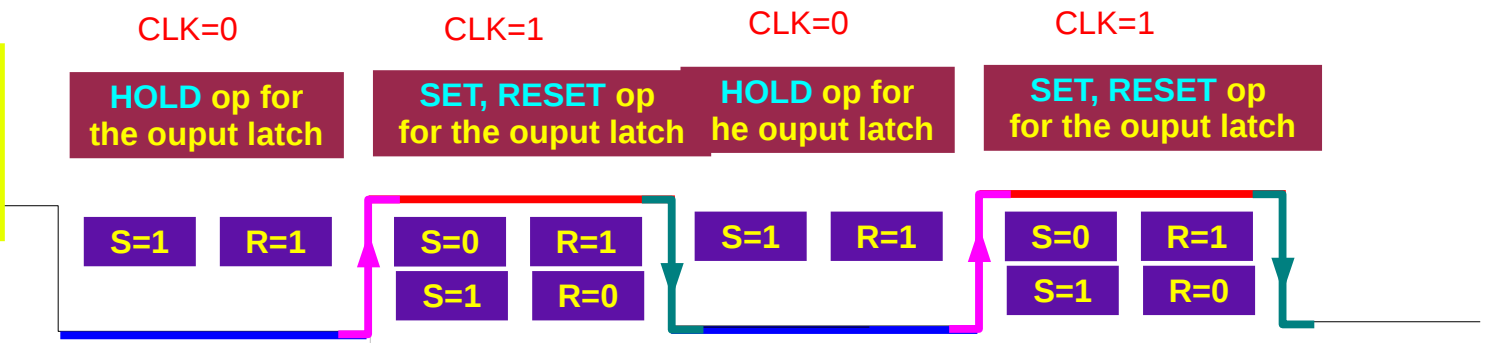
No delay is considered

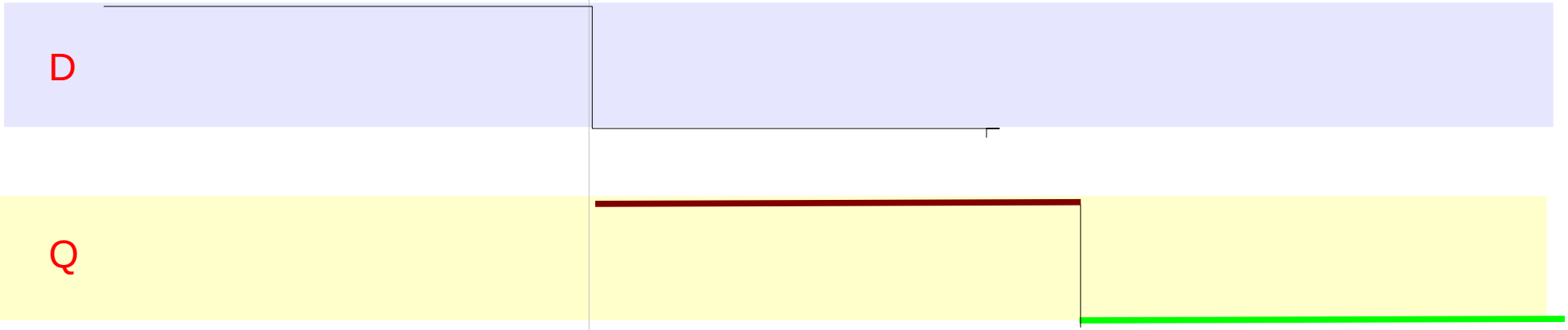


We can view as sampling input data just before the clock edge

Ideal Case

No delay is considered





We can view as sampling input data just before the clock edge

Since this ideal waveform will experience the ff gate delay