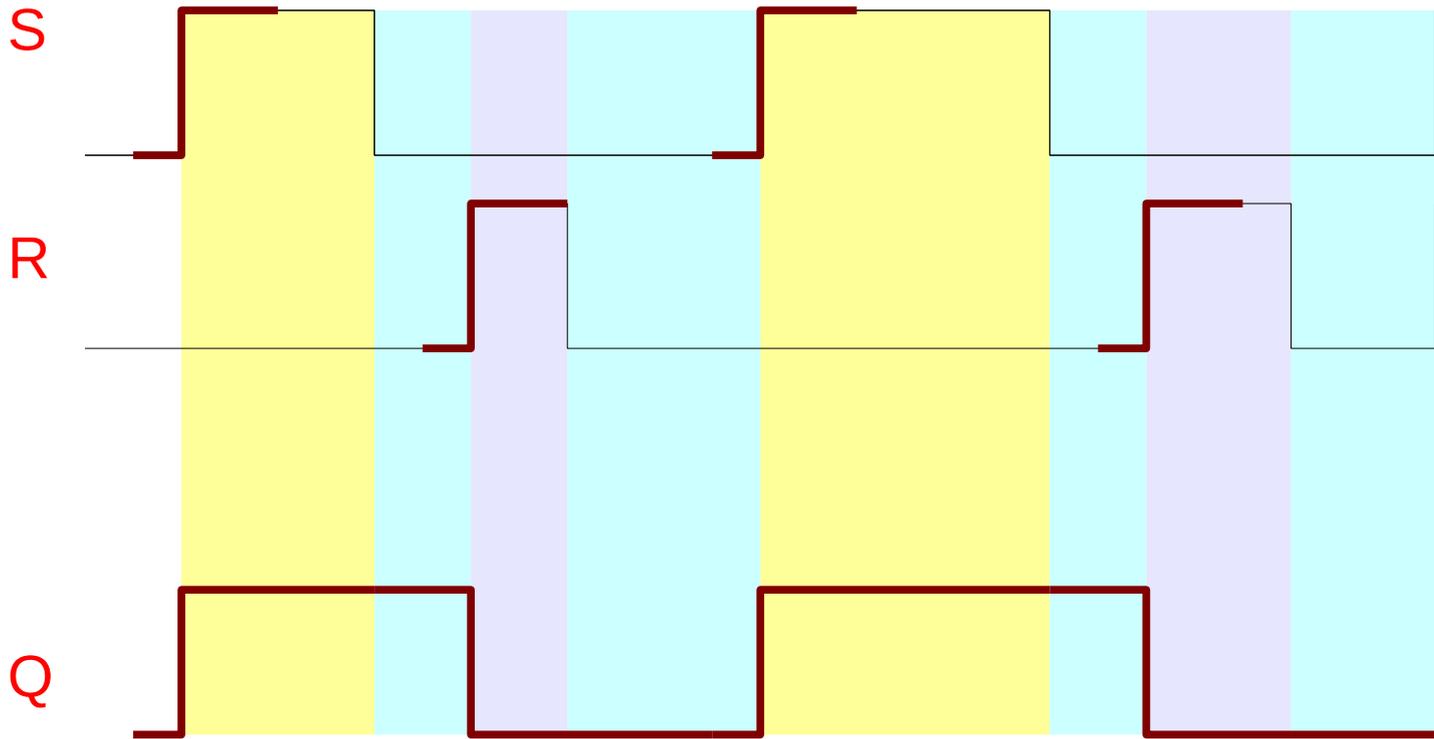


NOR SR Latch



$S = 1$
 $R = 0$

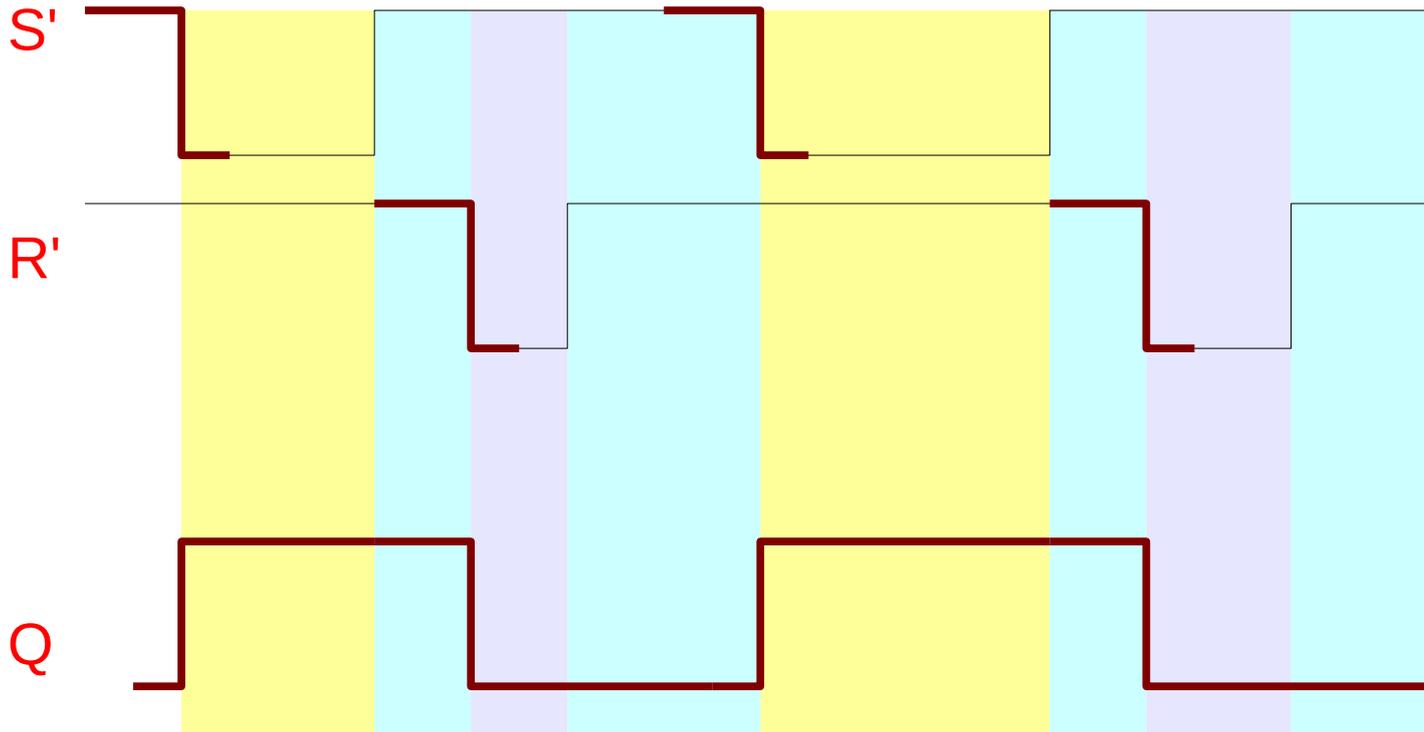
$S = 0$
 $R = 1$

$S = 1$
 $R = 0$

$S = 0$
 $R = 1$

$S = 0$
 $R = 0$

NAND RS Latch



$S' = 0$
 $R' = 1$

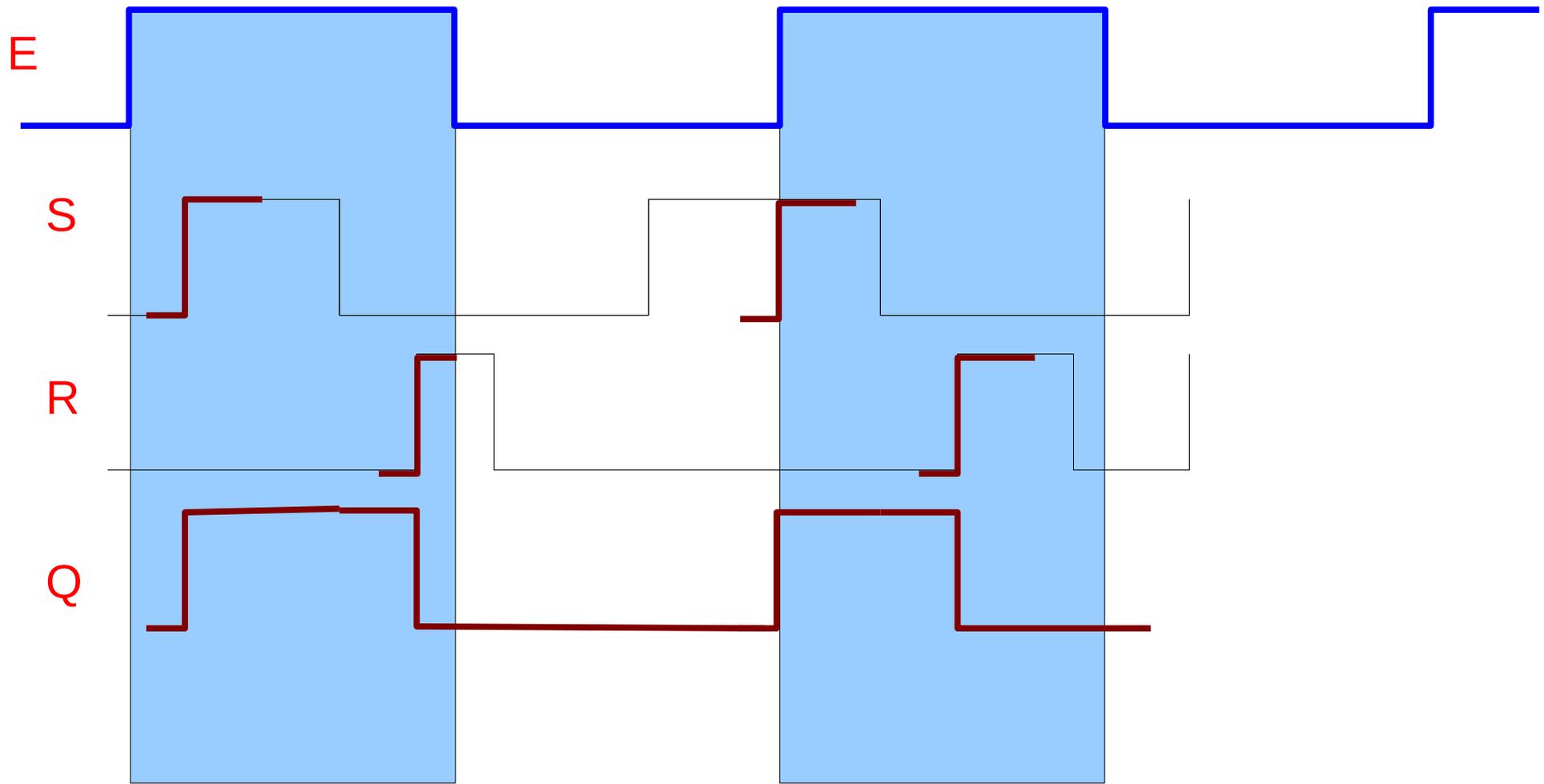
$S' = 1$
 $R' = 0$

$S' = 0$
 $R' = 1$

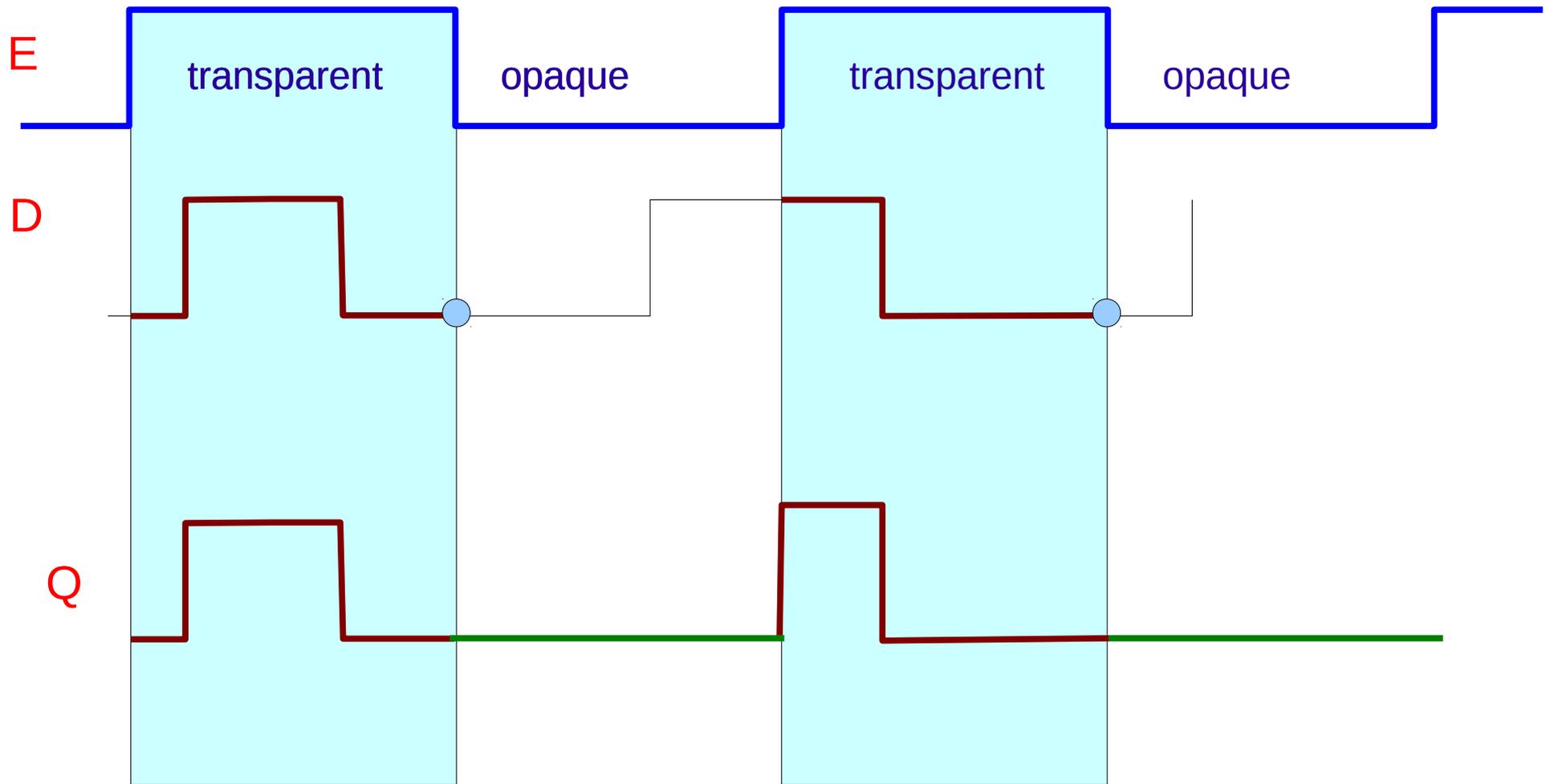
$S' = 1$
 $R' = 0$

$S' = 1$
 $R' = 1$

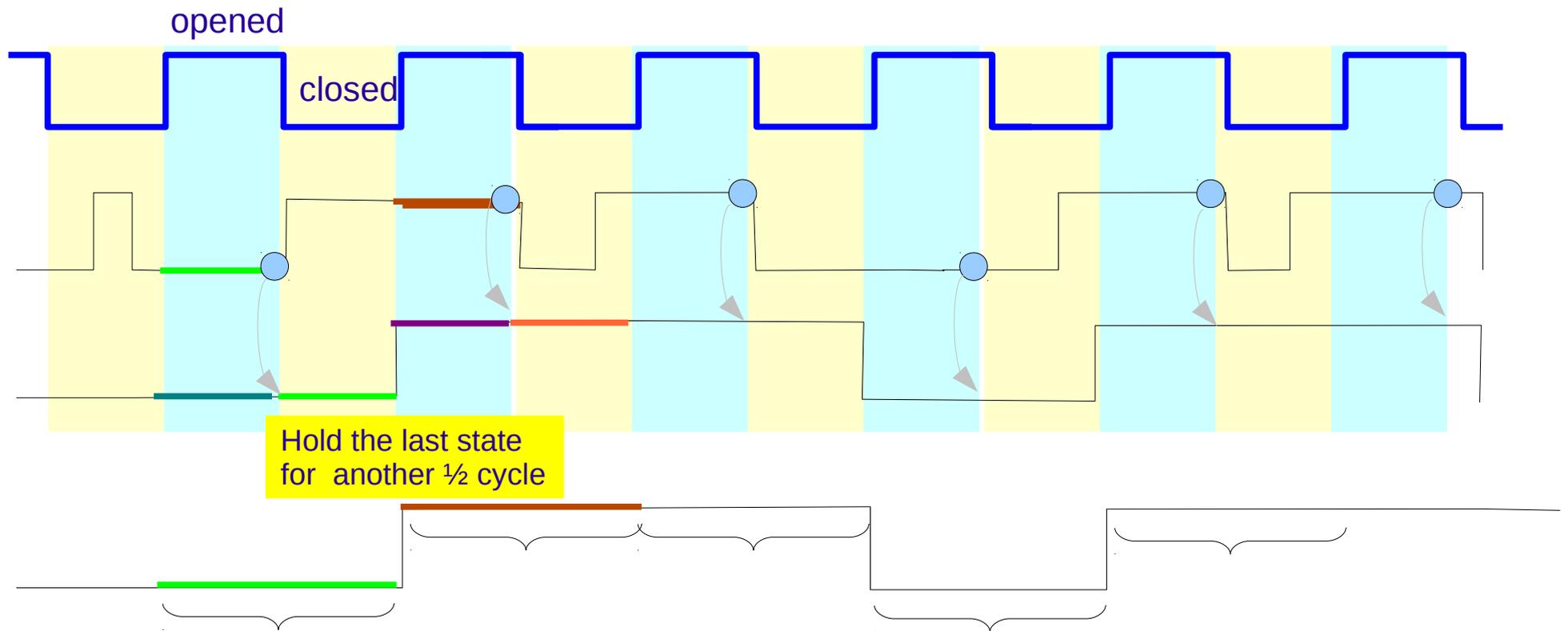
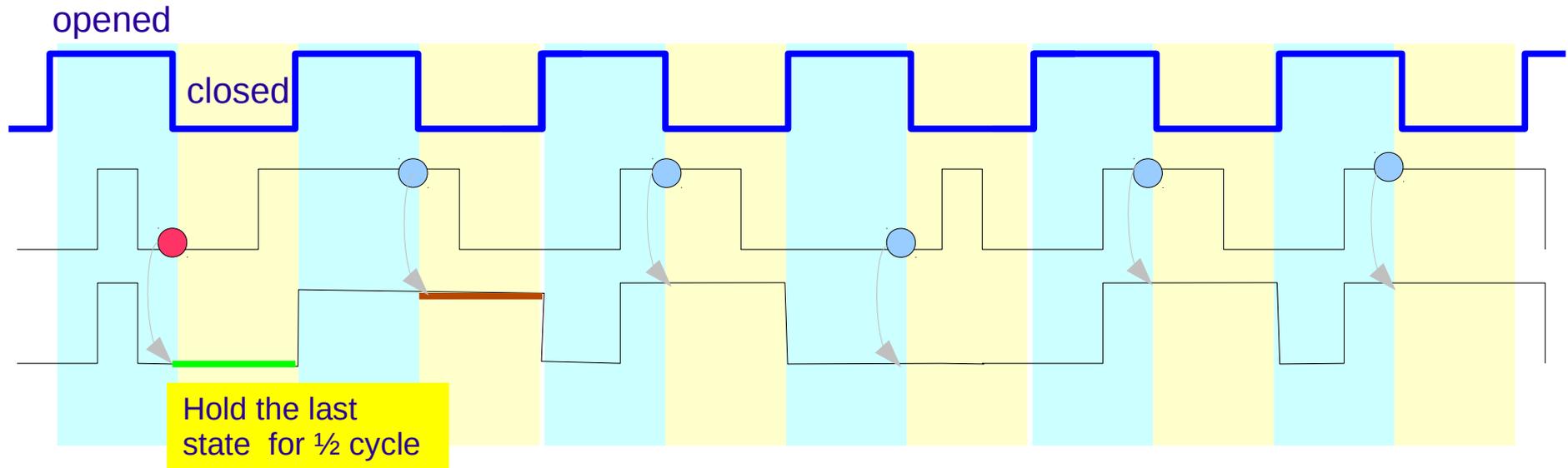
Clocked NOR RS Latch



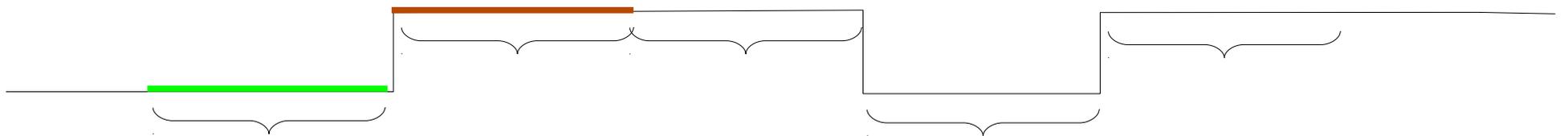
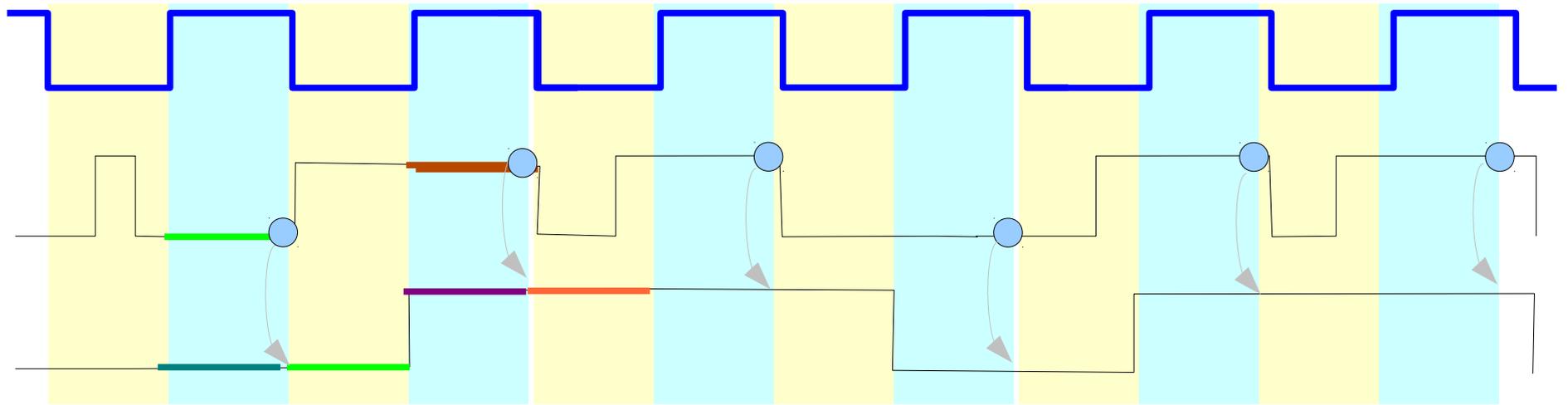
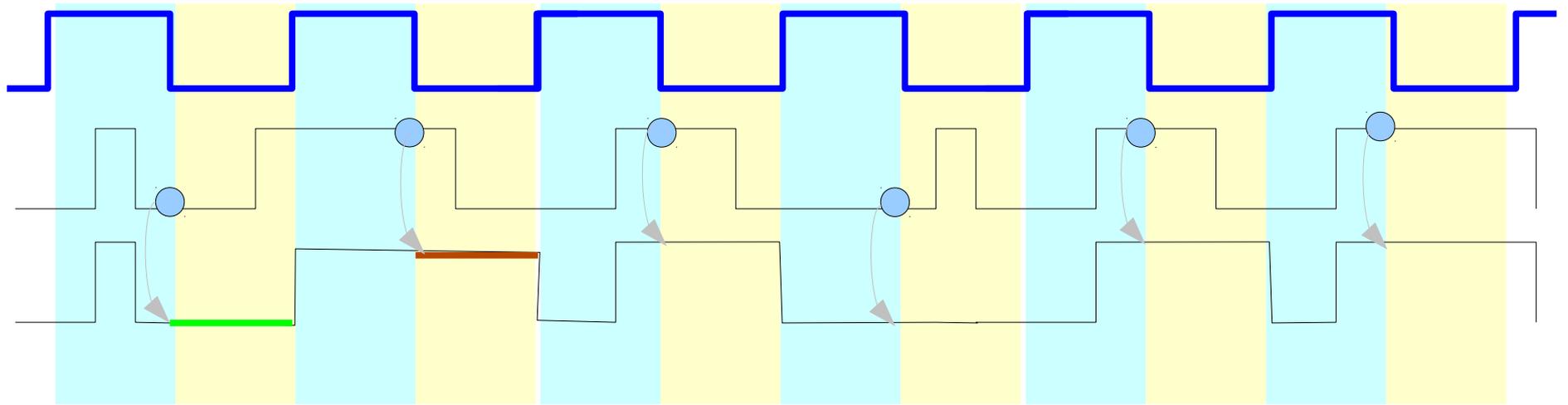
Gated D Latch



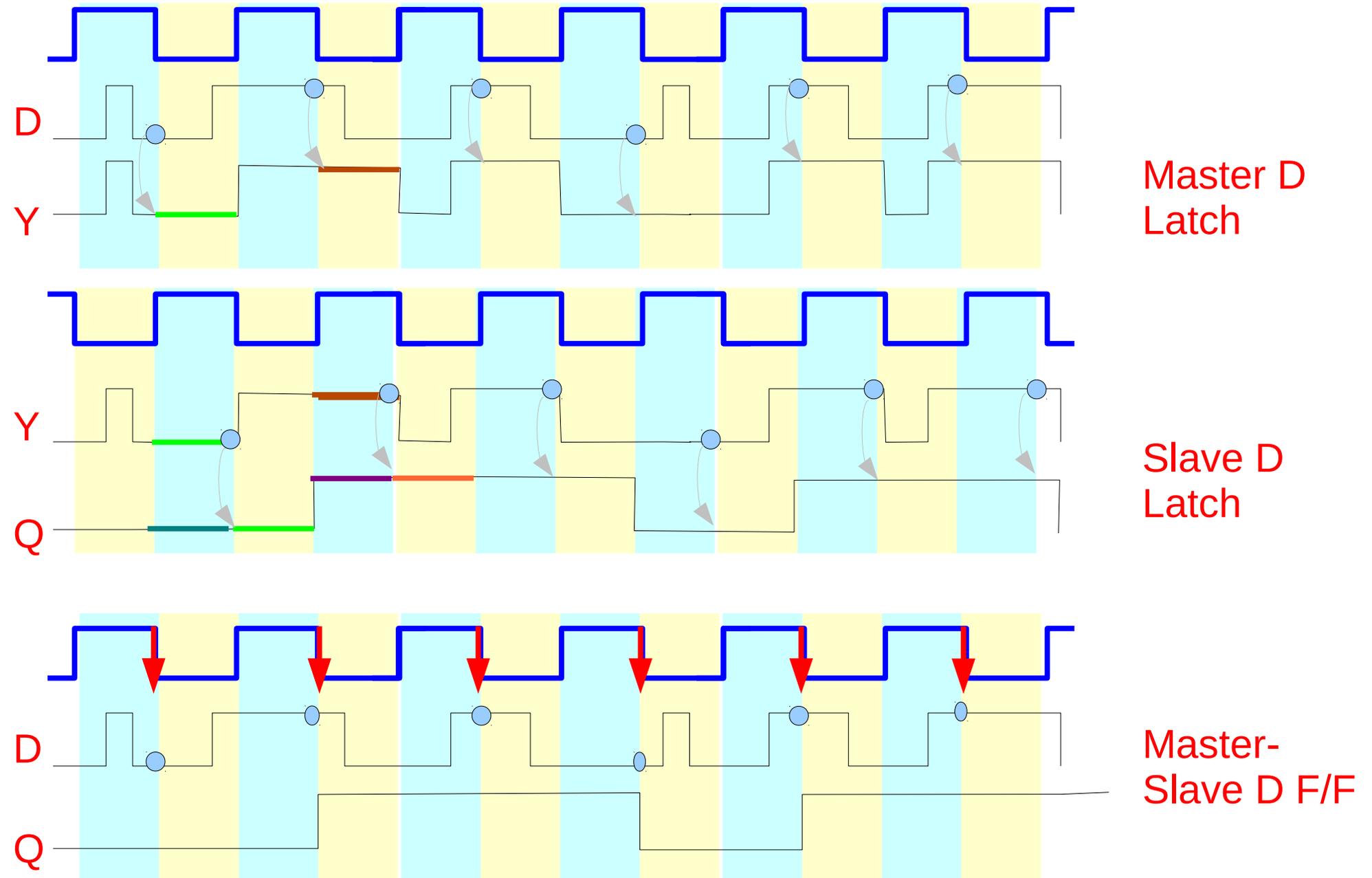
Master Slave D Flip Flop

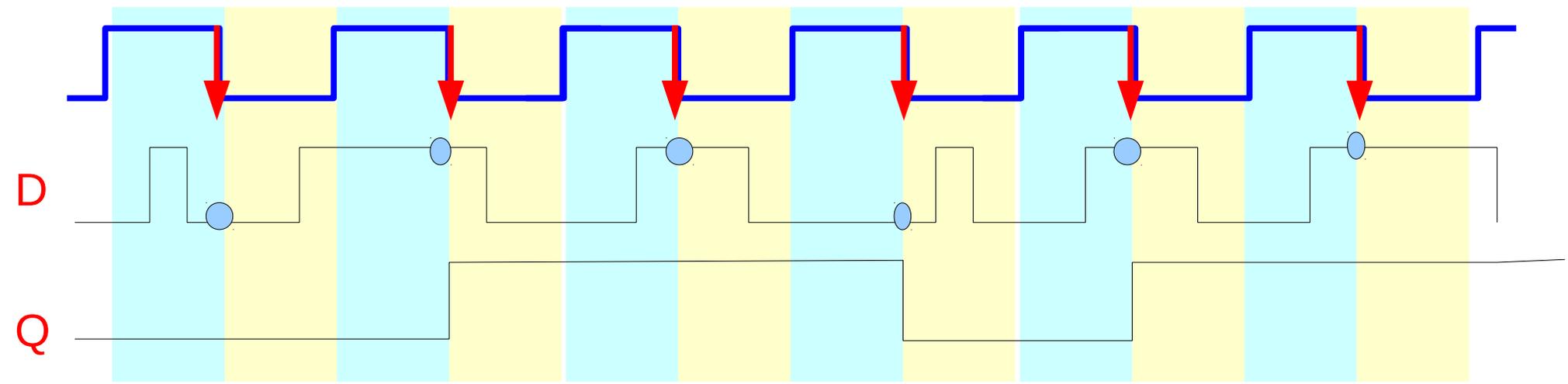


Master Slave D Flip Flop



Master Slave D Flip Flop





Y

Q