# CMOS Delay-5 (H.5)
# Inverter Chain

20161202

# References

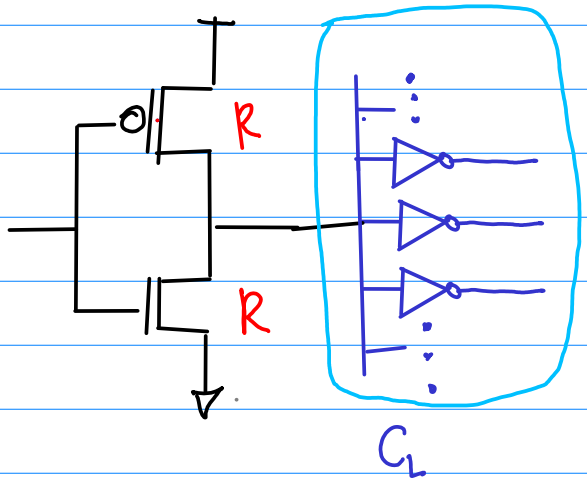
Some Figures from the following sites

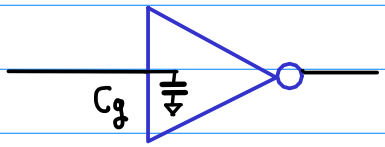
[1] http://pages.hmc.edu/harris/cmosvlsi/4e/index.html
Weste & Harris Book Site

[2] en.wikipedia.org

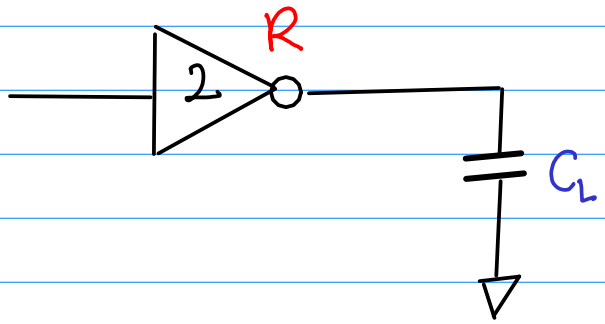
[3] http://www.ee.ic.ac.uk/pcheung/teaching/ee4_asic/notes/Topic%20

# Driving Large Capacitive Loads




$$t \propto R C_L$$




how to minimize $t \propto R C_L$

# Transconductance $\beta \longrightarrow R$

$\beta$ : Device **Transconductance** Parameter

$k$ : Process **Transconductance** Parameter

$\mu$ : Electron / Hole Mobility

pMOS $\beta_p = k_p \left(\frac{W}{L}\right)_p$ $k_p = \mu_p C_{ox}$ $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

nMOS $\beta_n = k_n \left(\frac{W}{L}\right)_n$ $k_n = \mu_n C_{ox}$ $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

pMOS $\beta_p = \boxed{\mu_p C_{ox}} \left(\frac{W}{L}\right)_p = \boxed{k_p} \left(\frac{W}{L}\right)_p$

nMOS $\beta_n = \boxed{\mu_n C_{ox}} \left(\frac{W}{L}\right)_n = \boxed{k_n} \left(\frac{W}{L}\right)_n$

Saturation Current

$I_{dp} = \frac{\beta_p}{2} (V_{GSn} - |V_{Tp}|)^2$ $V_{Tp} < 0$

$I_{dn} = \frac{\beta_n}{2} (V_{GSn} - V_{Tn})^2$ $V_{Tn} > 0$

# Transconductance Ratio

$$\frac{\beta_n}{\beta_p} = \frac{k_n \left(\frac{W}{L}\right)_n}{k_p \left(\frac{W}{L}\right)_p}$$

$$\beta \propto \frac{1}{k} \qquad \beta \propto \left(\frac{W}{L}\right) \qquad \beta \propto k.$$

a unit nMOS
a unit pMOS

$$\frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p} = 1$$

$$\frac{\beta_n}{\beta_p} = \frac{k_n \left(\frac{W}{L}\right)_n}{k_p \left(\frac{W}{L}\right)_p} = \frac{k_n}{k_p} = r = 2 \sim 3$$

$$\boxed{\frac{k_n}{k_p} = 2 \sim 3}$$ different mobility

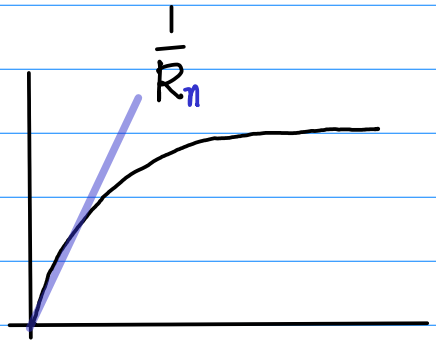
physical property

# R during transient switching

$$\frac{\beta_n}{\beta_p} = \frac{k_n \left(\frac{W}{L}\right)_n}{k_p \left(\frac{W}{L}\right)_p} \qquad \frac{k'_n}{k'_p} = \frac{\mu_n}{\mu_p} = r = 2 \sim 3$$

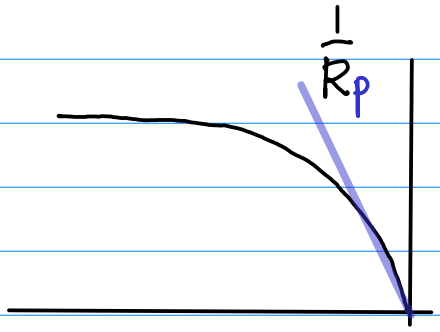
fall time $t_f$

$$R_n = \frac{1}{\beta_n (V_{DD} - V_{Tn})}$$

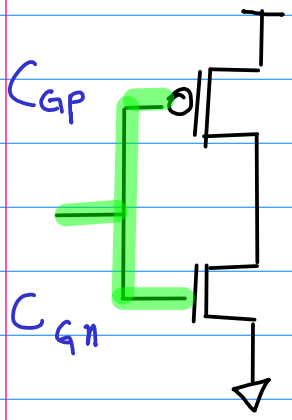


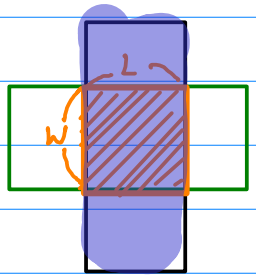

rise time $t_r$

$$R_p = \frac{1}{\beta_p (V_{DD} - V_{Tp})}$$

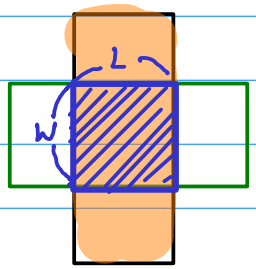


# Input Capacitance




a unit pMOS
with minimum size
min W & min L




a unit nMOS
· with minimum size
· min W & min L

$$C_{in} = C_{Gn} + C_{GP}$$
$$= C_{ox}(A_{Gn} + A_{GP})$$
$$= C_{ox}(LW_n + LW_p)$$

$A_G$: gate area

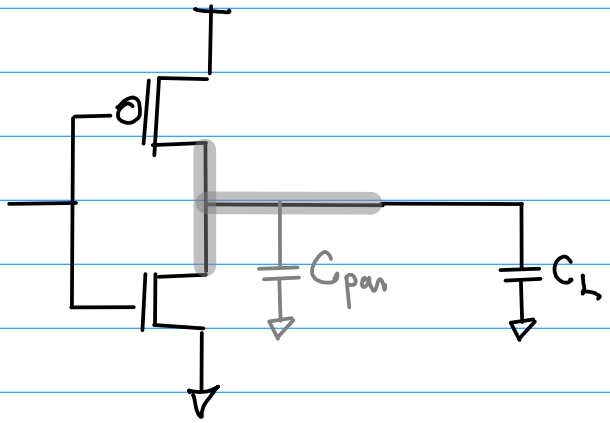
the channel length L assumed

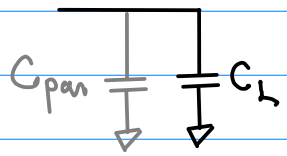
$$C_{in} = C_{ox} L (W_n + W_p)$$
$$= C_{ox} L (W_n + r W_n)$$
$$= C_{ox} L W_n (1 + r)$$
$$= C_{Gn} (1 + r)$$

# Output Capacitance

$$C_{out} = C_{par} + C_L$$

↑ drain parasitic cap.



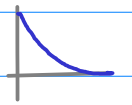




$C_{out} = C_{par} + C_L$

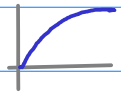
Parasitic Capacitance

# Time Constants

$$\begin{cases} V_{out}(t) = V_{DD}\left(1 - e^{-t/\tau}\right) \\ V_{out}(t) = V_{DD}\, e^{-t/\tau} \end{cases}$$



$t_f$



$t_r$

$$\tau = RC_{out} = R(C_{par} + C_L)$$

## Generic Switching Delay

$$t_s = t_0 + \alpha C_L \Rightarrow t_s = t_r = t_f$$

↑

When $C_L = 0$ Zero Load

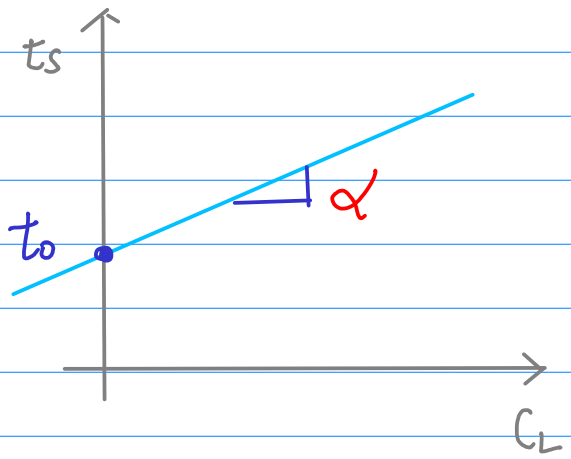
non zero $C_{par}$

Panasitic Capacitance

# Generic Switching Delay, $\alpha$ slope

## Generic Switching Delay

$$t_s = t_0 + \alpha C_L$$



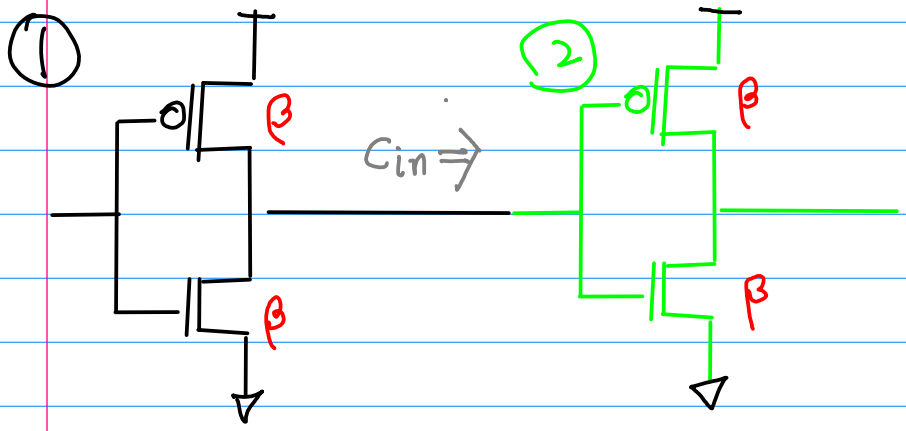

$t_0$ : zero load delay

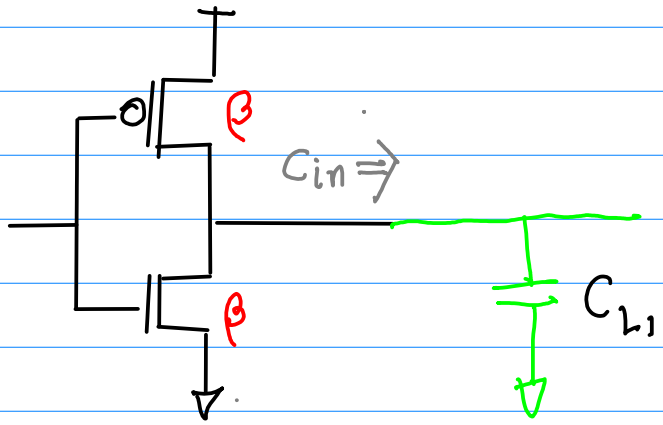
$\alpha$ : slope

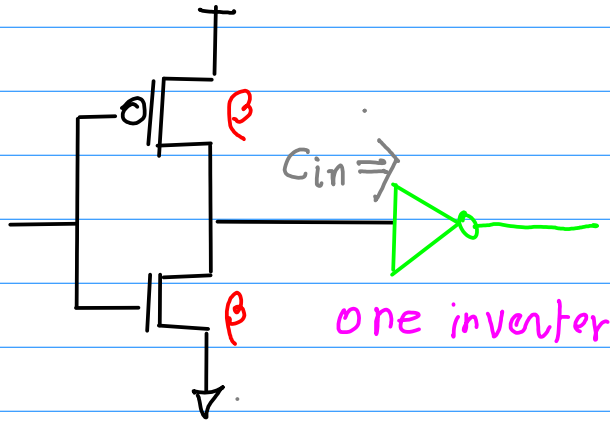
$t \approx RC$

$\alpha \propto \frac{1}{\beta(V_{DD} - V_T)}$

$C_L$



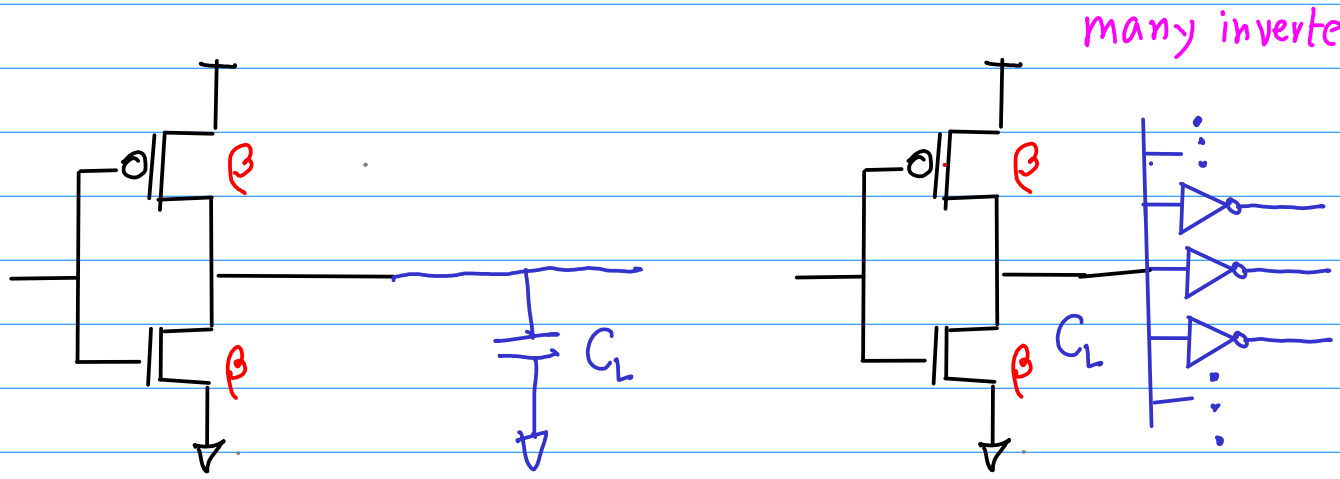

reference case $\boxed{C_{L1} = C_{in}}$

Generic Switching Delay of (1)

$$t_{s1} = t_0 + \alpha C_{L1}$$

$$= t_0 + \alpha C_{in}$$

When $C_L \gg C_{in}$




to minimize $t_s$ (generic switching delay)

$\alpha \downarrow \Rightarrow R \downarrow \Rightarrow \beta \uparrow \Rightarrow$ bigger size

speed v.s. area tradeoff

$t_s = t_0 + \alpha C_L \qquad t \approx RC$

$\alpha \propto \frac{1}{\beta (V_{DD} - V_T)}$

$C_L$

to minimize $t_s$

$\alpha \downarrow \Rightarrow R \downarrow \Rightarrow \beta \uparrow \Rightarrow$ bigger size

speed v.s. area tradeoff

Scaling Factor $S$

$$t_s = t_0 + \frac{\alpha}{S} C_L$$

(R, C)

$$\beta' = S\beta$$

$$R' = \frac{R}{S}$$

$$\alpha' = \frac{\alpha}{S}$$

Compensation Factor $\frac{1}{S}$

enables an inverter to drive larger values of $C_L$

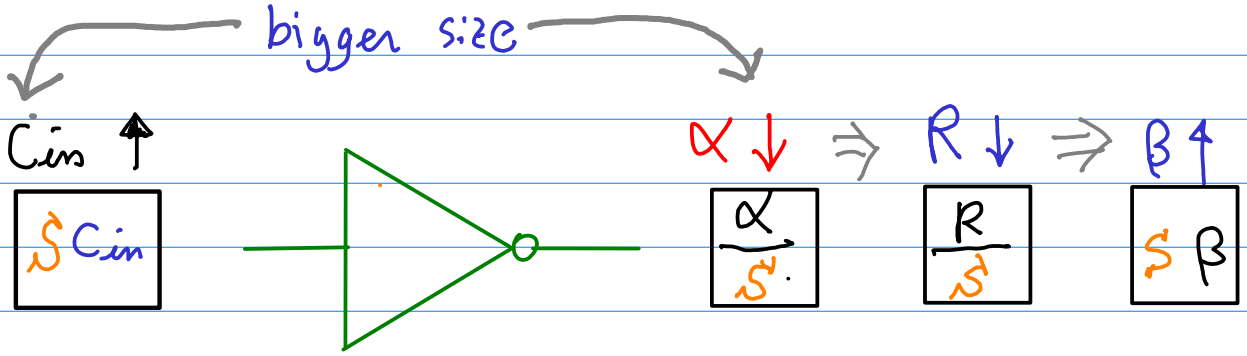
If $C_L = S\, C_{in}$ (increased by the scaling factor $S$)

then the switching time is the same

# Bigger Inverter

to minimize $t_s$ (generic switching Delay)

$$t_s = t_0 + \alpha C_L \Rightarrow t_0 + \frac{\alpha}{S} C_L$$

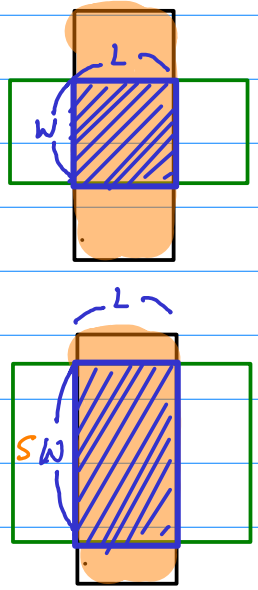



Scaling Factor $S$

$$W_n' = S\, W_n$$

$$C_{in}' = S\, C_{in}$$

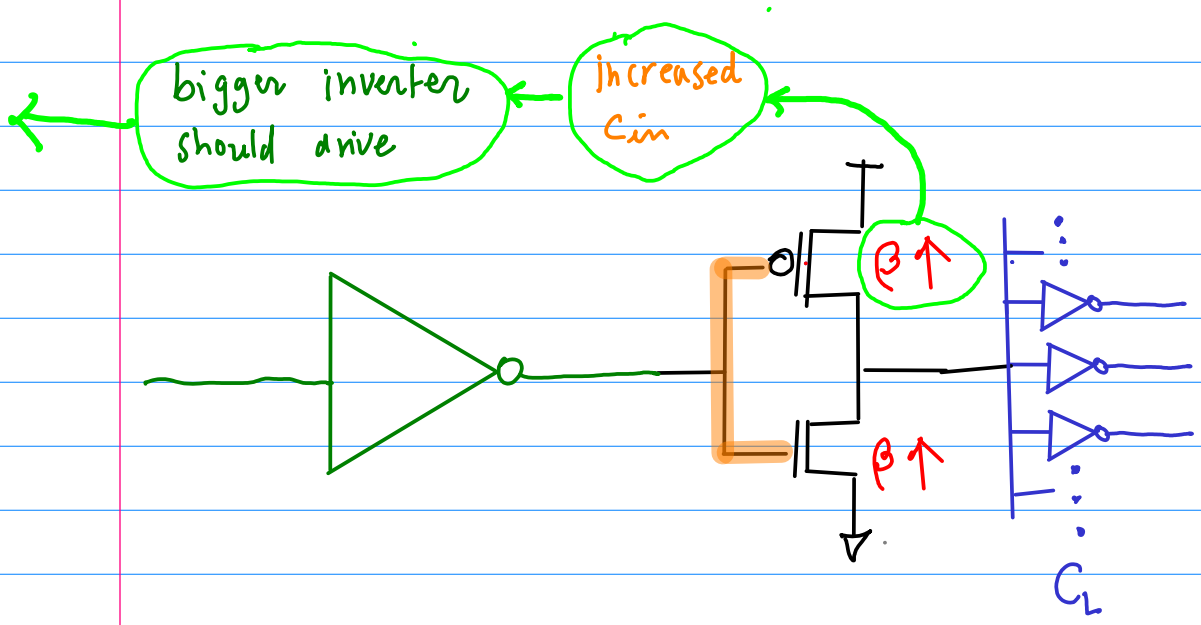
Cause problems to the drivers.

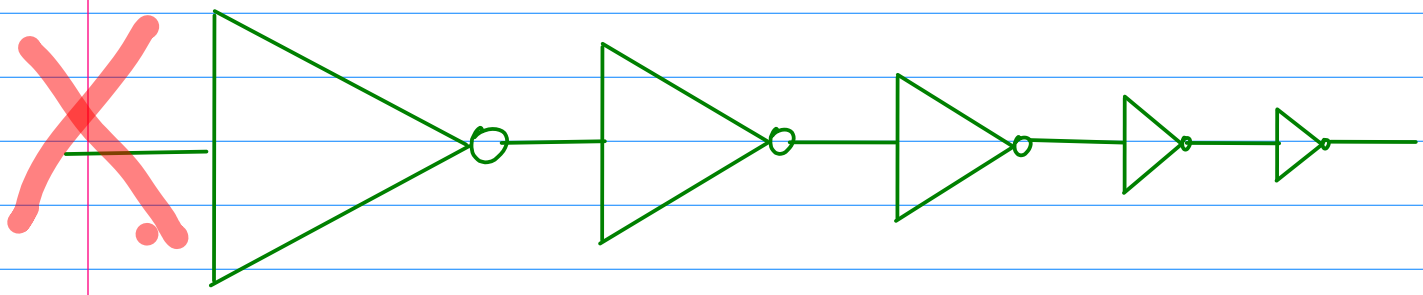



$$\beta' = S\,\beta$$

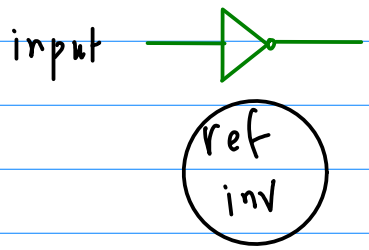
$$R' = \frac{R}{S}$$

$$\alpha' = \frac{\alpha}{S}$$

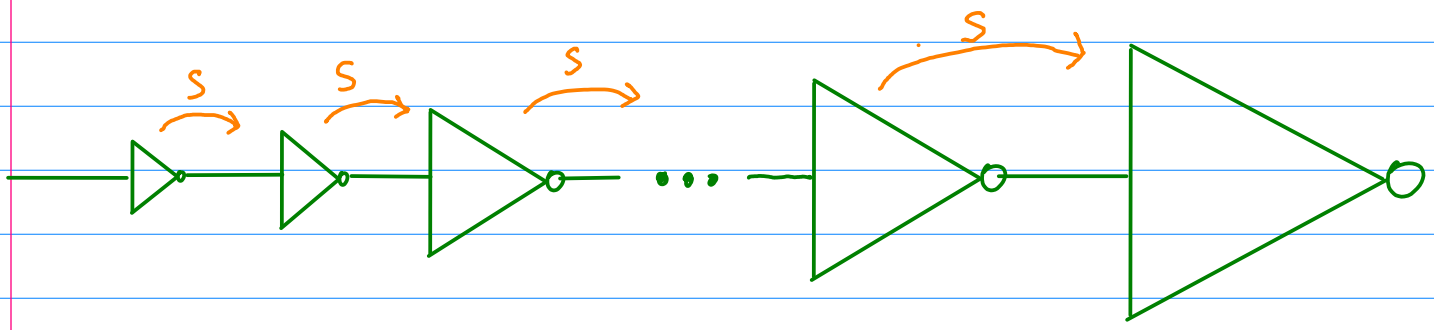


it is natural to assume the first driving gate must be comparable to the reference gate



think G.P. (Geometric Progression)
in size factors




* Arithmetic Progression // Geometric Progression

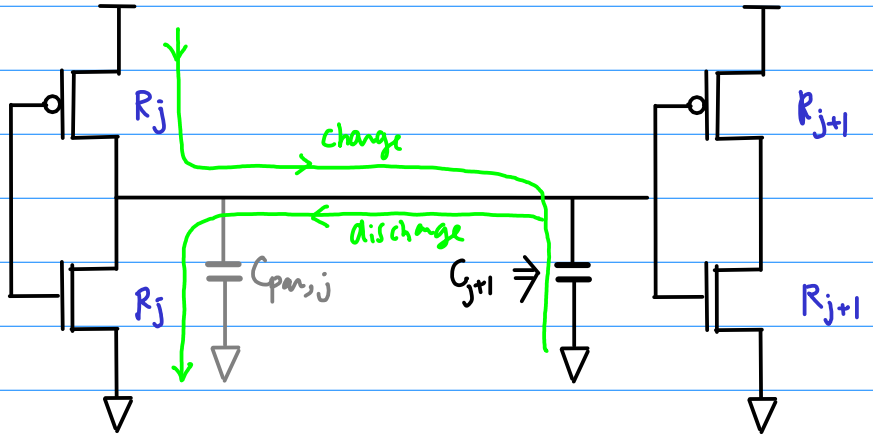
Σ path delay

↓

min delay.

when all equal path delay

# Case I: Ignore Parasitic Capacitance




$C_{par,j} \ll C_{j+1}$

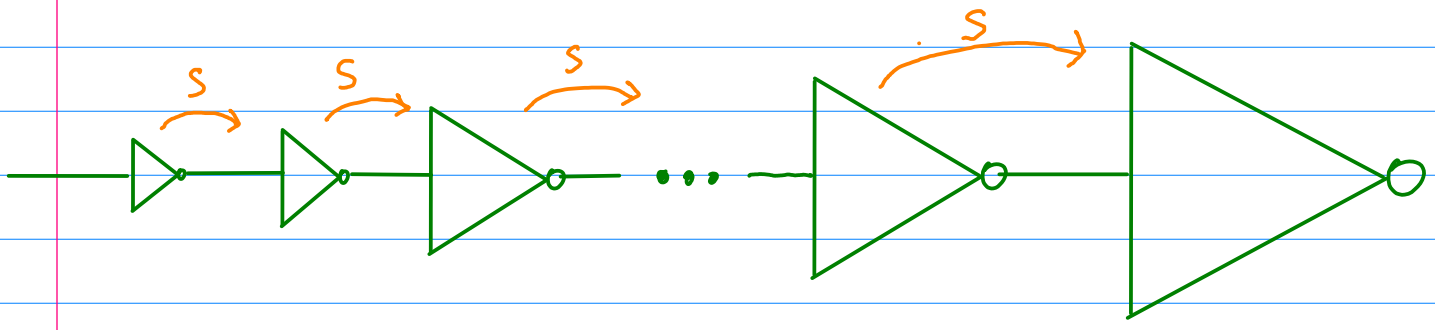
$\tau_j = R_j C_{j+1}$

Using $d_i = g_i h_i$

$(p_i = 0)$

# Delay Minimization in an inverter cascade

* increasing size




$$\beta_1 < \beta_2 < \beta_3 < \cdots < \beta_{N-1} < \beta_N$$

$$\beta_2 = S\beta_1$$
$$\beta_3 = S\beta_2 = S^2\beta_1$$
$$\beta_4 = S\beta_3 = S^3\beta_1$$

Geometric progress

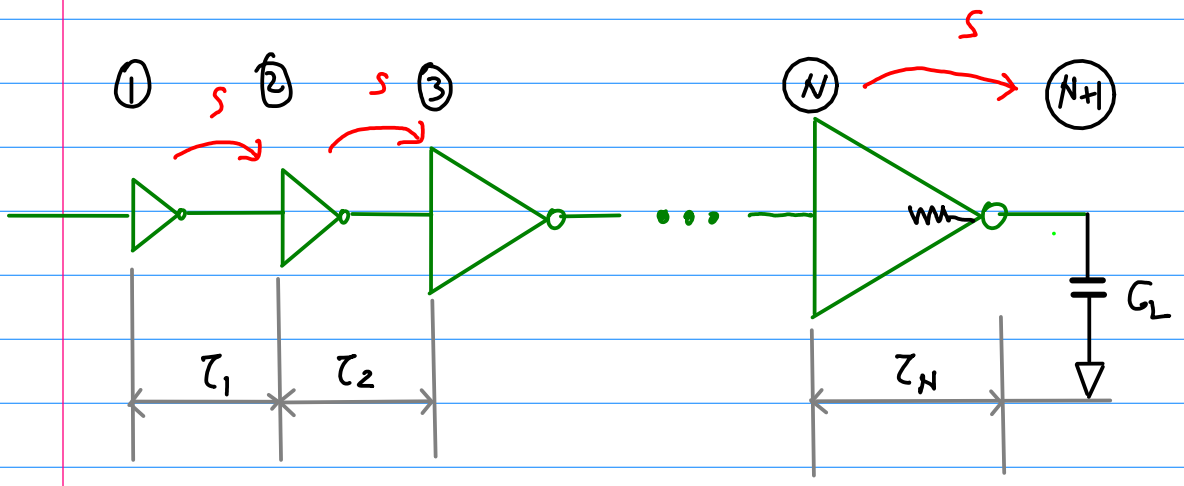
$$\beta_j = S\beta_{j-1} = S^{j-1}\beta_1$$

$$\boxed{\beta_j = S^{j-1}\beta_1}$$

$$C_j = S^{j-1}C_1$$
$$R_j = \frac{R_1}{S^{j-1}}$$

common ratio = $S \rightarrow e$ for min delay

S : size factor




N-stage inverter chain $\quad \boxed{\tau_j = R_j C_{j+1}}$

$$\tau_d = \tau_1 + \tau_2 + \cdots + \tau_N$$

$$= R_1 C_2 + R_2 C_3 + \cdots + R_N C_L \qquad (C_{N+1} = C_L)$$

$$= \left(R_1\right)\left(S C_1\right) + \left(\frac{R_1}{S}\right)\left(S^2 C_1\right) + \left(\frac{R_1}{S^2}\right)\left(S^3 C_1\right) + \cdots + \left(\frac{R_1}{S^{N-1}}\right)\left(S^N C_1\right)$$

$$= S R_1 C_1 + S R_1 C_1 + S R_1 C_1 + \cdots + S R_1 C_1$$

$$= N S R_1 C_1 \qquad \boxed{\tau_r = R_1 C_1} \qquad \boxed{S\tau_r = S R_1 C_1}$$

$$= \boxed{N S \tau_r}$$

Equalize the signal delay through each stage

$$C_L = S^N C_1 \qquad S^N = \frac{C_L}{C_1}$$

$$\ln(S^N) = N \ln(S) = \ln\left(\frac{C_L}{C_1}\right)$$

$$N = \frac{\ln\left(\frac{C_L}{C_1}\right)}{\ln(S)}$$

# of stages

$$\tau_d = N S \tau_r = \tau_r \ln\left(\frac{C_L}{C_1}\right)\left(\frac{S}{\ln S}\right)$$

$$\tau_r = R_1 C_1$$

for the min delay

$$\frac{\partial \tau_d}{\partial S} = 0 \Rightarrow \frac{\partial}{\partial S}\left[\frac{S}{\ln(S)}\right] = 0$$

$$\ln(S) = 1 \Leftarrow \left(\frac{\ln(S) - S \cdot \frac{1}{S}}{(\ln(S))^2} = 0\right)$$

$\tau_d$ minimum when size factor $S = e$

$$N = \frac{\ln\left(\frac{C_L}{C_1}\right)}{\ln(S)}$$

# of stages

$S = e$

$$N = \ln\left(\frac{C_L}{C_1}\right)$$

# of stages which give the min. $\tau_d$

$$\tau_d = N S \tau_r = \tau_r \ln\left(\frac{C_L}{C_1}\right)\left(\frac{S}{\ln S}\right)$$

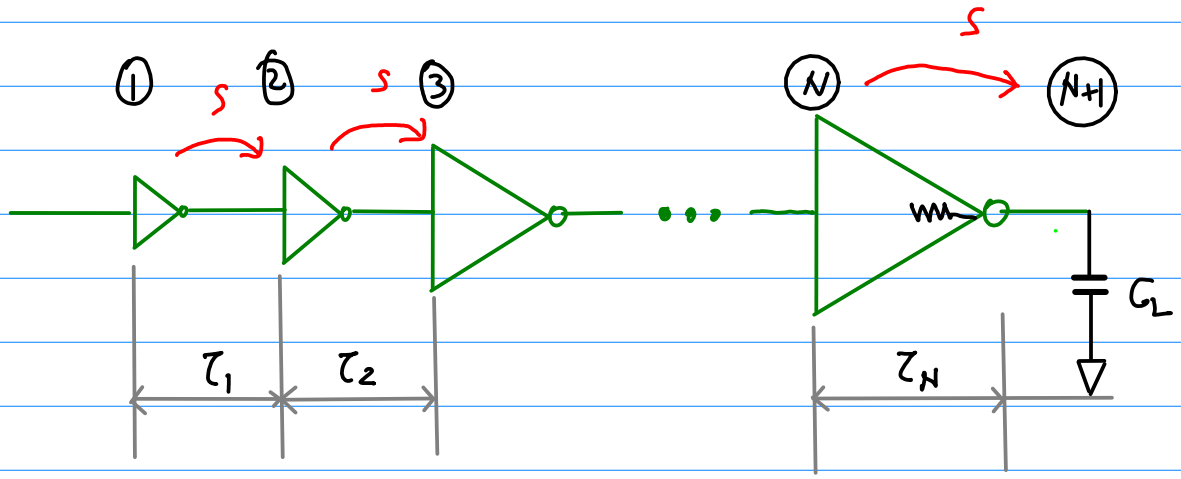
$\tau_r = R_1 C_1$

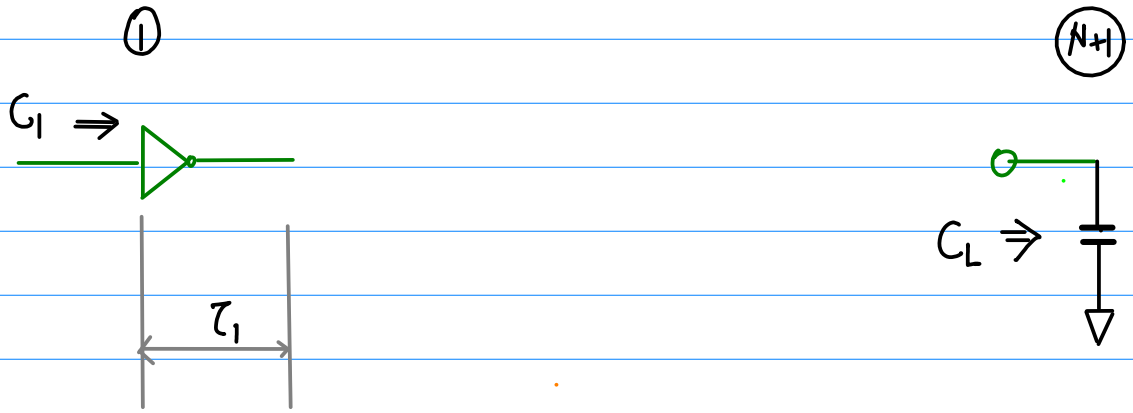
$S = e$

$$\tau_d = N e \tau_r = \tau_r \ln\left(\frac{C_L}{C_1}\right) e$$

$\tau_r = R_1 C_1$

min. delay



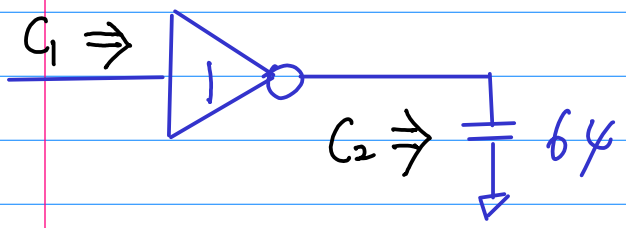

$$H = \frac{C_L}{C_1}$$

$$N = \ln\left(\frac{C_L}{C_1}\right)$$

$$\tau_d = N \cdot \tau_r = \ln\left(\frac{C_L}{C_1}\right) \cdot \tau_r$$

* parasitic capacitance ignored

# Ignoring $C_{par}$

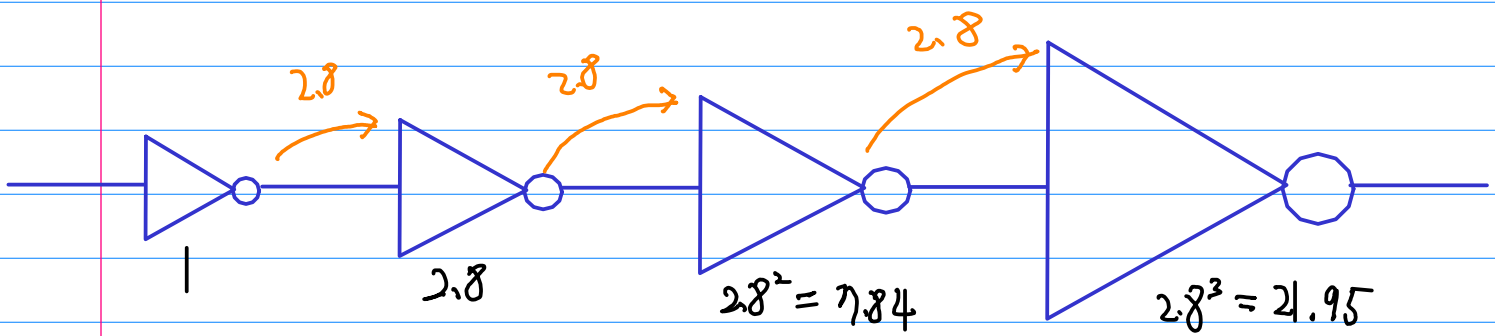



$$N = \ln\left(\frac{C_L}{C_1}\right) = \ln(64) = 4.15 \Rightarrow \boxed{N = 4}$$

$$\tau_d = \ln\left(\frac{C_L}{C_1}\right) S\,\tau_r = S \ln(64)\,\tau_r \qquad (\tau_r = R_1 C_1)$$

$$S = \left(\frac{C_L}{C_1}\right)^{\frac{1}{N}} = 64^{\frac{1}{4}} = \underline{2.8}$$

$$= 64^{\frac{1}{4.15}} \Rightarrow e = 2.718$$




$$\tau_d = 2.8 \ln(64)\,\tau_r = 11.6\,\tau_r$$

# Case II: $p$ ← Parasitic capacitance

## parasitic delay ($p$)

- delay due to internal parasitic capacitance ($sC_p$)
- excluding external load cap ($C_L$)
- count only diffusion capacitance of the output
- delay without output load (zero load)

$$p = \frac{C_{p,ref}}{C_{ref}}$$

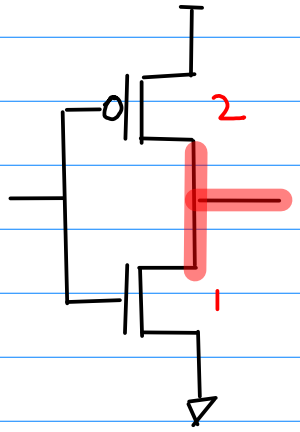
$C_{p,ref}$ ← $C_{dp} + C_{dn}$ drain parasitic cap

$C_{ref}$ ← $C_{in}$ of the ref inverter (Symmetric Inverter)

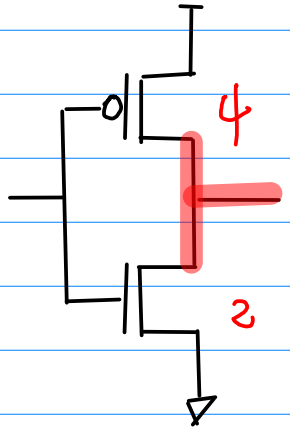
$$p = \frac{\tau_{par}}{\tau_{ref}} = \left(\frac{R_{ref} \cdot C_{p,ref}}{R_{ref} \cdot C_{ref}}\right)$$

$C_{in}$ of a reference inverter
(symmetric inverter)

$$p = \frac{1}{3}\left(\sum \text{Output scaling factors}\right)$$

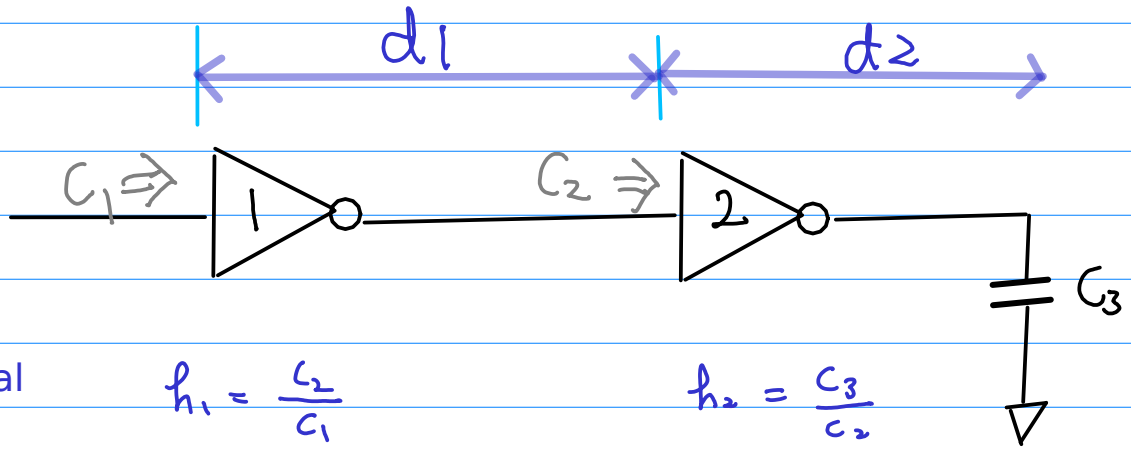



$p = \frac{3}{3} = 1$




$p = \frac{6}{3} = 2.$

Using $d_i = g_i h_i + p_i$




Electrical Effort

$h_1 = \frac{C_2}{C_1}$ $\qquad$ $h_2 = \frac{C_3}{C_2}$

Logical Effort

$g_1 = 1$ (inverter) $\qquad$ $g_2 = 1$ (inverter)

Normalized path delay

$$D = \sum_i \text{individual delays}$$

$$= d_1 + d_2$$

$$= (g_1 h_1 + p_1) + (g_2 h_2 + p_2)$$

$$= (h_1 + p_1) + (h_2 + p_2)$$

$$= \left(\frac{C_2}{C_1} + p_1\right) + \left(\frac{C_3}{C_2} + p_2\right)$$

# Path Electrical Effort

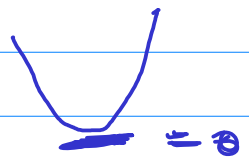
$$H = \frac{C_{last}}{C_{first}} = \frac{C_3}{C_1} = \left(\frac{C_2}{C_1}\right)\cdot\left(\frac{C_3}{C_2}\right) = h_1 h_2$$

$$h_2 = \frac{H}{h_1}$$

Path delay $\quad D = (h_1 + p_1) + \left(\frac{H}{h_1} + p_2\right)$

Minimize path delay $\quad D(h_1, h_2)$

$$\Rightarrow \frac{\partial D}{\partial h_1} = \frac{\partial}{\partial h_1}\left[(h_1 + p_1) + \left(\frac{H}{h_1} + p_2\right)\right] = 0$$




$$= \quad 1 - \frac{H}{h_1^2} = 0$$

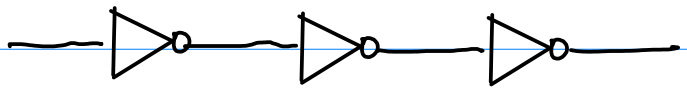
$$\frac{1}{h_1^2}\left(h_1^2 - h_1 h_2\right) = \frac{1}{h_1}\left(h_1 - h_2\right) = 0$$

when $\boxed{h_1 = h_2}$, $D(h_1, h_2)$ has a minimum.

minimum delay

by equalizing the delay through each stage

$\boxed{d_1 = d_2}$



Path Delay $D = (h_1 + p_1) + (h_2 + p_2) + (h_3 + p_3)$

$$\frac{h_1 + h_2 + h_3}{3} \geq \sqrt[3]{h_1 h_2 h_3}$$

$$h_1 + h_2 + h_3 \geq 3\sqrt[3]{h_1 h_2 h_3} = 3H^{\frac{1}{3}}$$

minimum when $h_1 = h_2 = h_3$

arithmetic average $\geq$ geometric average

# N ?

By ignoring parasitic capacitance

$$N = \frac{\ln\left(\frac{C_L}{C_1}\right)}{\ln(S)}$$

# of stages

$S = e$

$$N = \ln(H)$$

# of stages which give the min. $\tau_d$

$$D = N\sqrt[N]{H} + N$$

Path Delay

$$D = \sum_i d_i = D_F + P$$
$$= \sum_i f_i + \sum_i p_i$$

$$\forall i \quad \hat{f} = f_i = g_i h_i = F^{1/N}$$ equal delay

$$f_1 + f_2 + \cdots + f_N = g_1h_1 + g_2h_2 + \cdots + g_Nh_N$$
$$\geq (g_1h_1)(g_2h_2)\cdots(g_Nh_N)$$

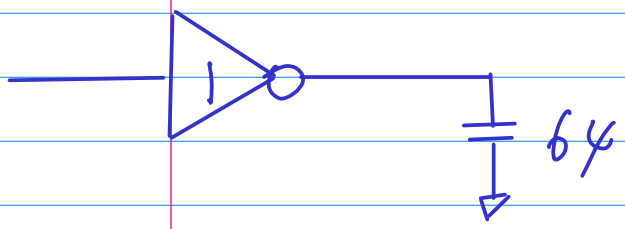
Path Effort $F = GBH$ $F = GH$

$$G = \prod g_i$$
$$H = \frac{C_{out}}{C_{in}}$$
$$B = \prod b_i$$

$$G = \prod g_i$$
$$H = \frac{C_{out}}{C_{in}}$$
$$B = 1$$

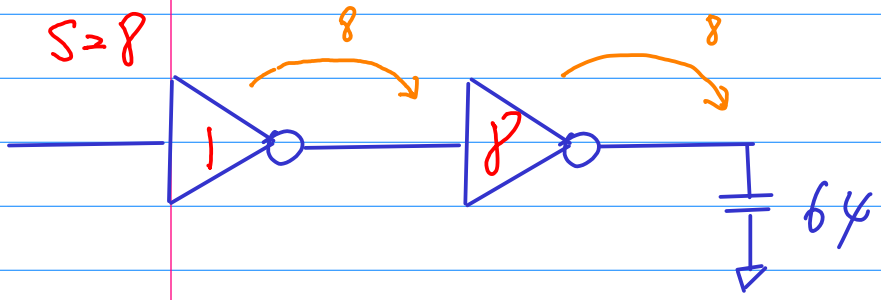
$$D = \sum_i d_i = \sum_i f_i + \sum_i p_i$$
$$= N F^{1/N} + N$$

$$D = N\sqrt[N]{H} + N$$



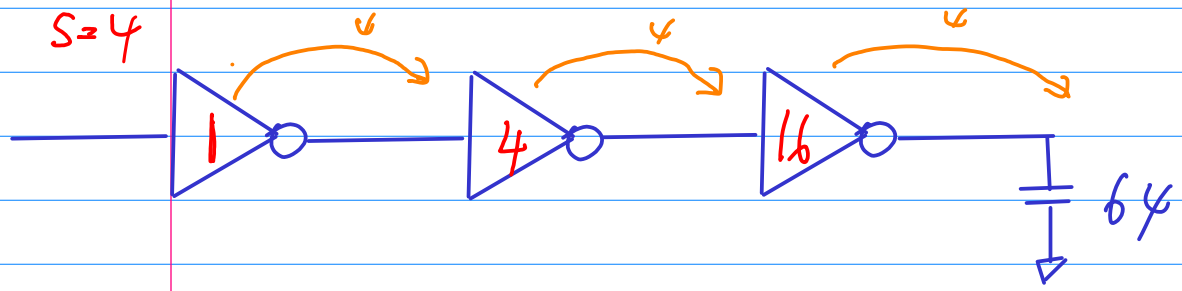

**N=1**
$f = 64$

$D = (gh + p) = (1 \cdot 64 + 1) = 65$



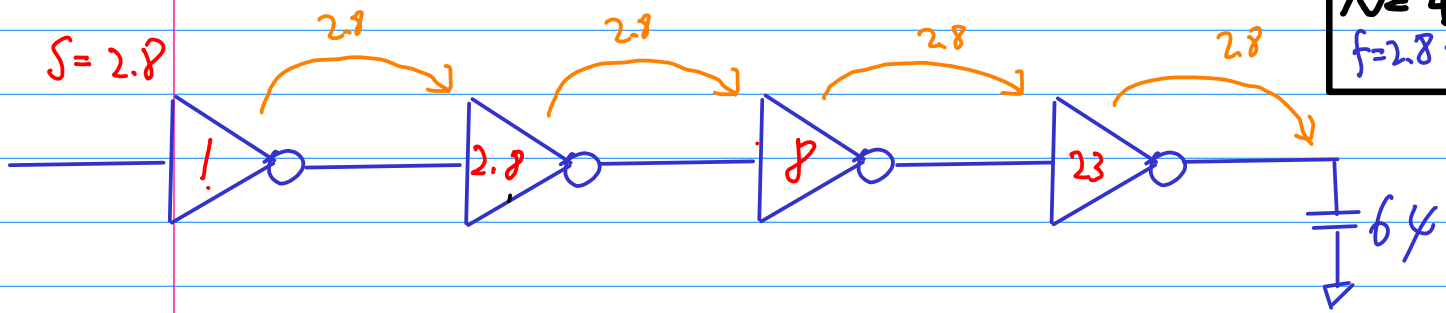

**N=2**
$f = 8 = (64)^{\frac{1}{2}}$

$D = (1 \cdot 8 + 1) \cdot 2 = 18$



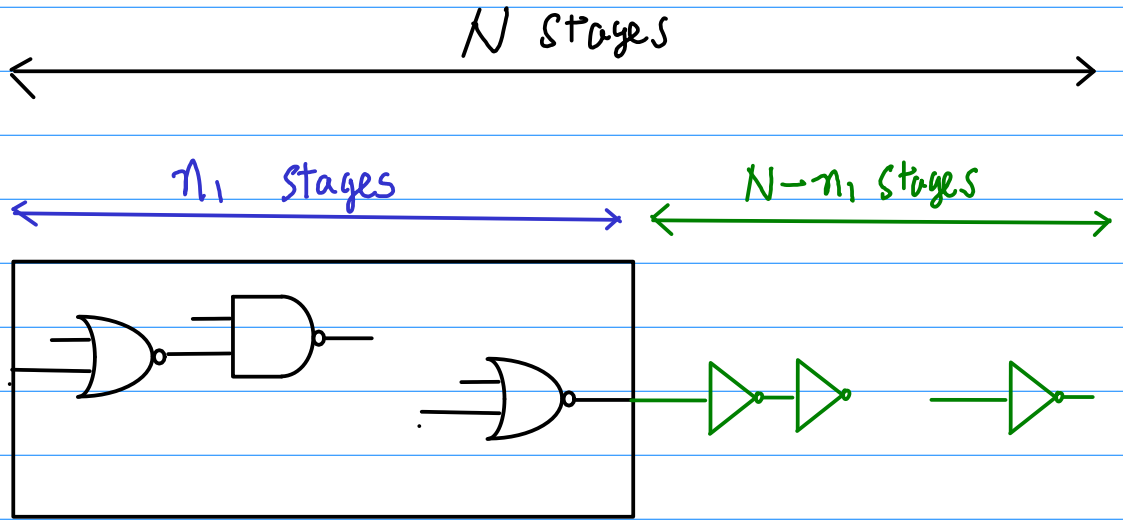

**N=3**
$f = 4 = (64)^{\frac{1}{3}}$

$D = (1 \cdot 4 + 1) \cdot 3 = 15$




**N=4**
$f = 2.8 = (64)^{\frac{1}{4}}$

$D = (1 \cdot 2.8 + 1) \cdot 4 = 15.2$




$$D = \underbrace{g_1h_1}_{+p_1} + \underbrace{g_2h_2}_{+p_2} + \cdots + \underbrace{g_{n_1}h_{n_1}}_{+p_{n_1}} + \underbrace{g_{n_1+1}h_{n_1+1}}_{+p_{inv}} + \cdots + \underbrace{g_Nh_N}_{+p_{inv}}$$

$$D = g_1h_1 + g_2h_2 + \cdots + g_Nh_N \geq (g_1h_1)(g_2h_2)\cdots(g_Nh_N)$$
$$= (g_1g_2\cdots g_N)(h_1h_2\cdots h_N) = GH = F$$

$$g_1h_1 = g_2h_2 = \cdots = g_Nh_N = F^{1/N} \rightarrow \text{minimum } D$$

$$D = NF^{1/N} + \sum_{i=1}^{n_1} p_i + (N-n_1)p_{inv}$$

$p_i$ : i-th stage parasitic capacitance $(1 \leq i \leq n_1)$

$p_{inv}$ : inverter " " $(n_1+1 \leq i \leq N)$

$$D = N F^{1/N} + \sum_{i=1}^{n_1} p_i + (N - n_1)\, p_{inv}$$

Find $N$ s.t $\frac{\partial D}{\partial N} = 0$ for minimum delay $D$

$$\frac{d}{dx}(c^{ax}) = c^{ax} \ln c \cdot a, \qquad c > 0$$

$$\frac{\partial D}{\partial N} = F^{1/N} + \left(N\right)\left(\frac{-1}{N^2}\right)\left(F^{1/N}\right) \ln F + p_{inv}$$

$$= F^{1/N} - \left(\frac{1}{N} \ln F\right) F^{1/N} + p_{inv}$$

$$= -\left(\ln F^{1/N}\right) F^{1/N} + F^{1/N} + p_{inv} = 0$$

Let $\boxed{F^{1/N} = \rho}$

$$\frac{\partial D}{\partial N} = p_{inv} - \rho \ln \rho + \rho = \boxed{p_{inv} + \rho(1 - \ln \rho) = 0}$$

$$F^{1/N} = \rho \qquad \ln F^{1/N} = \ln \rho \qquad \frac{1}{N} \ln F = \ln \rho$$

$$\boxed{\frac{\partial D}{\partial N} = 0} \longrightarrow \boxed{N = \frac{\ln F}{\ln \rho} = \log_\rho F}$$

$$\frac{\partial D}{\partial N} = p_{inv} - \rho \ln \rho + \rho$$

$$= p_{inv} + \rho(1 - \ln \rho) = 0$$

assume $p_{inv} = 0$ → $\rho(1 - \ln \rho) = 0$

$\rho = 0$, $\ln \rho = 1$ $\rho = e = 2.718$

assume $p_{inv} = 1$ → $p_{inv} + \rho(1 - \ln \rho) = 0$

numerical solution $\rho = 3.59$

$$D = N F^{1/N} + \sum_{i=1}^{n_1} p_i + (N - n_1)\, p_{inv}$$

$$F^{1/N} = \rho$$

$$\frac{\partial D}{\partial N} = p_{inv} + \rho(1 - \ln \rho) = 0$$

$p_{inv} = 0 \rightarrow \rho = e = 2.718 \rightarrow$ min D

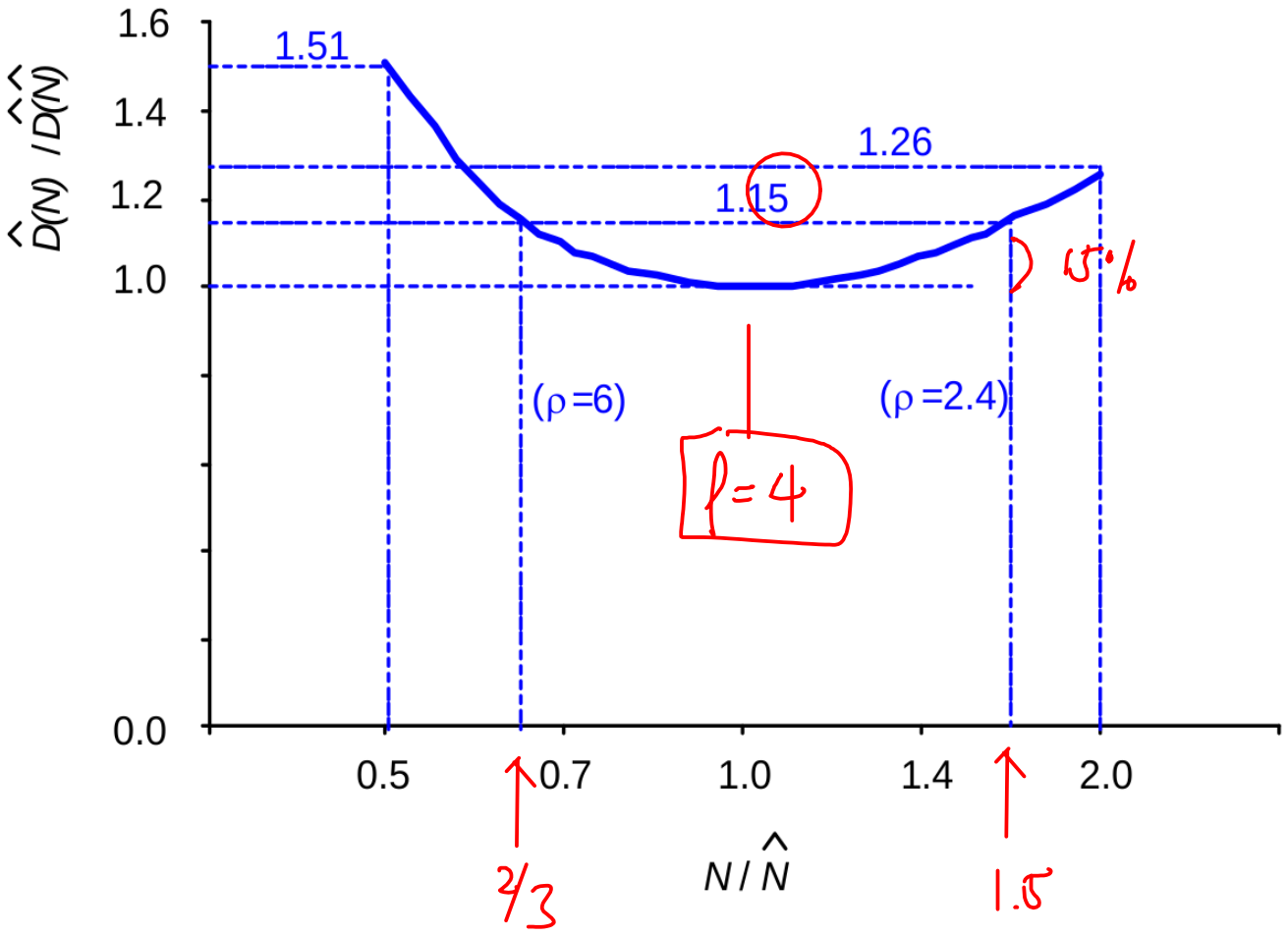
$p_{inv} = 1 \rightarrow \rho = 3.59 \rightarrow$ min D

$F^{1/N} = \rho \qquad \ln F^{1/N} = \ln \rho \qquad \frac{1}{N} \ln F = \ln \rho$

$$N = \frac{\ln F}{\ln \rho} = \log_\rho F \qquad \text{\# of stages}$$

$N = \log_\rho F \approx \hat{N}$ — integer approximation

$\hat{D}(N) \qquad \hat{D}(\hat{N})$


1.6
1.4
1.2
1.0
0.0
$\hat{D}(N) / \hat{D}(N)$
1.51
1.26
1.15
(ρ=6)
(ρ=2.4)
0.5
0.7
1.0
1.4
2.0
$N / \hat{N}$
2/3
1.5
5%
ρ=4

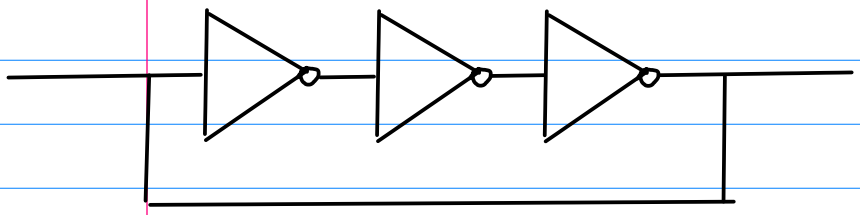
# Ring Oscillators

a uniform way of measuring $t_p = \frac{t_{pr} + t_{pf}}{2}$

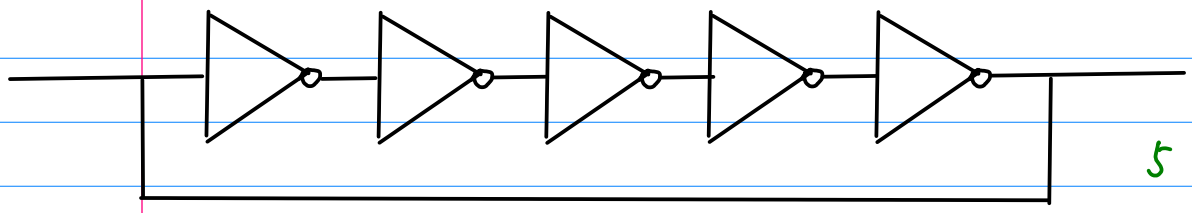
ring oscillator

odd number of inverters
connected in circular chain

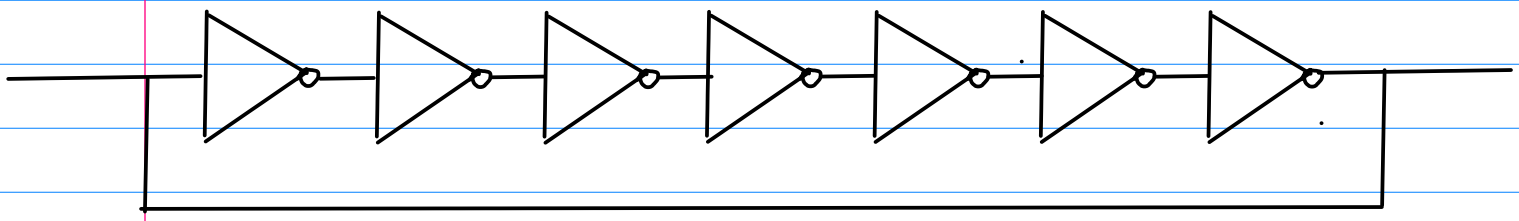
# Odd Number of Inverters



3 inverters



5 inverters

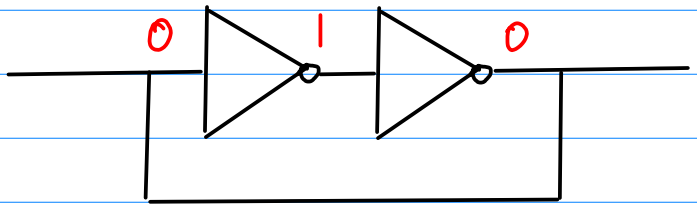


n inverters

Odd number of inverters

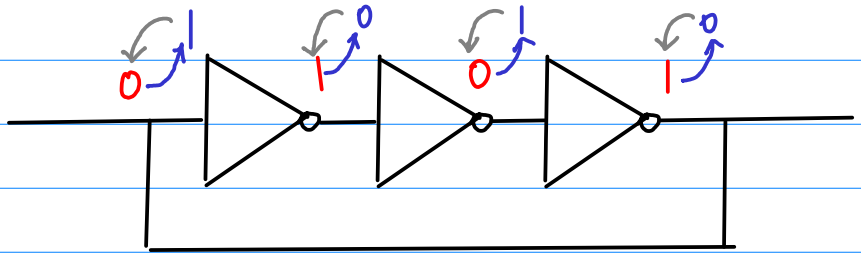
No stable operating points → Oscillating

ring oscillator



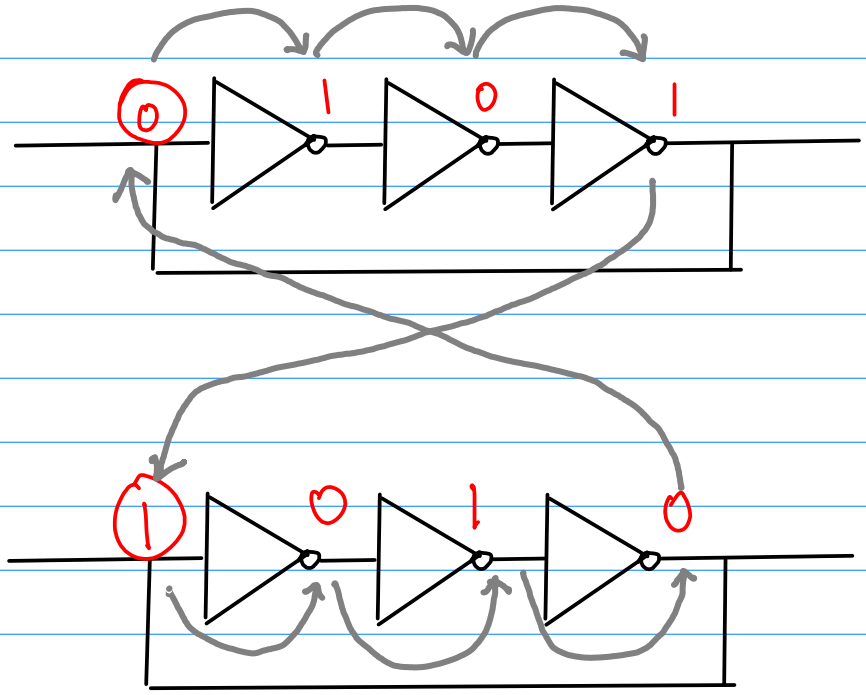

Stable

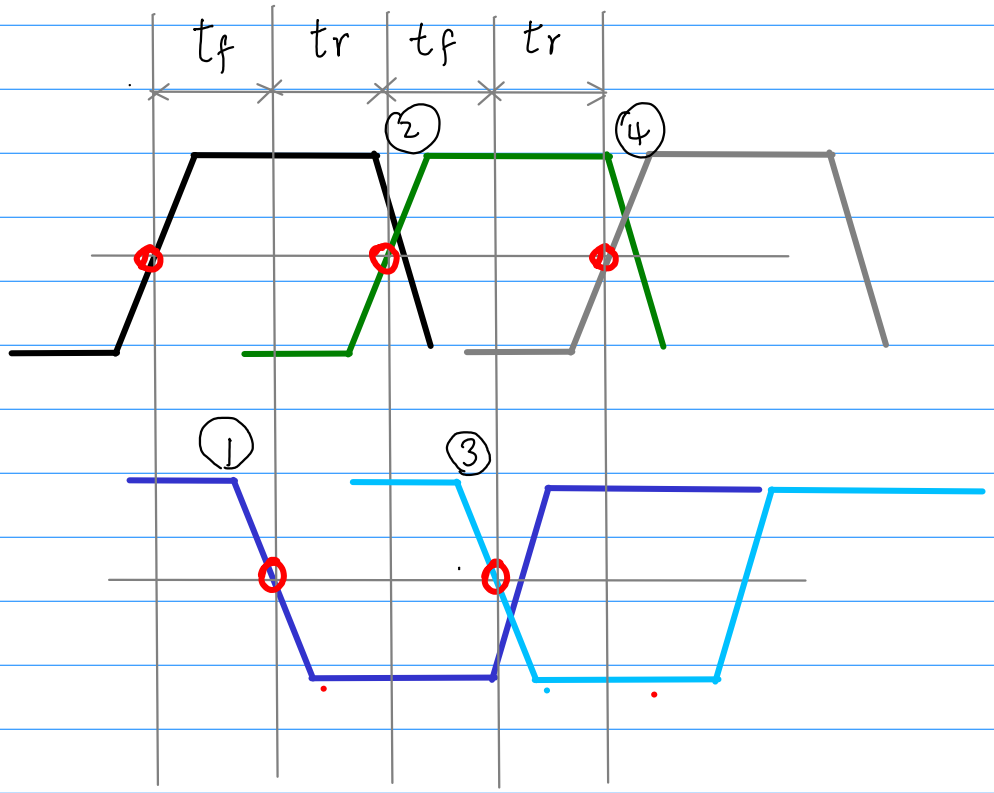
latch

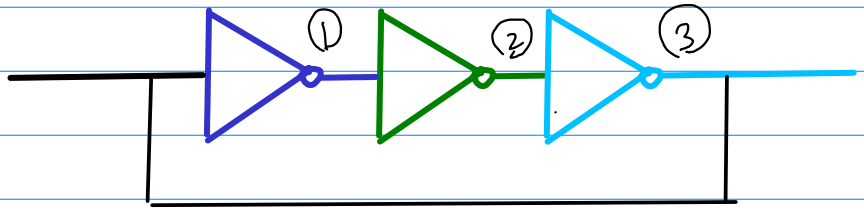


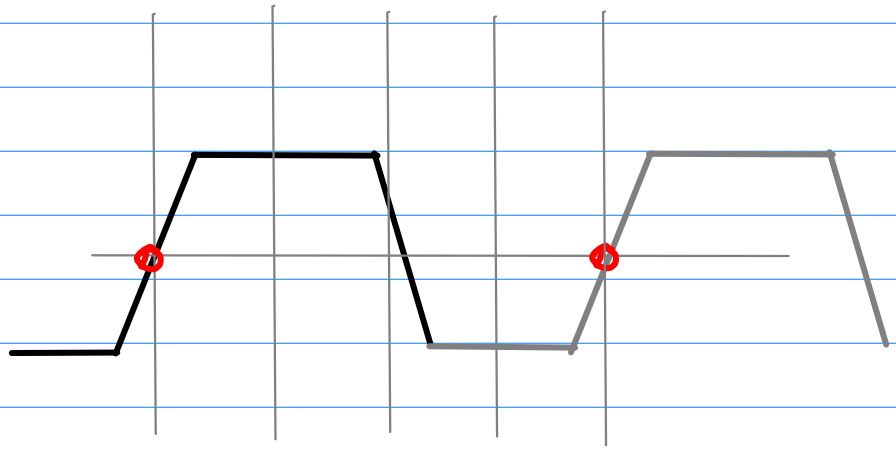

Astable

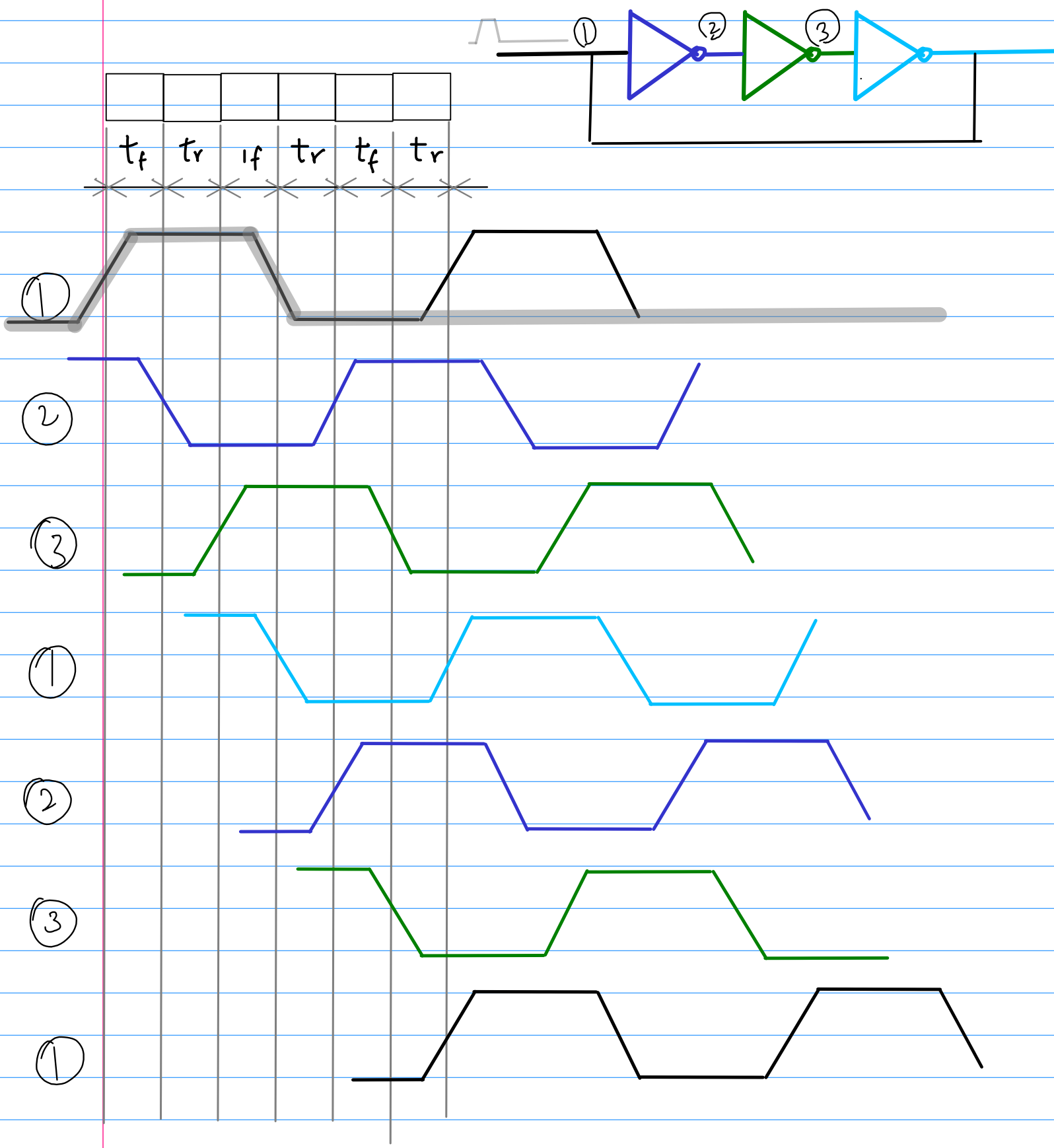
ring oscillator

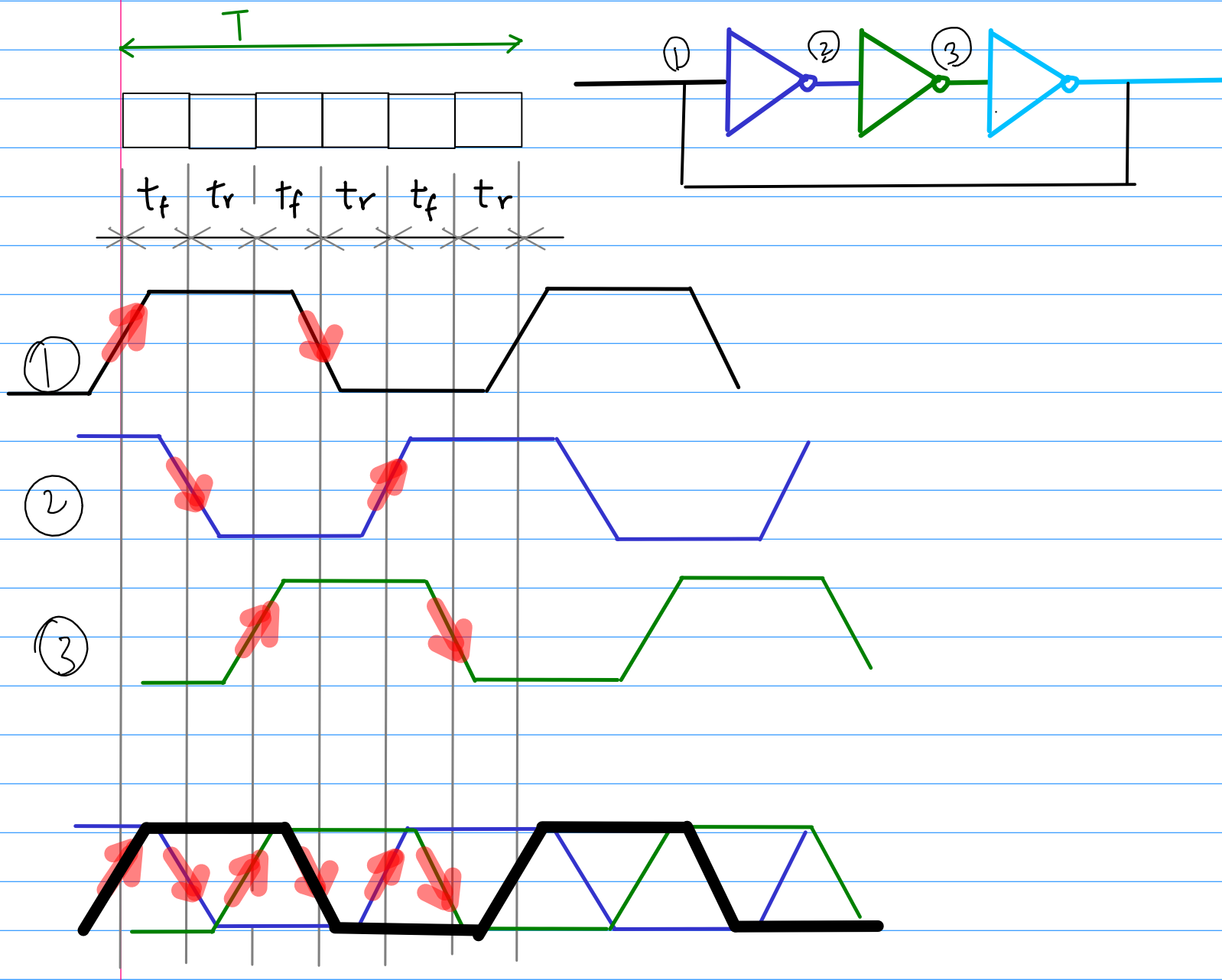


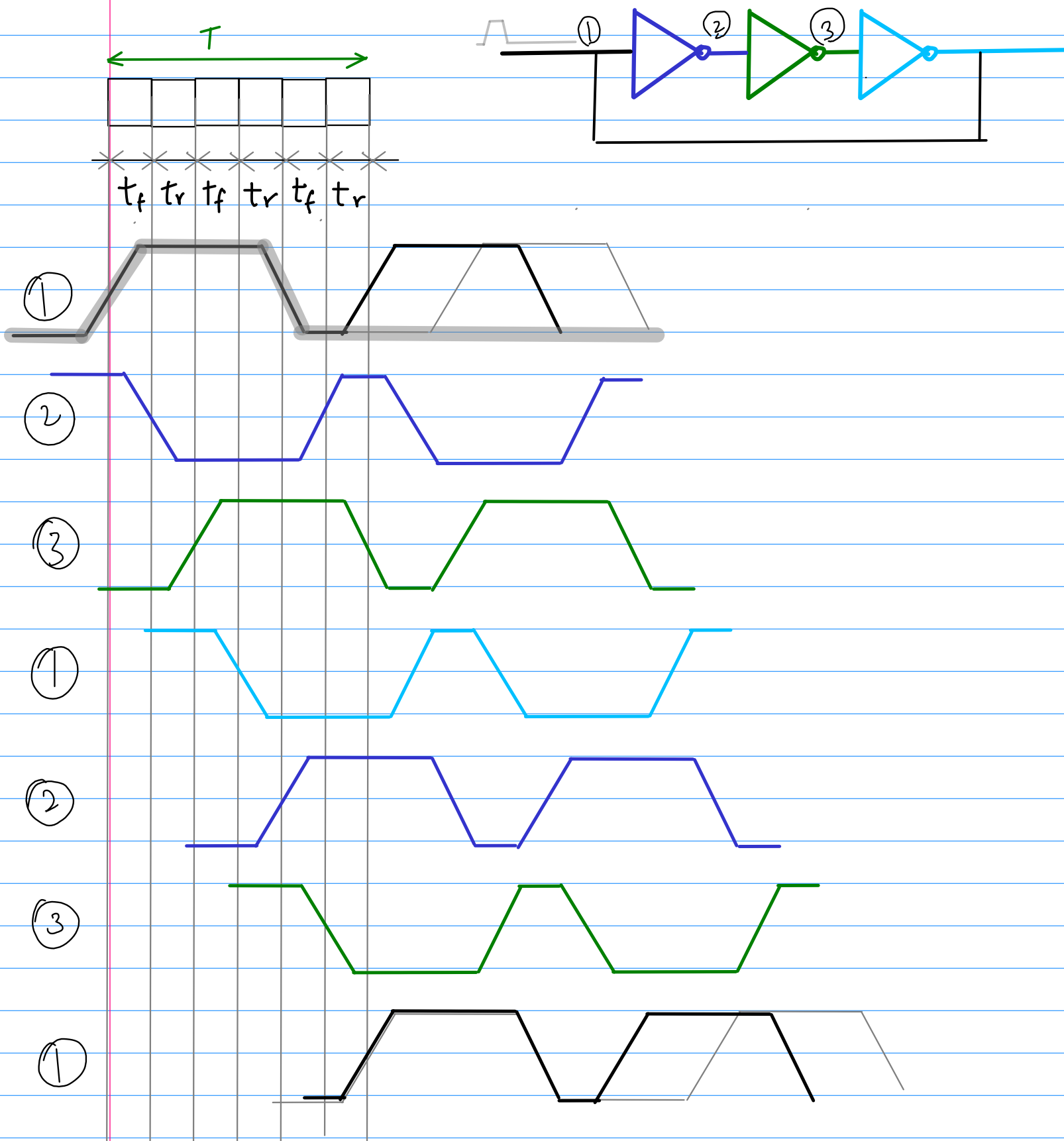

tf
tr
tf
tr
2
4
1
3

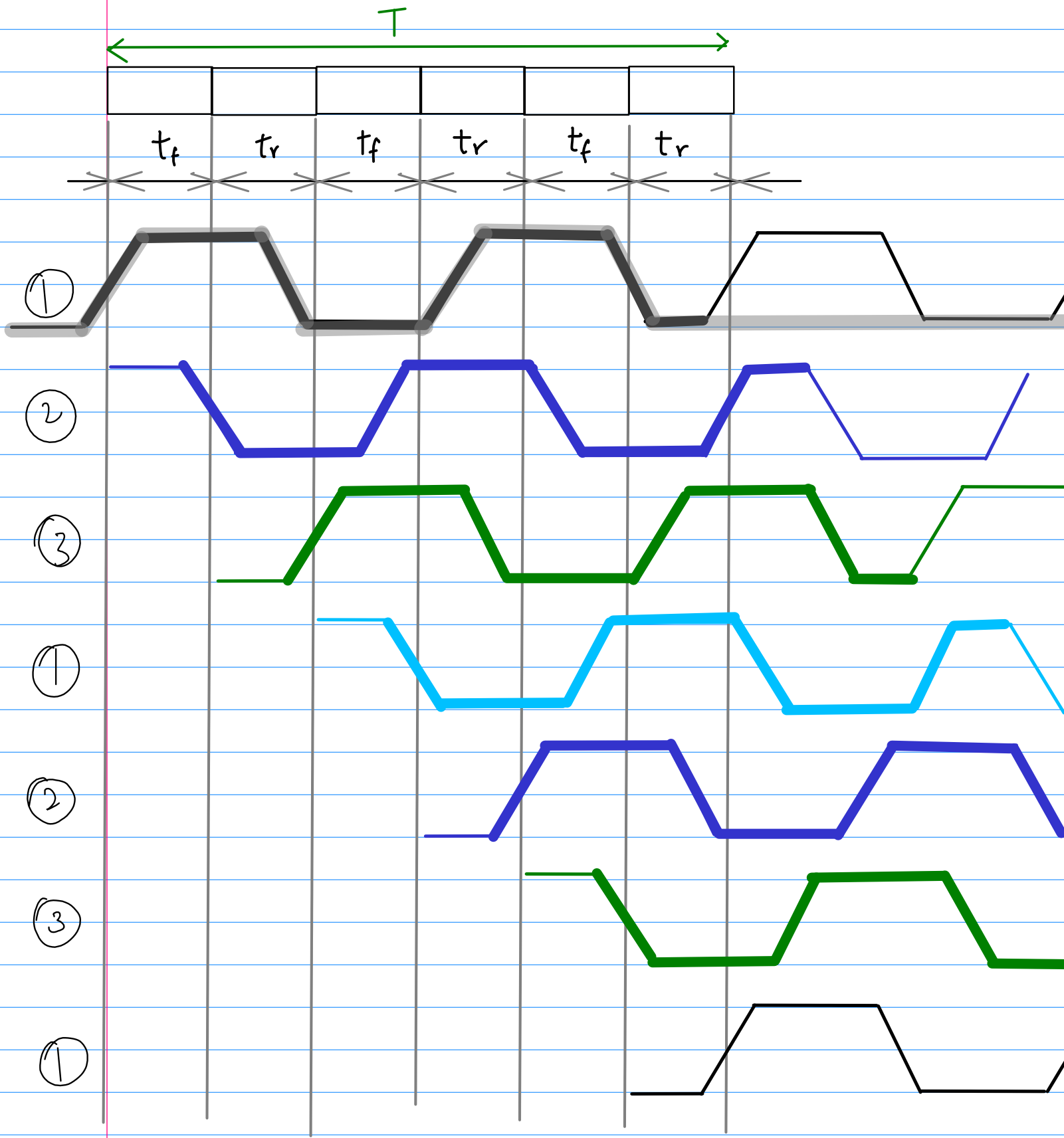

1
2
3




①
②
③
$t_f$
$t_r$
$t_f$
$t_r$
$t_f$
$t_r$
①
②
③
①
②
③
①


T
$t_f$
$t_r$
$t_f$
$t_r$
$t_f$
$t_r$
①
②
③
①
②
③


T
$t_f$ $t_r$ $t_f$ $t_r$ $t_f$ $t_r$
①
②
③
①
②
③
①


T
$t_f$
$t_r$
$t_f$
$t_r$
$t_f$
$t_r$
①
②
③
①
②
③
①

$$T = 2 \cdot t_p \cdot N$$

$t_p$: propagation delay
$N$: # of inverters in chain

$$T \gg t_f + t_r$$

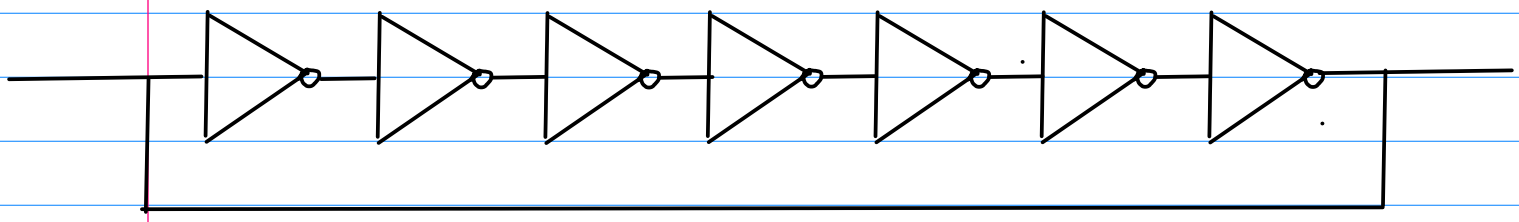
- used to measure the average propagation delay of a typical inverter with minimum capacitive loading

$$t_p = \frac{T}{2 \cdot N}$$

Characterise a particular design / fabrication process

- used as a simple on chip clock

N inverters (odd number)



$$g = \frac{C_{in}}{C_{ref}} = \frac{C_{ref}}{C_{ref}} = 1$$

$$h = \frac{C_{out}}{C_{in}} = \frac{C_{ref}}{C_{ref}} = 1$$

$$p = \left(\frac{C_{p,ref}}{C_{ref}}\right) = \left(\frac{\text{internal diffusion cap}}{\text{gate cap of ref inv}}\right) = \frac{3}{3} = 1$$

$$d = gh + p = 2 \qquad d_{abs} = 2\tau$$

$$f_{req} = \frac{1}{2N\, d_{abs}} = \frac{1}{4N\tau}$$