CMOS Delay-4 (H.4)
Device Delay
(Inv, NAND, NOR)

20161105

References

Some Figures from the following sites

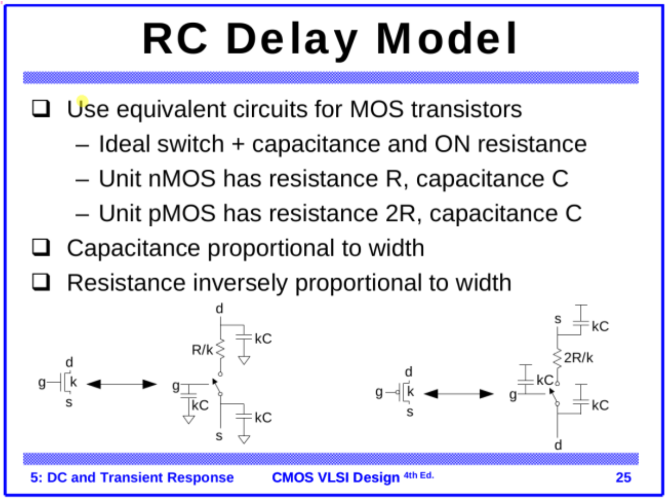
[1] http://pages.hmc.edu/harris/cmosvlsi/4e/index.html
Weste & Harris Book Site

[2] en.wikipedia.org

MODEL

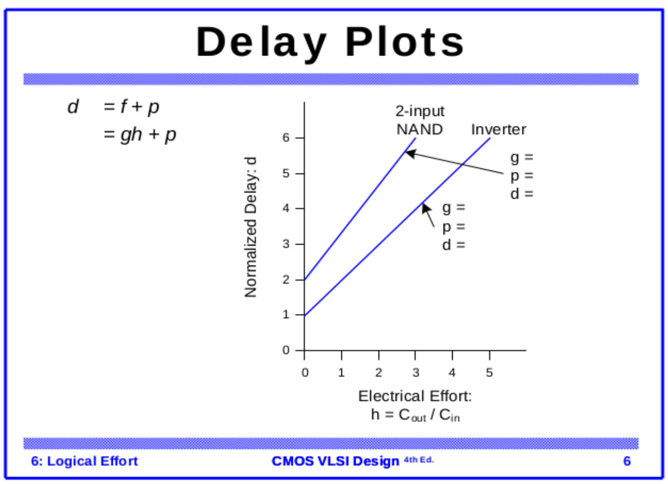
① RC Delay Model

Weste & Harris



② Linear Delay Model

Weste & Harris



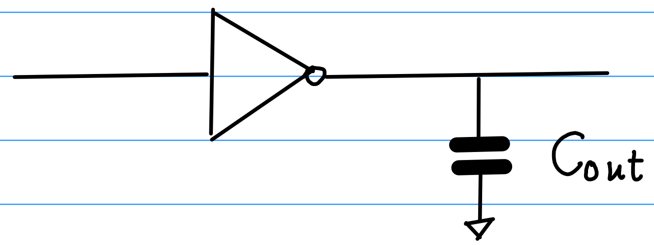
③ Analytic Delay Model

Mead & Conway
Weste & Eshraghian
Uyemura

Inverter Delay

for every kind of inverter

$$g = 1$$



Normalized Delay

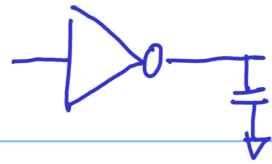
$$d = (p + g \cdot h) = (p + h)$$

$$= \frac{d_{abs}}{Z_{ref}}$$

Absolute Delay

$$d_{abs} = Z_{ref}(p + h)$$

Inverter Delay



$g = 1$

Absolute Delay

$$d_{abs} = \tau \cdot (p + h)$$

Normalized Delay

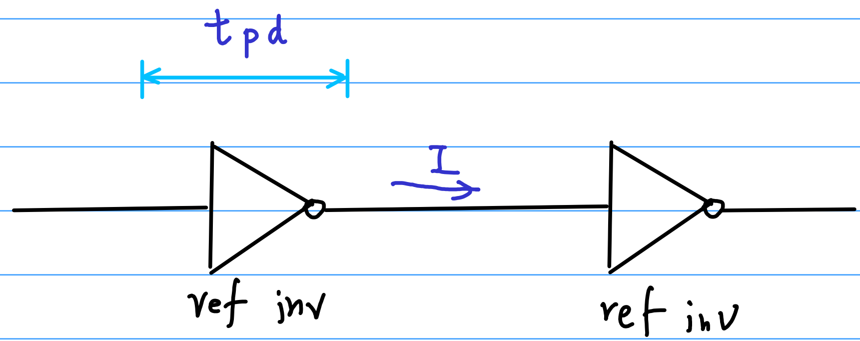
$$d = \frac{d_{abs}}{\tau} = (p + h)$$

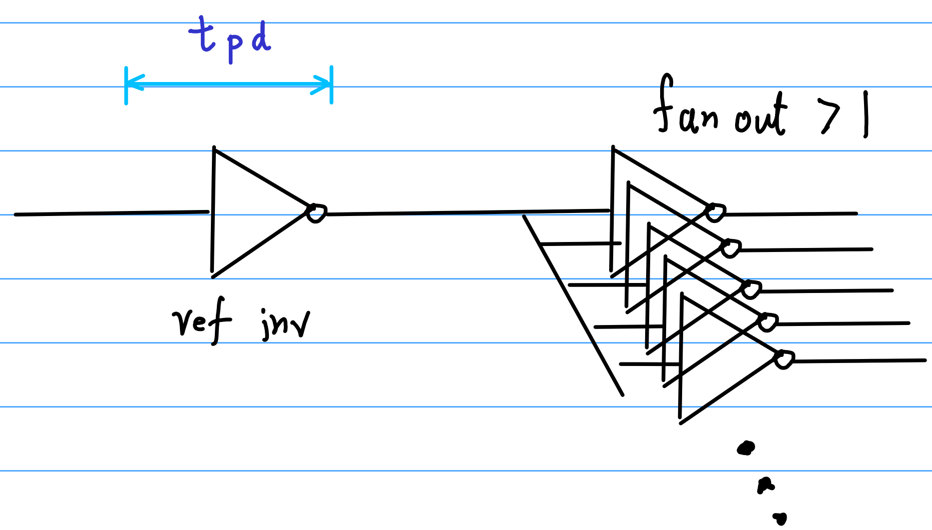
τ reference time constant

h : Electrical Effort $\left(\frac{C_{out}}{C_{in}}\right) \leftarrow C_{out}$

p : Parasitic Delay $\left(\frac{C_{p,ref}}{C_{ref}}\right) \leftarrow C_{p,ref}$

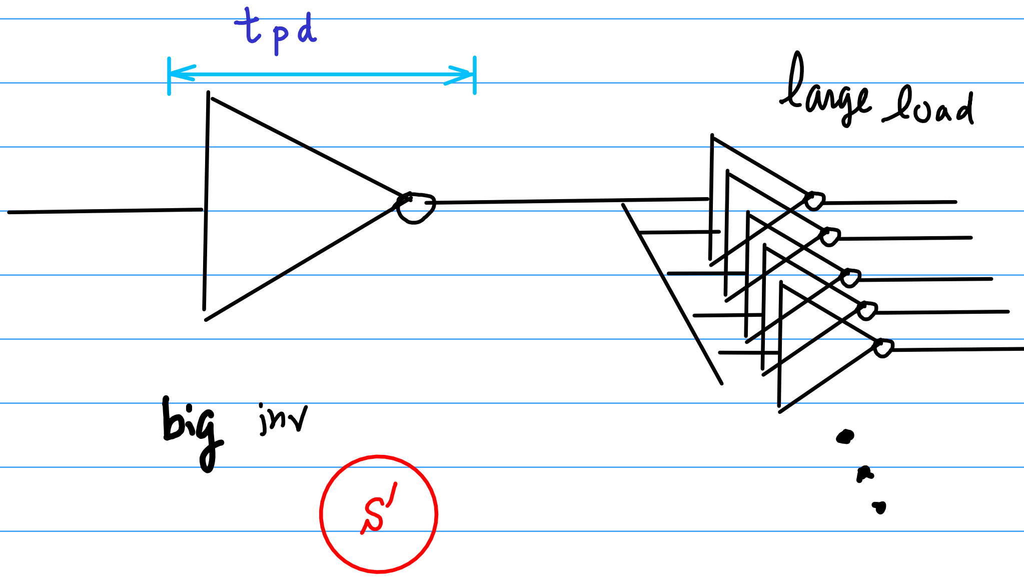
Propagation Delay

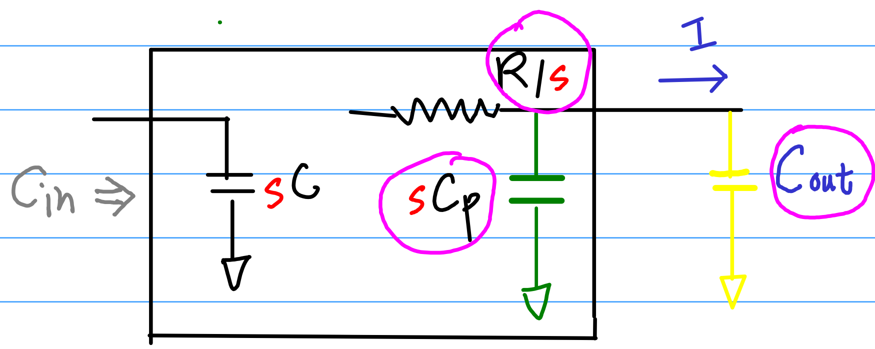




50% V_{DD} → 50% V_{DD}

to get the same current, need bigger inverter





$R \Rightarrow R_{ref}$

$R/s \cdot sC_p = R\,C_p$

fall time	$t_f =$	$0.9\ V_{DD} \rightarrow 0.1\ V_{DD}$
rise time	$t_r =$	$0.1\ V_{DD} \rightarrow 0.9\ V_{DD}$
propagation delay time	$t_p = \frac{1}{2}(t_{pf} + t_{pr})$	$0.5\ V_{DD} \rightarrow 0.5\ V_{DD}$
propagation fall time propagation rise time	t_{pf} t_{pr}	$V_{DD} \rightarrow 0.5\ V_{DD}$ $0 \rightarrow 0.5\ V_{DD}$

parasitic delay (p)

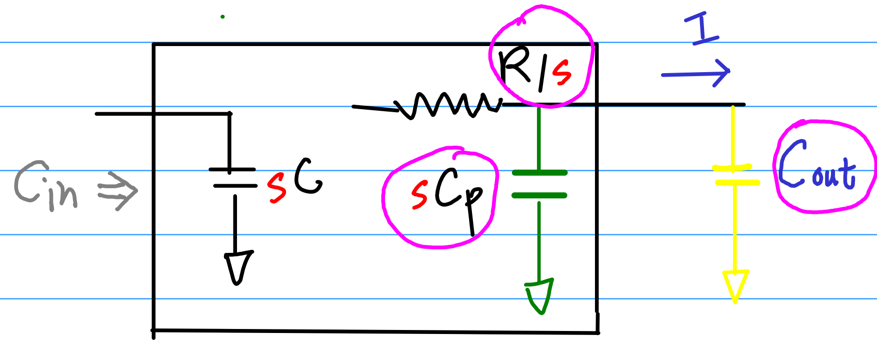
- delay due to internal parasitic capacitance — sC_p
- excluding external load cap — C_{out}
- count only diffusion capacitance of the output
- delay without output load

$$p = \frac{C_{p,ref}}{C_{ref}}$$

$C_{p,ref}$ ← $C_{dp} + C_{dn}$ drain parasitic cap

C_{ref} ← C_{in} of the ref inverter (symmetric inverter)

$R \Rightarrow R_{ref}$



$$\frac{R}{s} \cdot sC_p \approx R\,C_p$$

$$p = \left(\frac{C_{p,ref}}{C_{ref}}\right) = \left(\frac{\text{internal diffusion cap}}{\text{gate cap of ref inv}}\right)$$

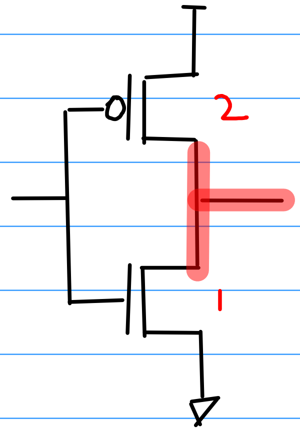
$$= \frac{\tau_{par}}{\tau_{ref}} = \left(\frac{R_{ref} \cdot C_{p,ref}}{R_{ref} \cdot C_{ref}}\right)$$

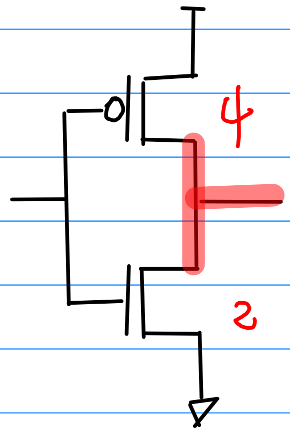
C_{in} of a reference inverter
(symmetric inverter)

$$p = \frac{\tau_{par}}{\tau_{ref}} = \left(\frac{R_{ref} \cdot C_{p,ref}}{R_{ref} \cdot C_{ref}}\right)$$

C_{ref}: Cin of a reference inverter (Symmetric inverter)

$$p = \frac{1}{3}\left(\Sigma \text{ output scaling factors}\right)$$



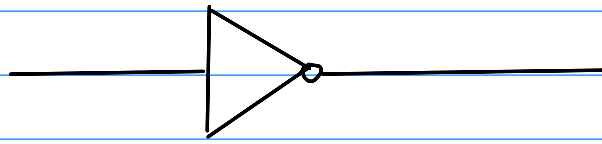


$p = \frac{3}{3} = 1$

$p = \frac{6}{3} = 2.$

reference inverter

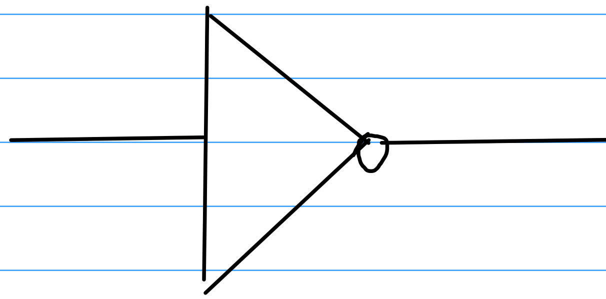
$g = 1$



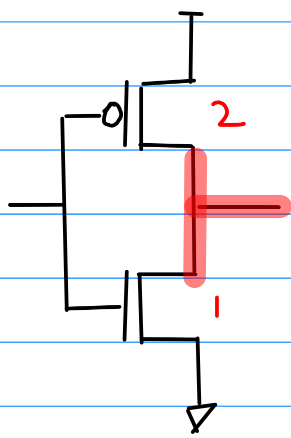
$p = 1$

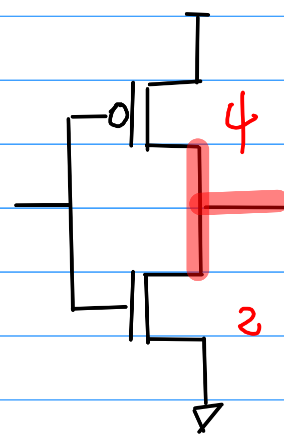
scaled inverters

$g = 1$



~~$p = 1$~~ not always





$p = \frac{3}{3} = 1$

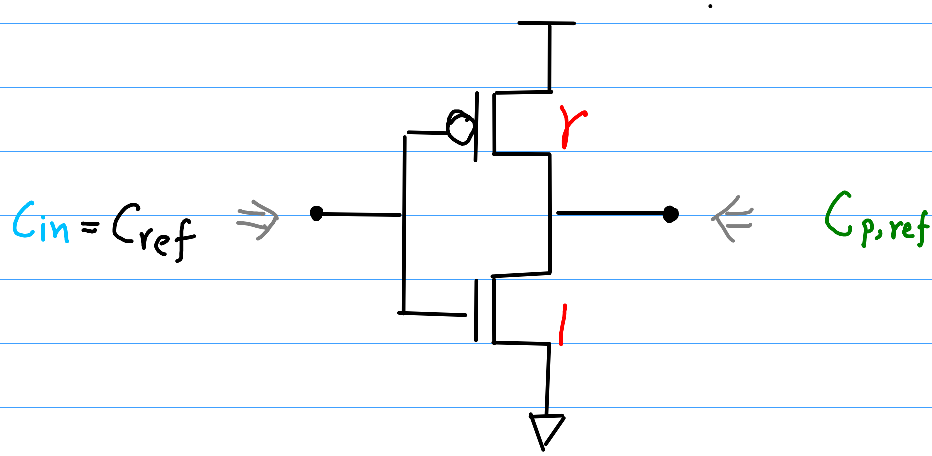
$p = \frac{6}{3} = 2.$

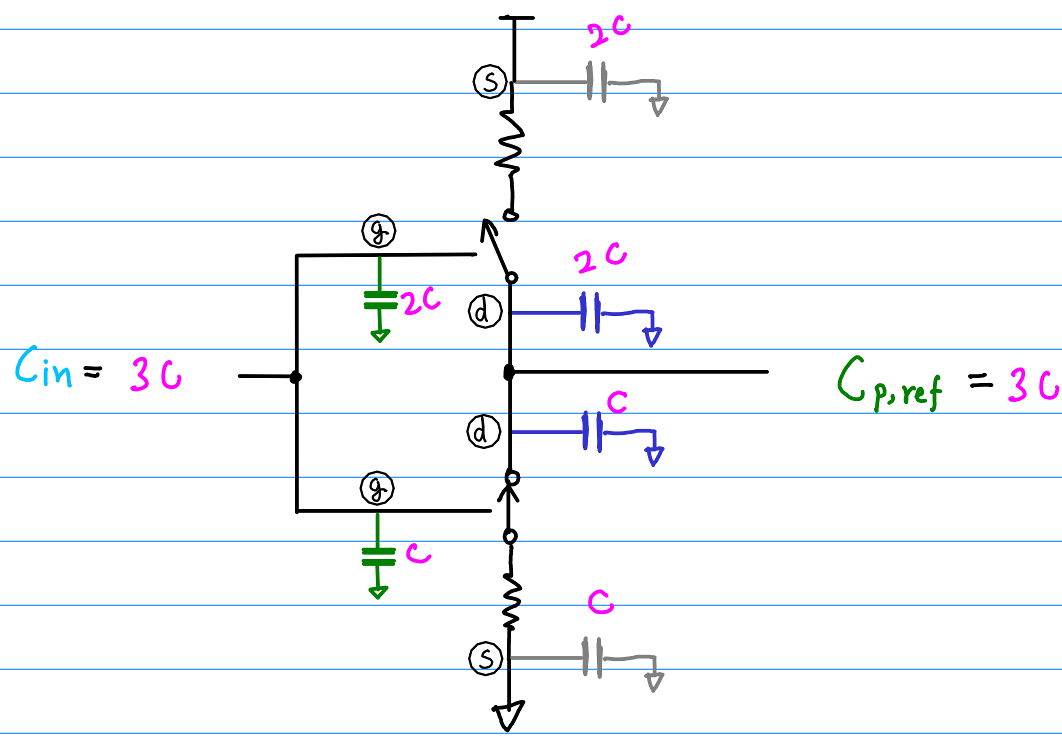
For the ref inverter

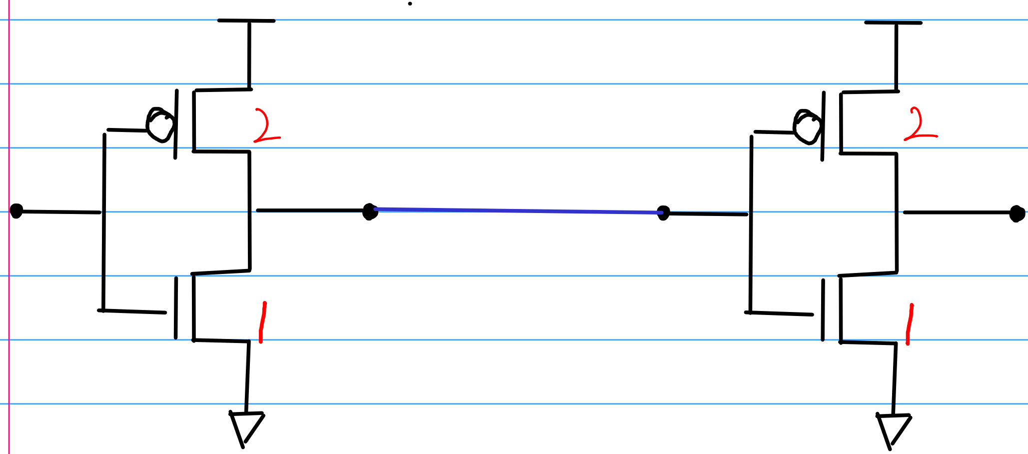
$$d_{abs} = Z_{ref}(h+1)$$

$$d = \frac{d_{abs}}{Z_{ref}} = (h+1)$$

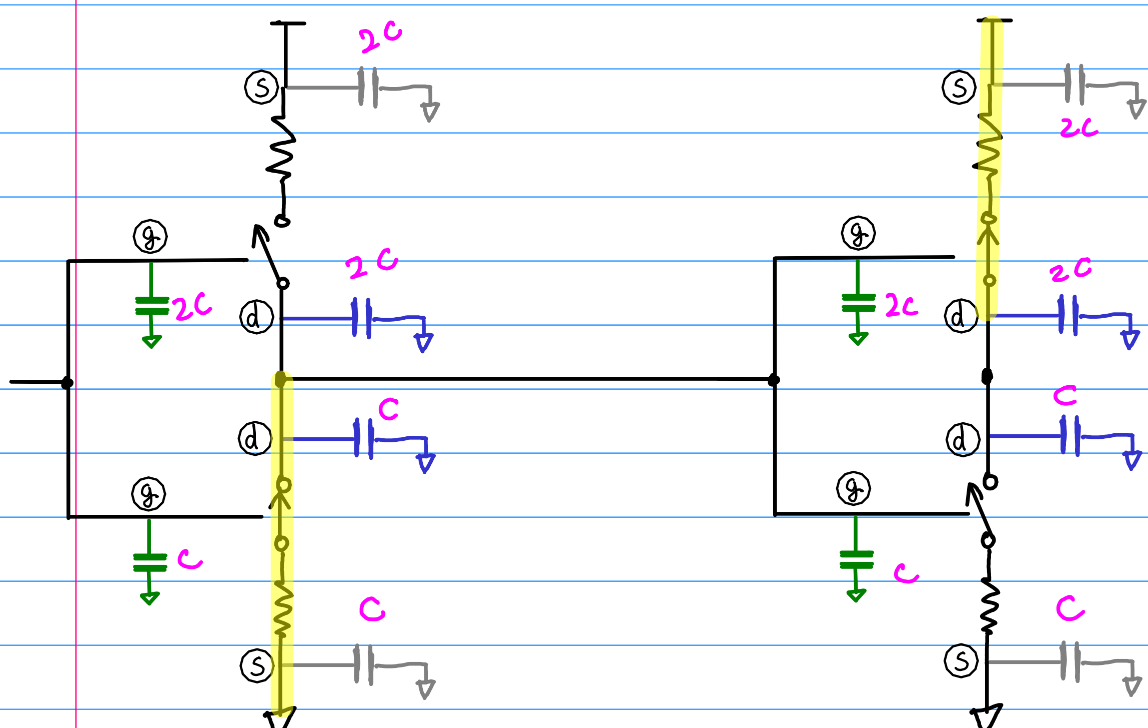
Equivalent RC Circuit



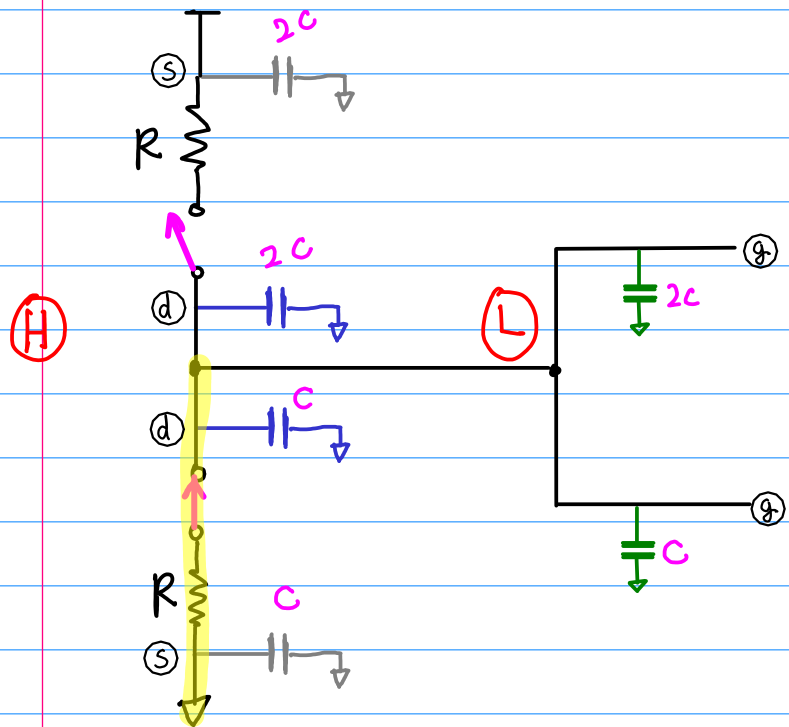


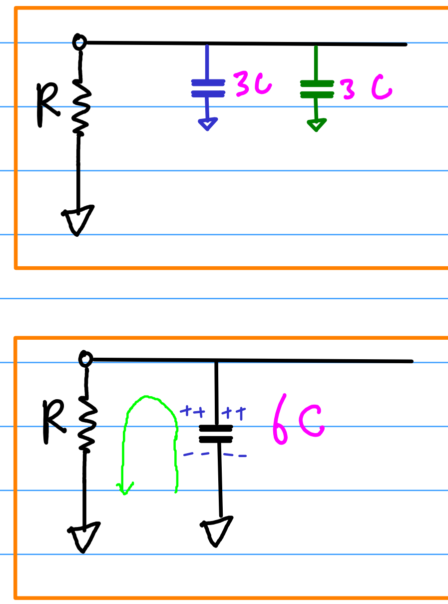


2
1
2
1

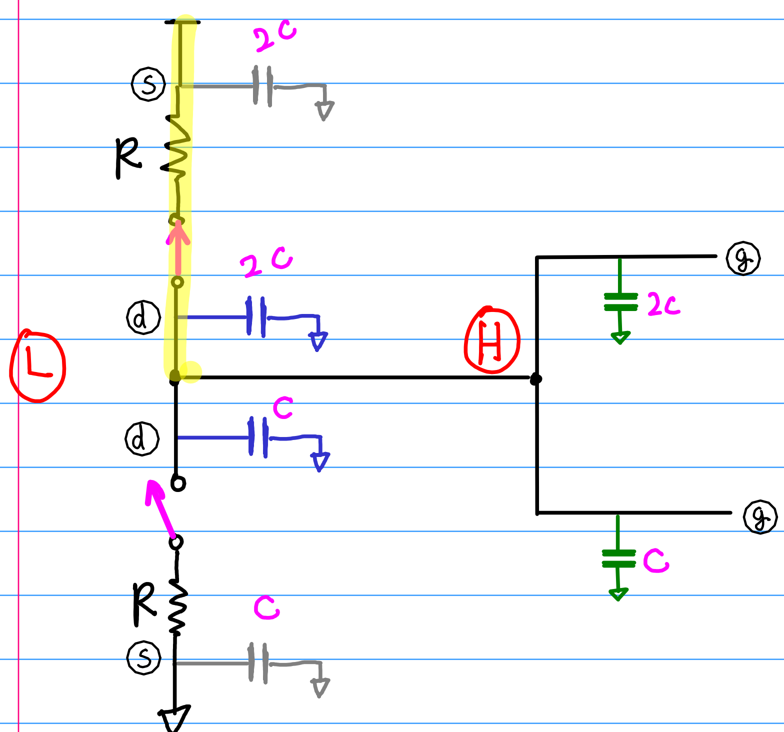


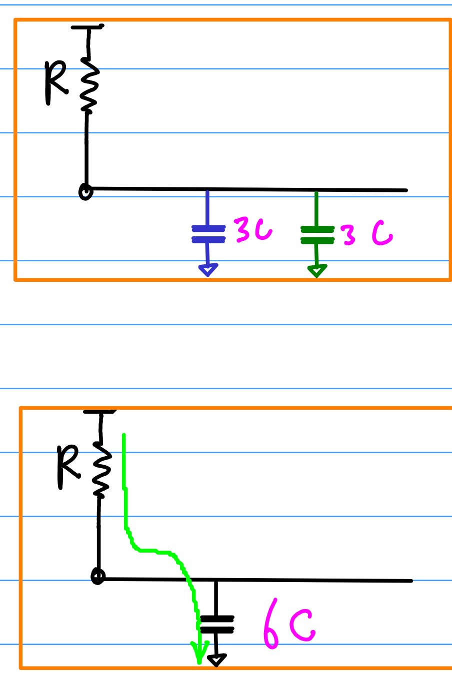
S
2C
g
2C
d
2C
d
C
g
C
S
C
S
2C
g
2C
d
2C
d
C
g
C
S
C



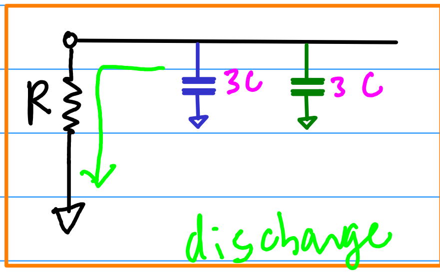


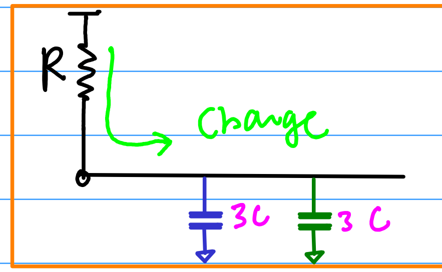
discharge



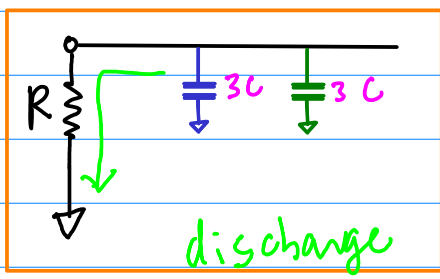


charge

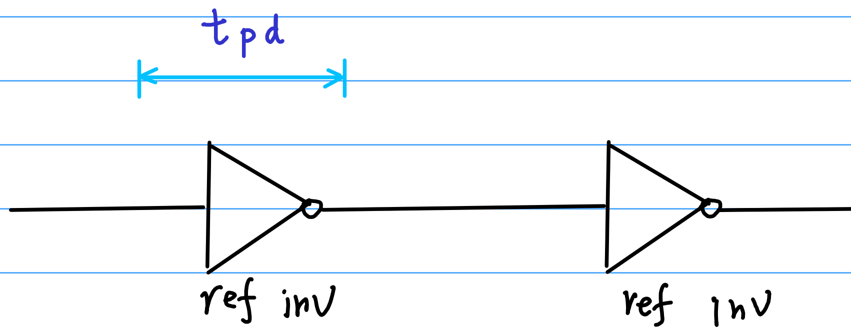


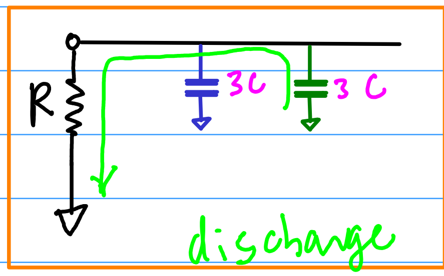


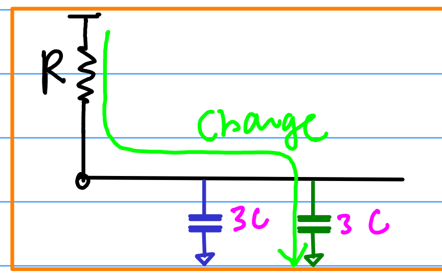
redundant



consider this only

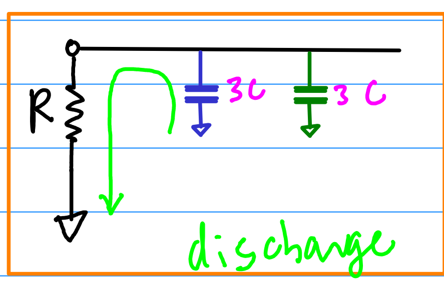


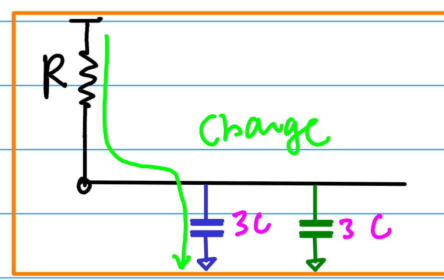




$\tau = 3RC$

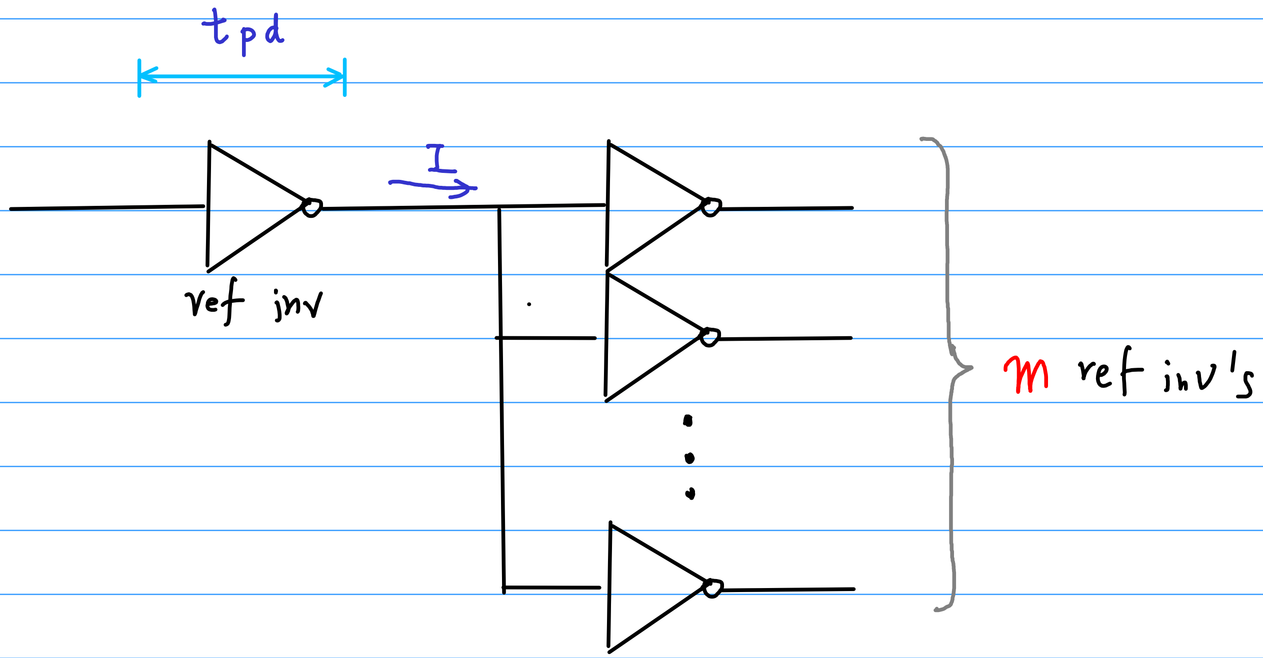
$\tau = 3RC$

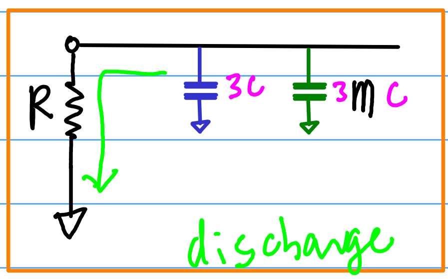


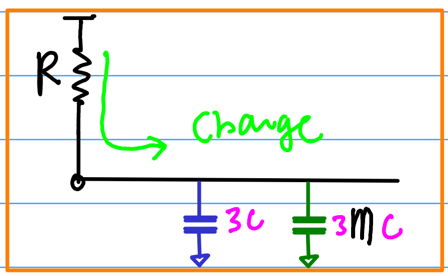


$\tau_{par} = 3RC$

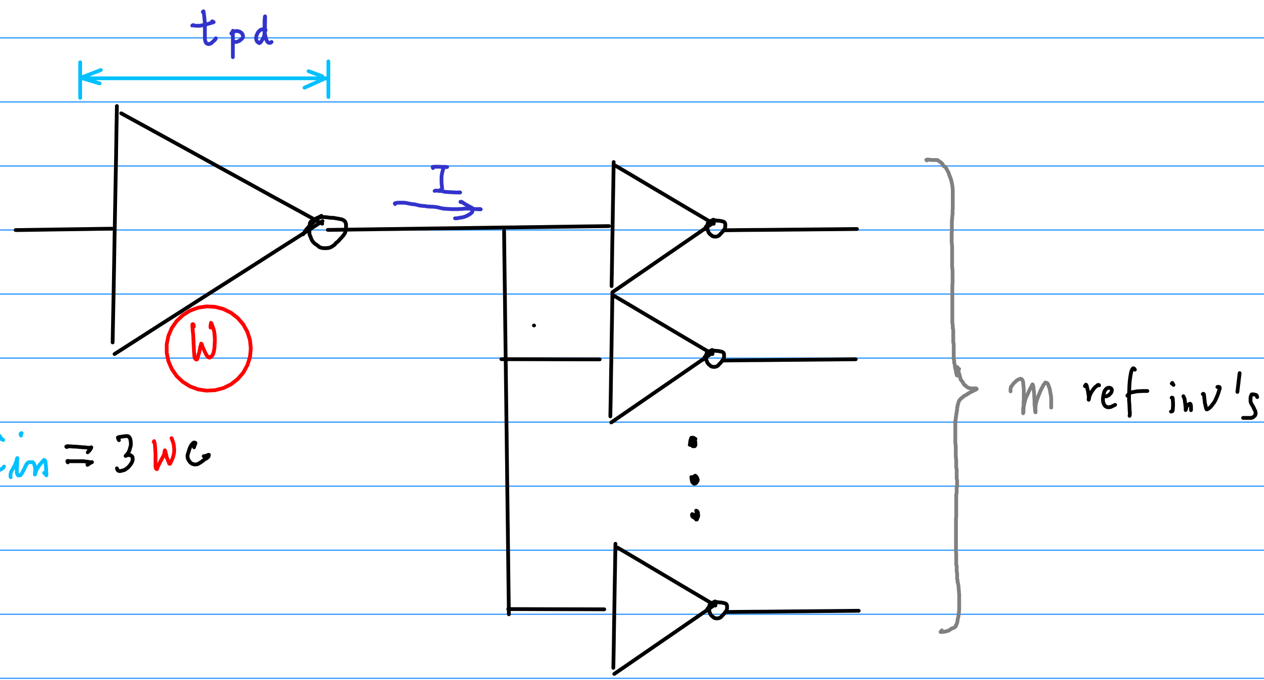
$\tau_{par} = 3RC$



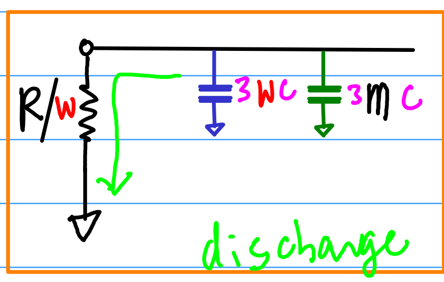


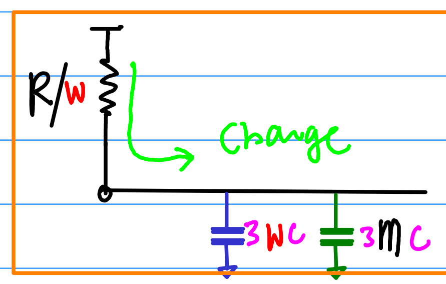


$$
\begin{aligned}
t_{pd} &= (R)(3C + 3mC) \\
&= (3+3m)RC \\
&= 3RC(1+m) \\
&= \tau(1+m)
\end{aligned}
$$



$C_{in} = 3WC$

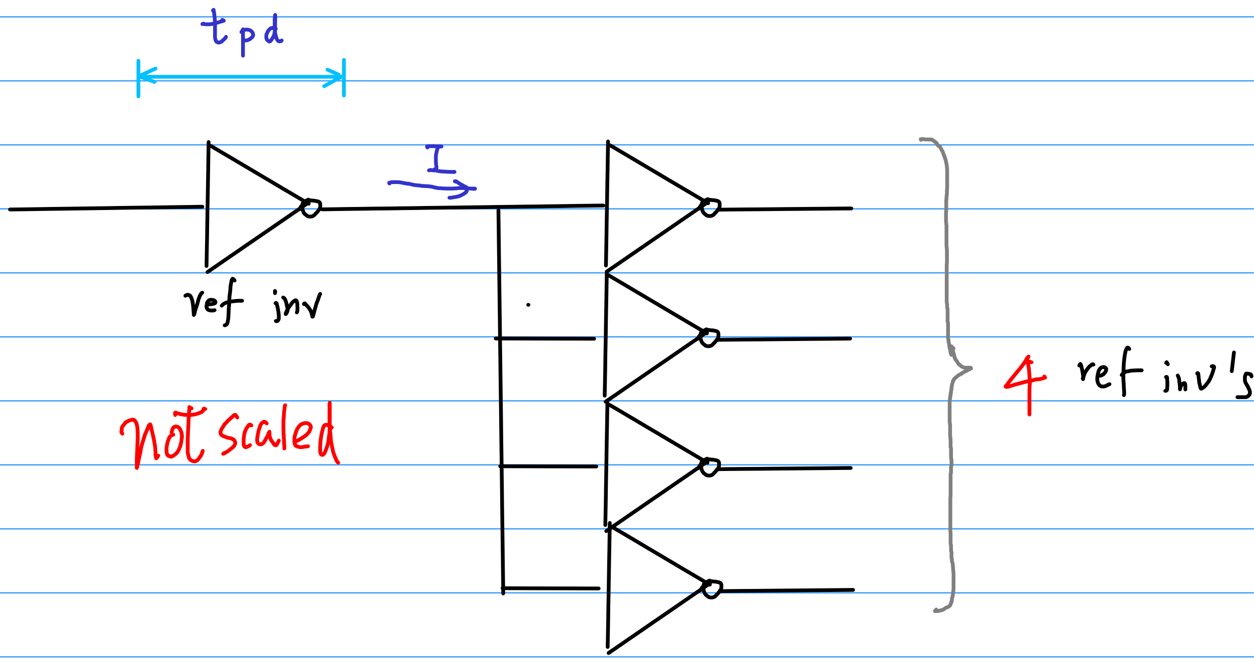


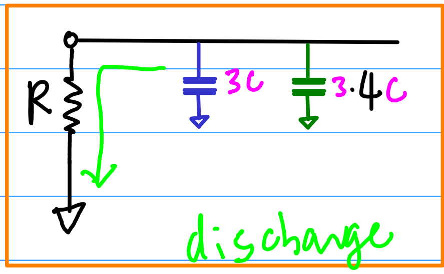


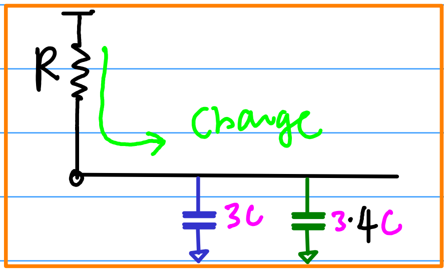
$$
\begin{aligned}
t_{pd} &= (R/W)(3WC + 3mC) \\
&= R\left(3C + 3C\frac{m}{W}\right) \\
&= RC(3 + 3h) \\
&= 3RC(1 + h) \\
&= \tau(1 + h)
\end{aligned}
$$

$$\frac{m}{W} = h = \frac{3mC}{3WC}$$

FO4 Inverter







$$t_{pd} = (R)(3C + 3\cdot 4C)$$
$$= (3 + 3\cdot 4)RC$$
$$= 3RC(1 + 4)$$
$$= \tau(1 + 4)$$

$h = 4$

absolute delay

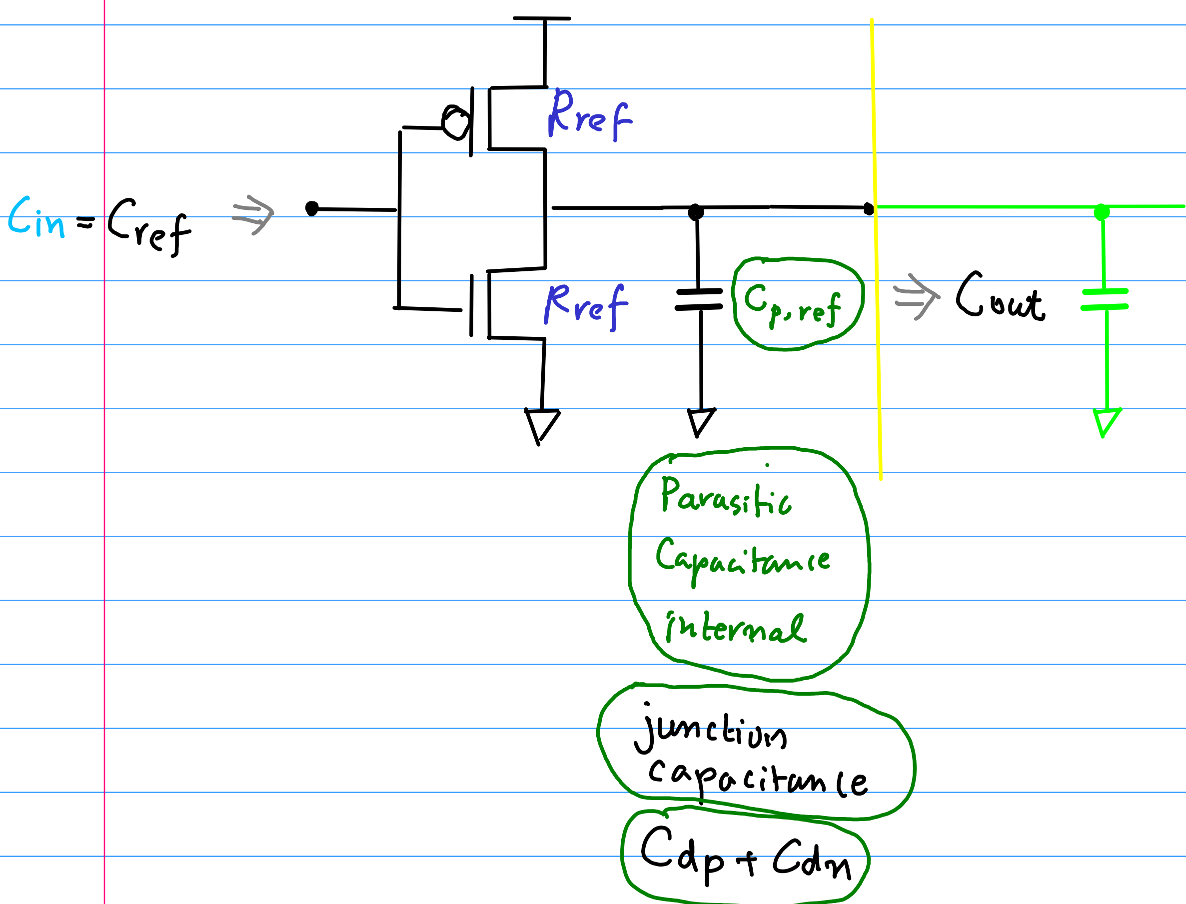
R C

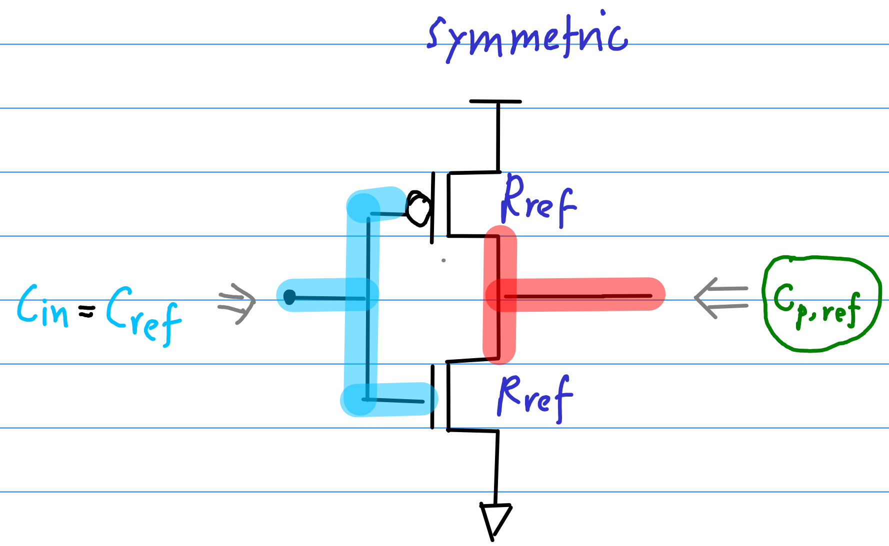
$$d_{abs} = k \cdot R_{ref} \cdot (C_{p,ref} + C_{out})$$

$R \cdot C$

$$k = \ln(9) = 2.2$$

Symmetric Inverter





$$\tau_{par} = k R_{ref} C_{p,ref}$$ parasitic time const.

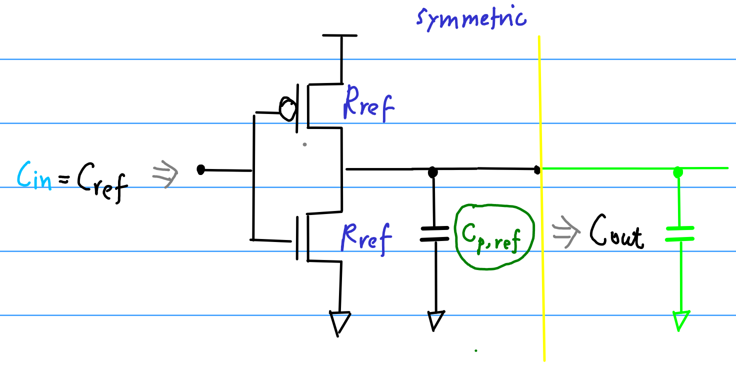
$$\tau = k R_{ref} C_{ref}$$ reference time const.

Scaling Factor $S > 1$

$$R = \frac{R_{ref}}{S}$$

$$C_p = S \cdot C_{p,ref}$$

$$C_{in} = S\, C_{ref}$$



$$d_{abs} = k\, R_{ref} \cdot (C_{p,ref} + C_{out})$$

after scaling $\Longrightarrow k \frac{R_{ref}}{S} (S \cdot C_{p,ref} + C_{out})$

$$= k R_{ref} C_{p,ref} + k \frac{R_{ref}}{S} C_{out}$$

$C_{in} = C_{ref}$

$$= k R_{ref} C_{p,ref} + k \frac{R_{ref}}{S} \left(\frac{C_{out}}{C_{ref}}\right) C_{ref}$$

$$= k R_{ref} C_{p,ref} + k R_{ref} \left(\frac{C_{out}}{C_{in}}\right) C_{ref}$$

$$= k R_{ref} C_{ref} \left(\frac{C_{p,ref}}{C_{ref}}\right) + k R_{ref} C_{ref} \left(\frac{C_{out}}{C_{in}}\right)$$

$$d_{abs} = k R_{ref} C_{ref} \left(\frac{C_{p,ref}}{C_{ref}} \right) + k R_{ref} C_{ref} \left(\frac{C_{out}}{C_{in}} \right)$$

$$= k R_{ref} C_{ref} \left[\frac{(k R_{ref})(C_{p,ref})}{(k R_{ref})(C_{ref})} + \left(\frac{C_{out}}{C_{in}} \right) \right]$$

$$= \tau \left[\left(\frac{\tau_{par}}{\tau} \right) + \left(\frac{C_{out}}{C_{in}} \right) \right]$$

$$= \tau \left[p + h \right]$$

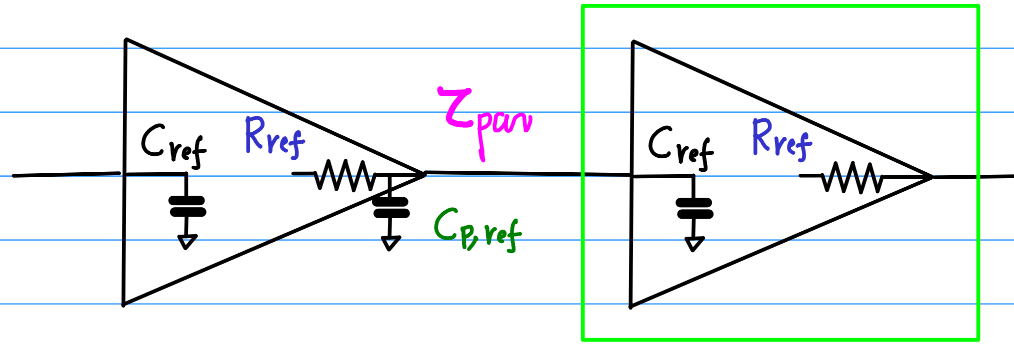
$$= \tau \cdot d$$

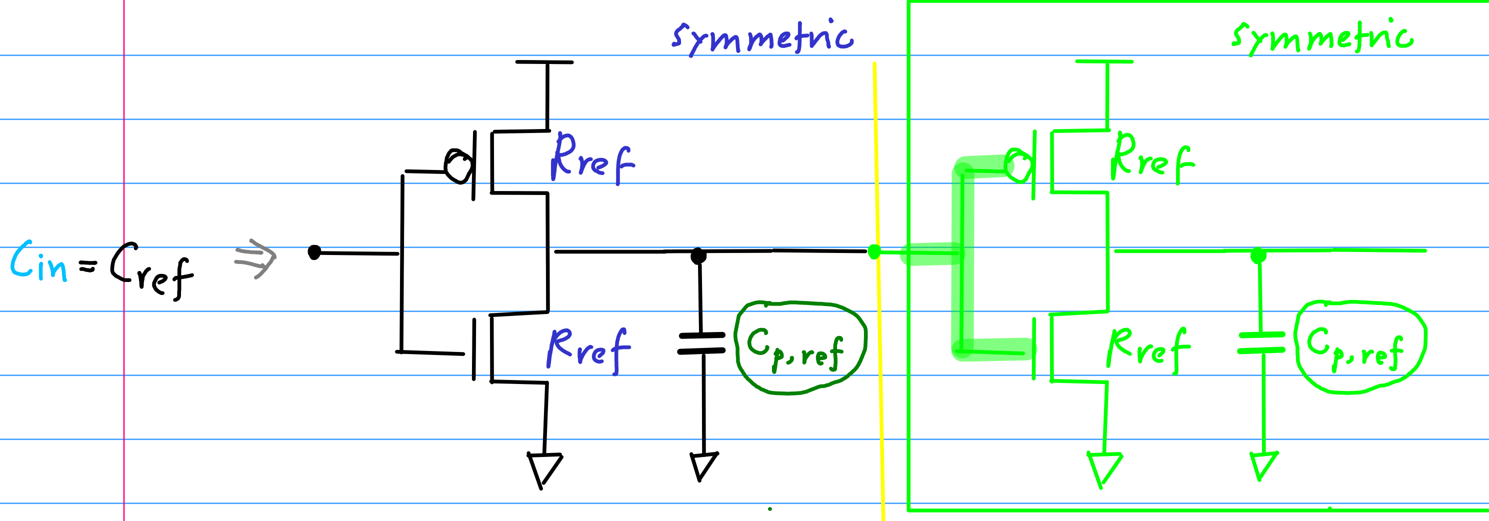
$$\boxed{\tau_{par} = k R_{ref} C_{p,ref}}$$ parasitic time const.

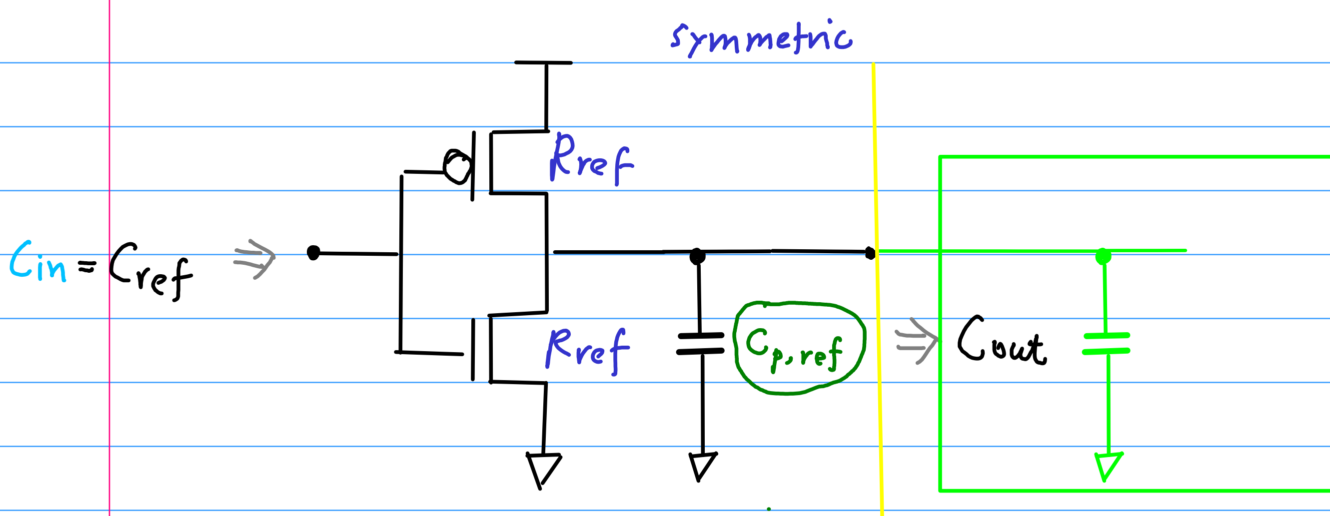
$$\boxed{\tau = k R_{ref} C_{ref}}$$ reference time const.

$$\tau_{par} = \tau \cdot p$$

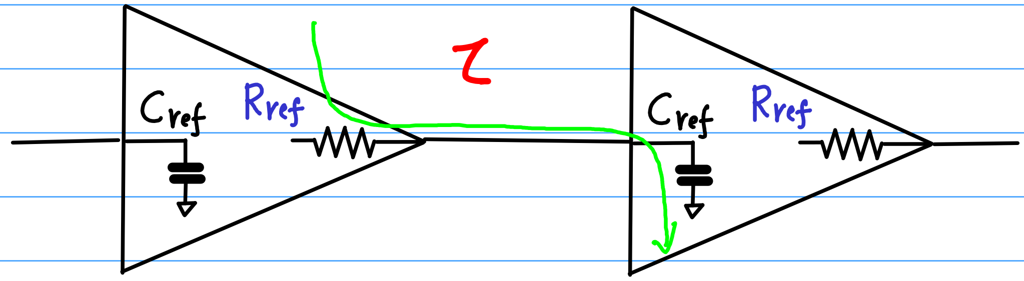
$$d_{abs} = \tau \cdot d$$


Cref
Rref
τpar
Cp,ref
Cref
Rref

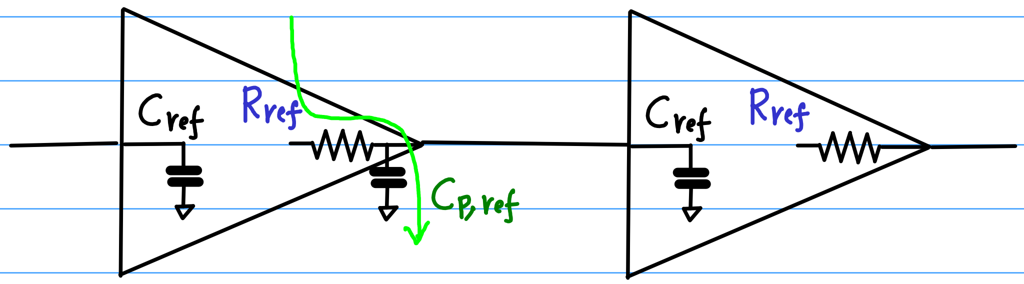

Symmetric
Symmetric
Rref
Rref
Cin = Cref
Rref
Cp,ref
Rref
Cp,ref

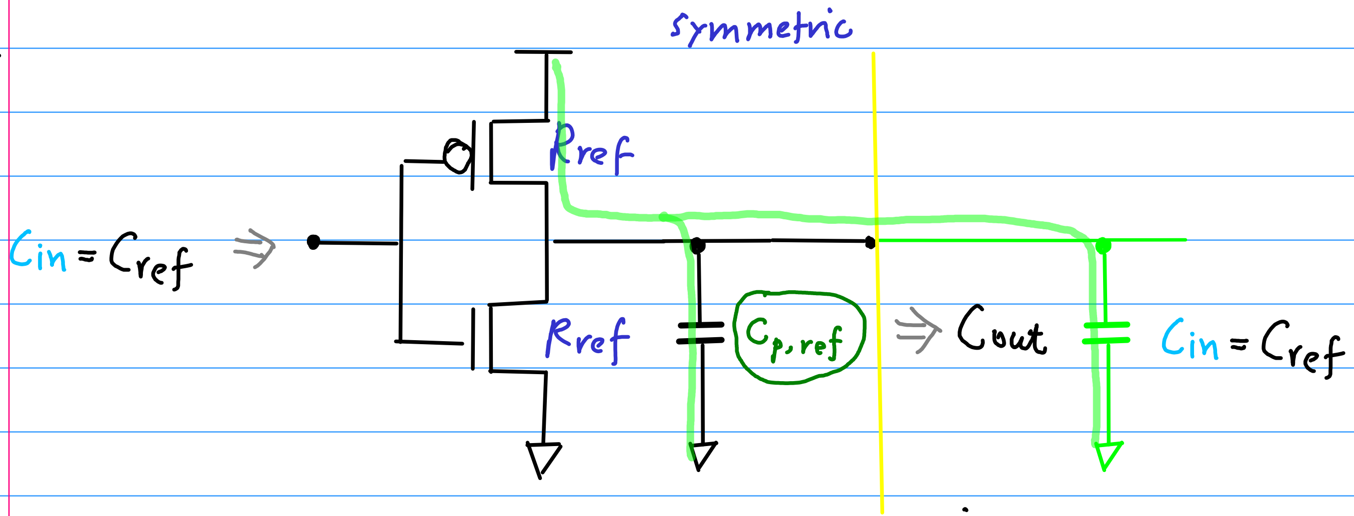

Symmetric
Rref
Cin = Cref
Rref
Cp,ref
Cout

$\tau = k R_{ref} C_{ref}$ reference time const.



$\tau_{par} = k R_{ref} C_{p,ref}$ parasitic time const.





τ: reference time const. $\tau = k R_{ref} C_{ref}$

τ_{par}: parasitic time const. $\tau_{par} = k R_{ref} C_{p,ref}$

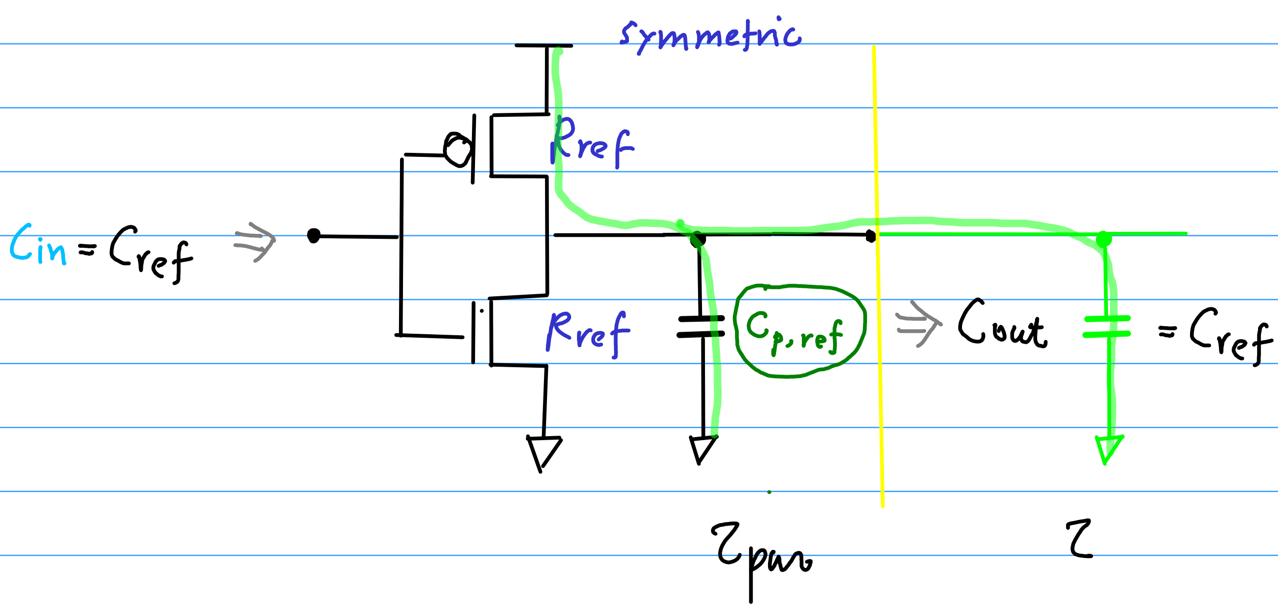
Parasitic Capacitance internal	junction capacitance $C_{dp} + C_{dn}$

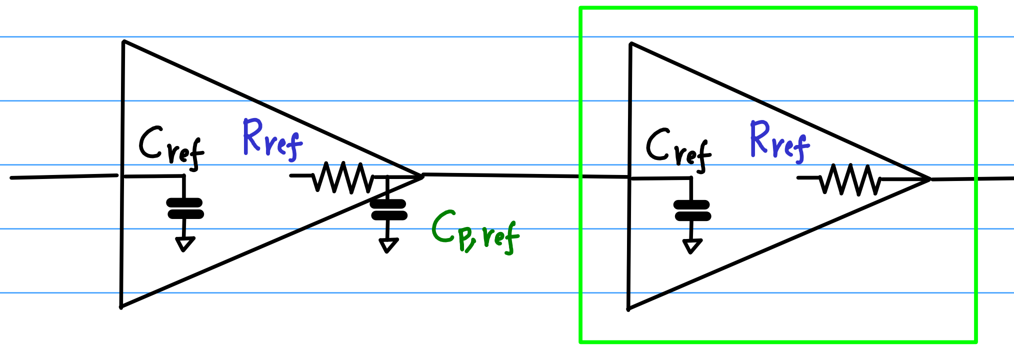
Electrical Effort

$$h = \frac{C_{out}}{C_{in}}$$

Parasitic Delay

$$p = \frac{\tau_{par}}{\tau} = \left(\frac{k R_{ref}\, C_{p,ref}}{k R_{ref}\, C_{ref}}\right) = \left(\frac{C_{p,ref}}{C_{ref}}\right)$$

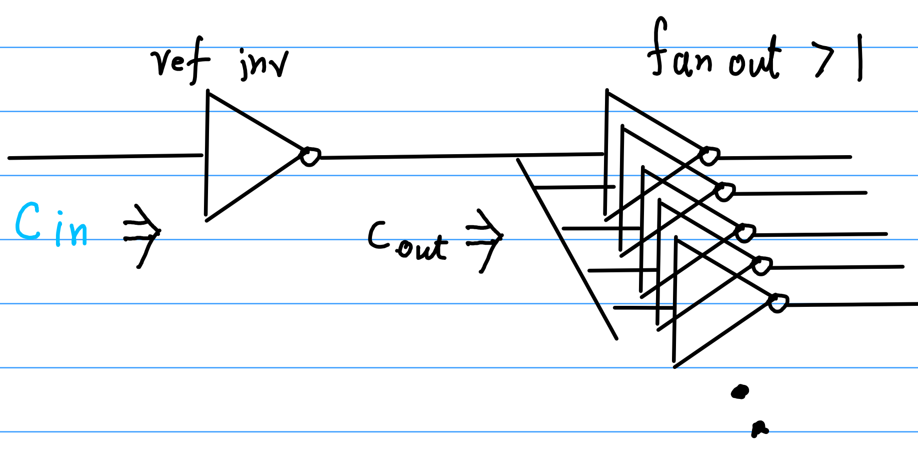




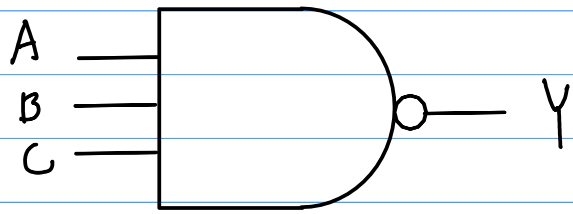
$$p = \frac{\tau_{par}}{\tau} = \left(\frac{k R_{ref}\; C_{p,ref}}{k R_{ref}\; C_{ref}}\right) = \left(\frac{C_{p,ref}}{C_{ref}}\right)$$

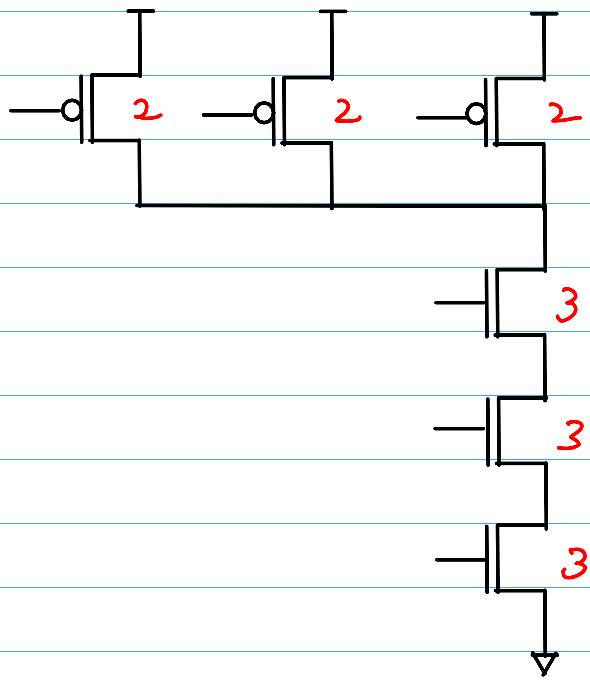
fixed for an inverter

$$h = \frac{C_{out}}{C_{in}}$$



3-input NAND Delay





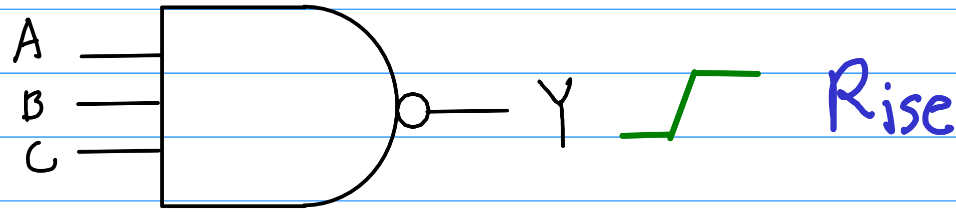
{ ① propagation delay

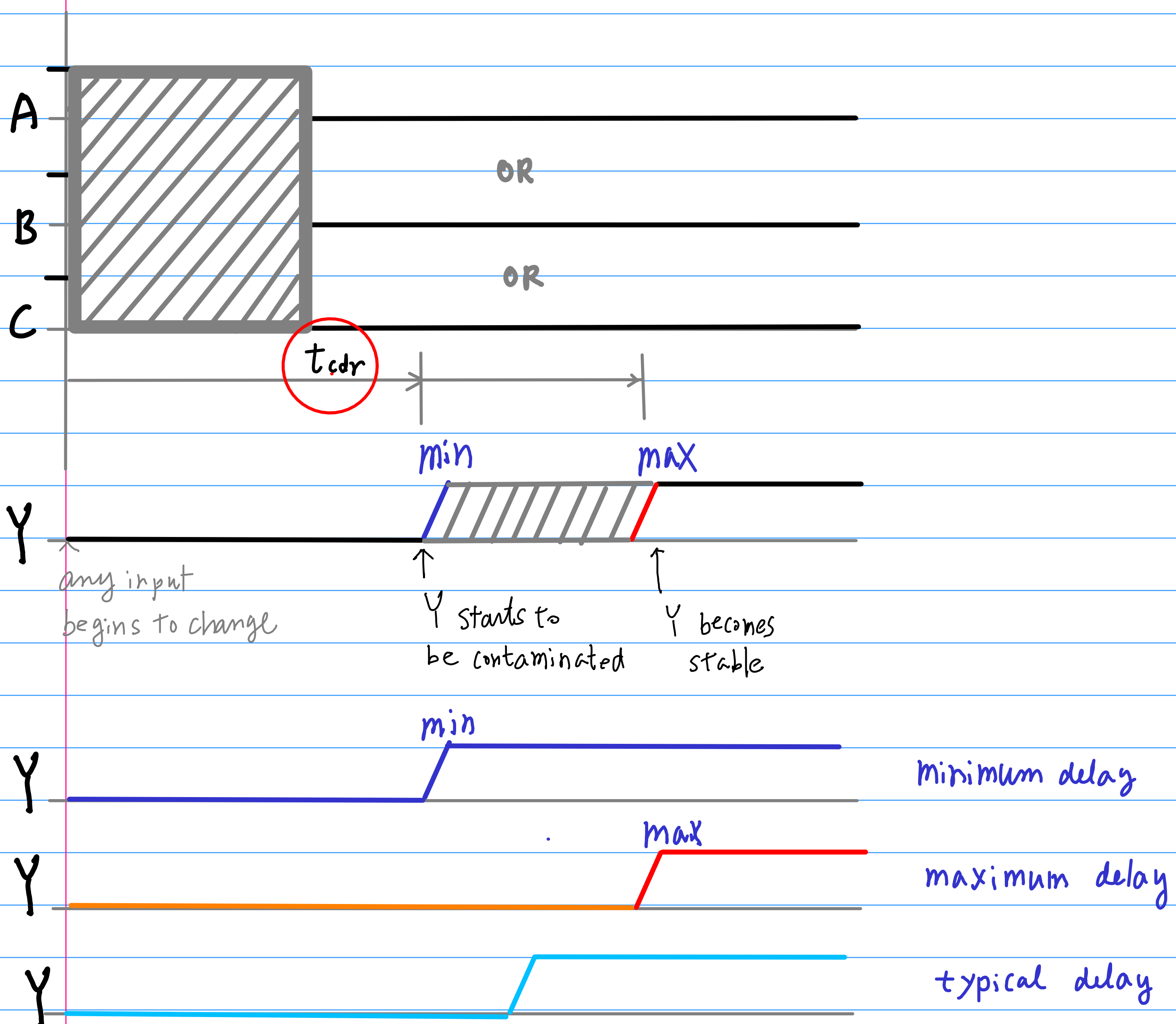
② contamination delay

Rise Delay

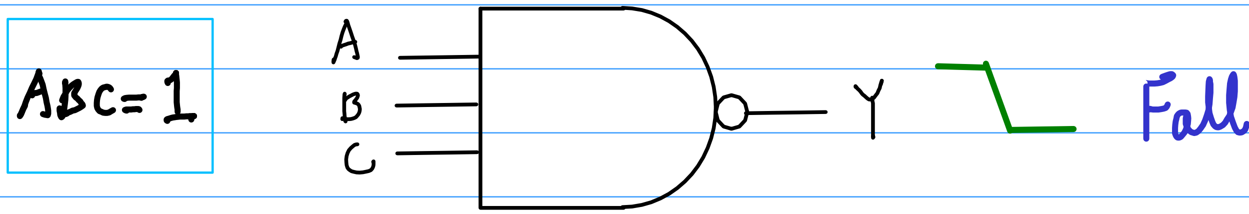
$\overline{ABC} = 1$

$(\bar{A}+\bar{B}+\bar{C}) = 1$

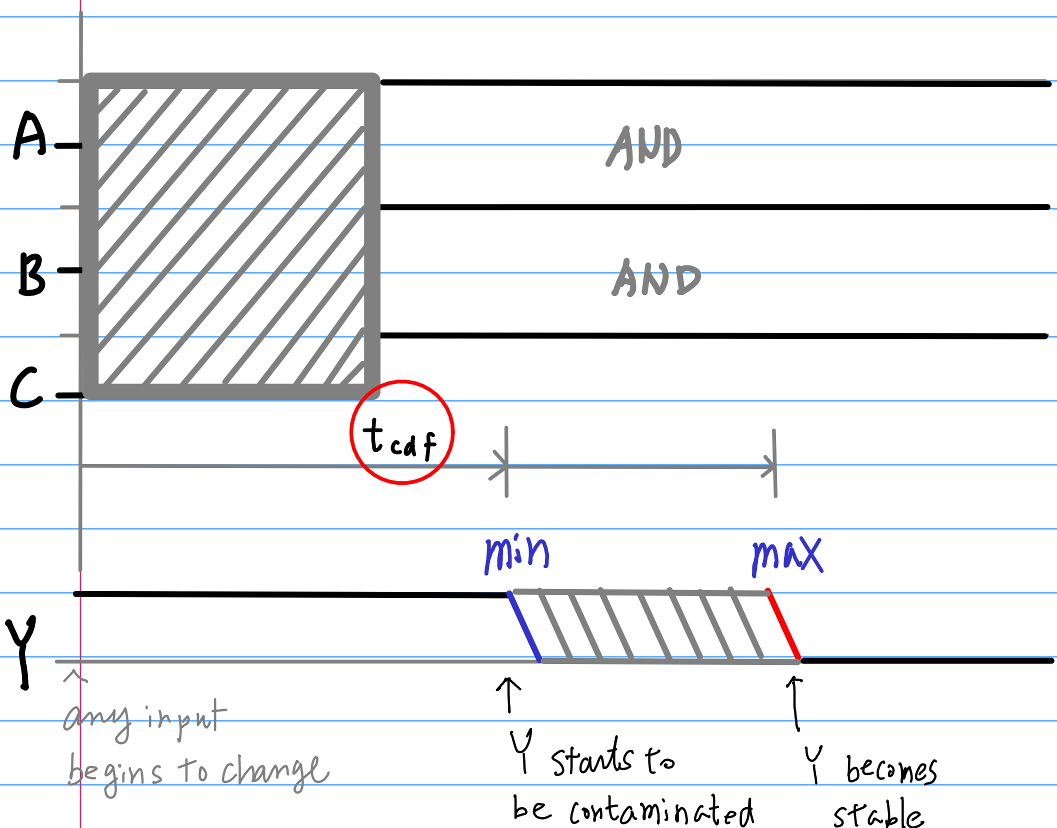




Fall Delay



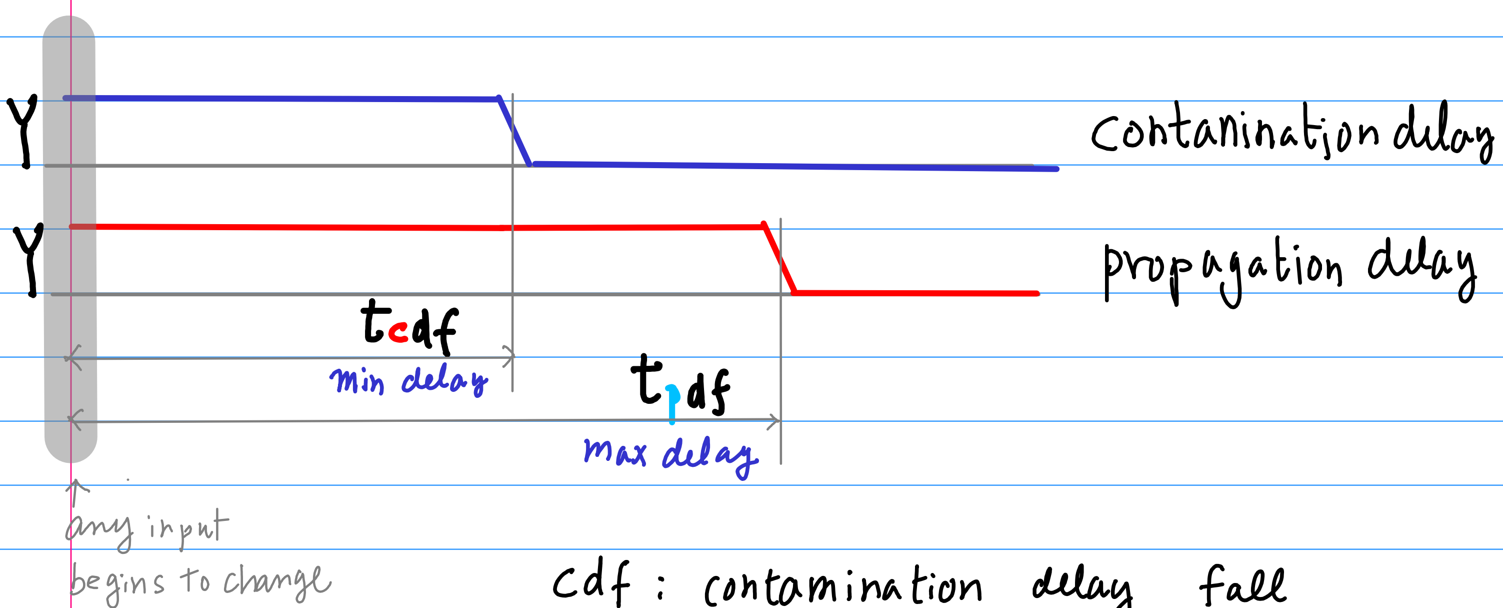
ABC=1
A
B
C
Y
Fall



A
B
C
AND
AND
t_{cdf}
min
max
Y
any input
begins to change
Y starts to
be contaminated
Y becomes
stable

min
Y
minimum delay
max
Y
maximum delay
Y
typical delay

cdr : contamination delay rise
pdr : propagation delay rise



cdf : contamination delay fall
pdf : propagation delay fall

Contamination Delay

In digital circuits, the contamination delay (denoted as tcd) is the minimum amount of time from when an input changes until any output starts to change its value.

This change in value does not imply that the value has reached a stable condition.

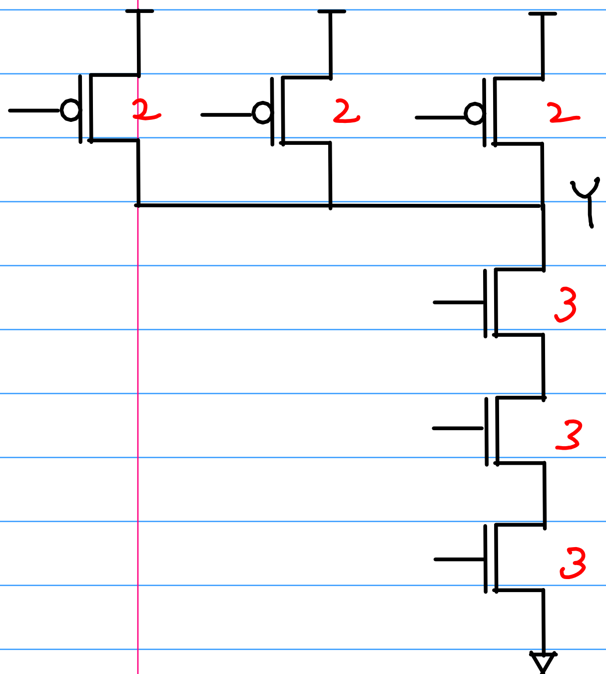
The contamination delay only specifies that the output rises (or falls) to 50% of the voltage level for a logic high.

The circuit is guaranteed
not to show any output change
in response to an input change
before tcd time units (calculated for the whole circuit) have passed.

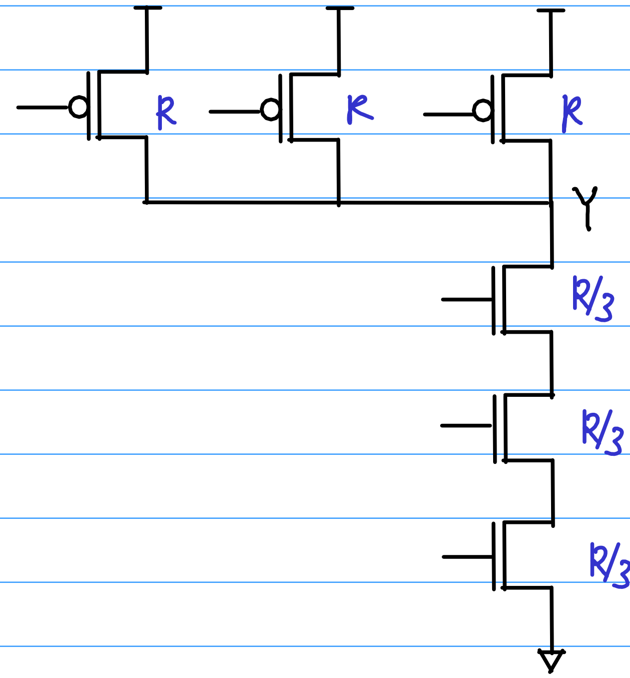
The determination of the contamination delay of a combined circuit requires identifying the shortest path of contamination delays
from input to output and by adding each tcd time along this path.

https://en.wikipedia.org/wiki/Contamination_delay

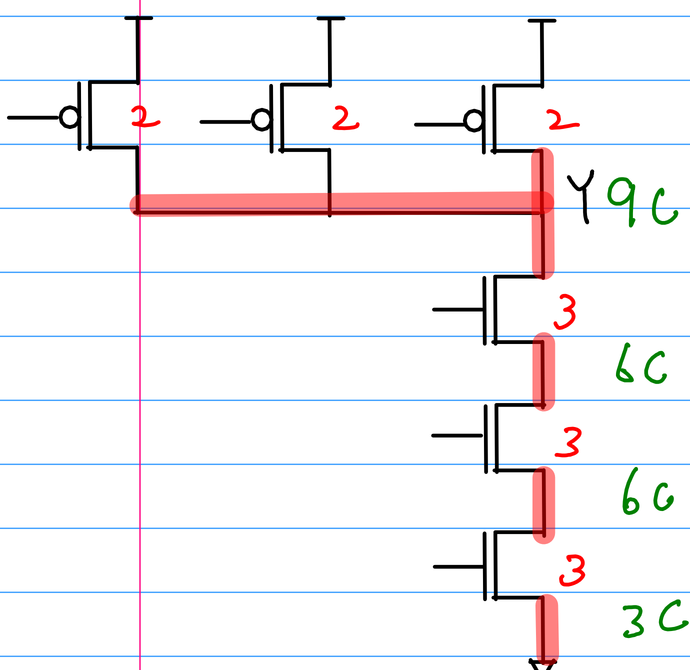
size info



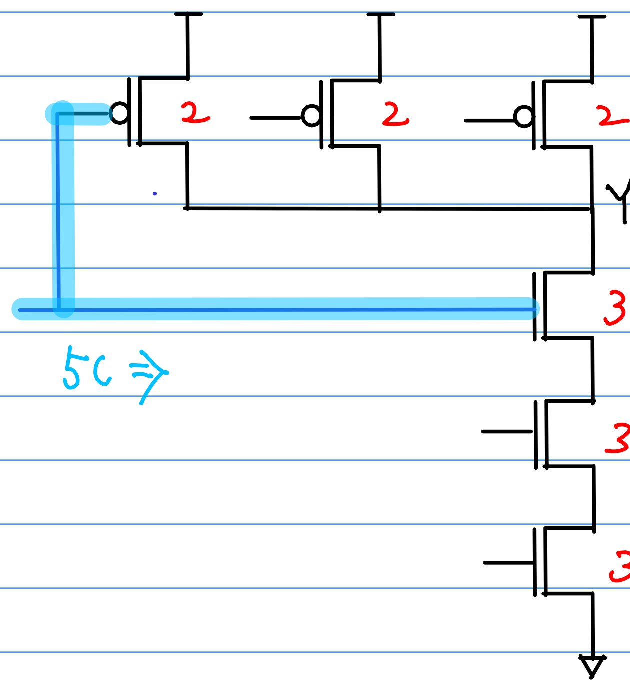
resistance



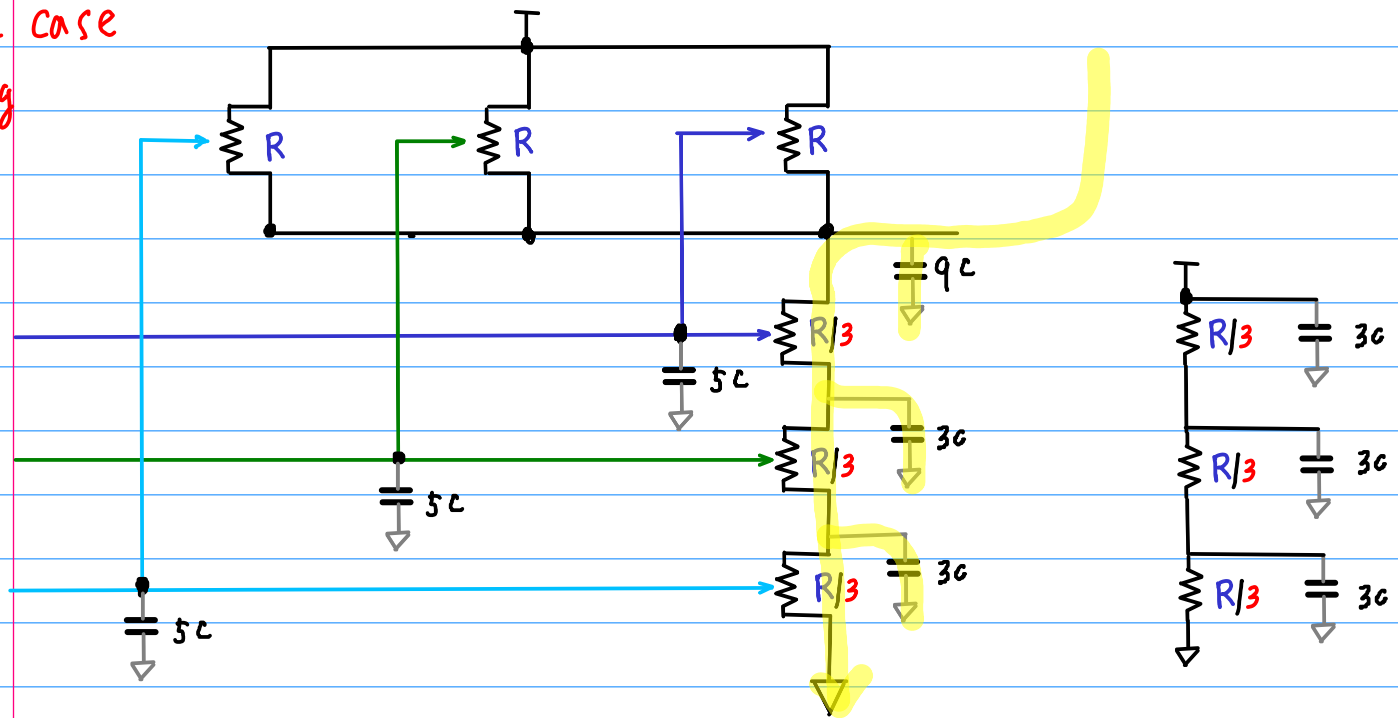
parasitic cap



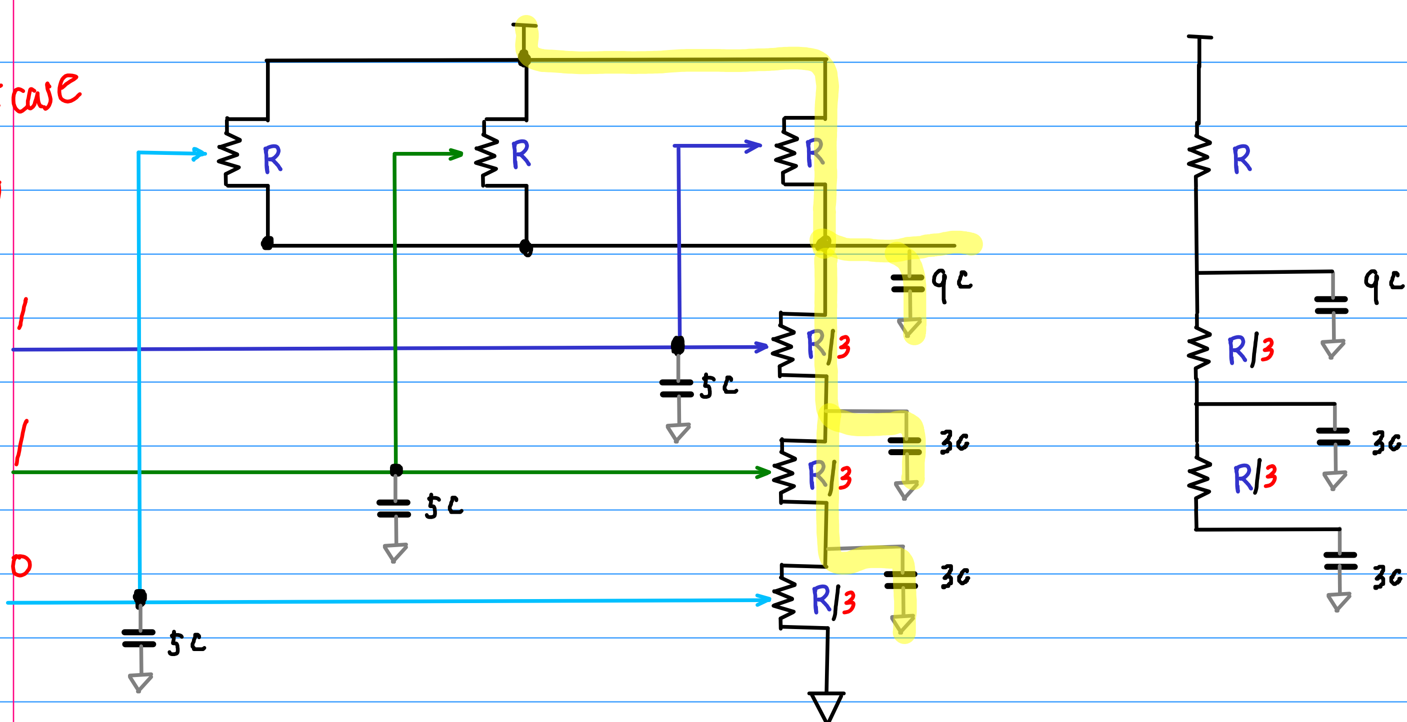
input cap



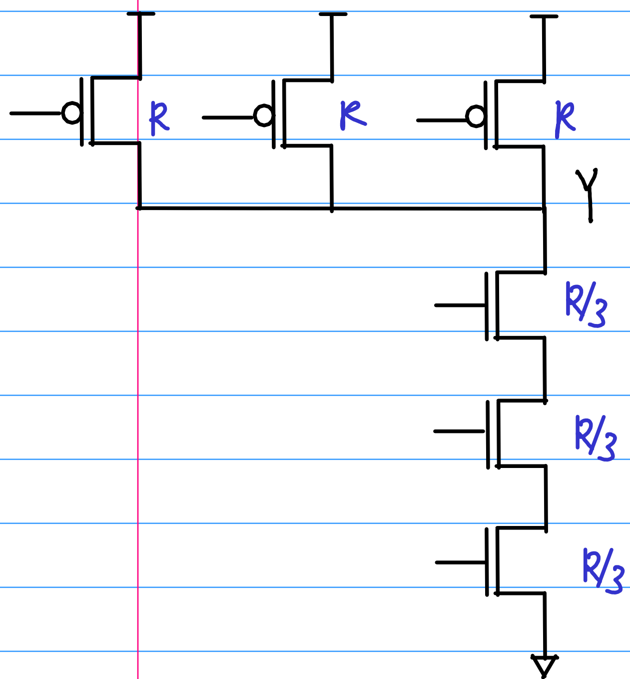
Worst case falling

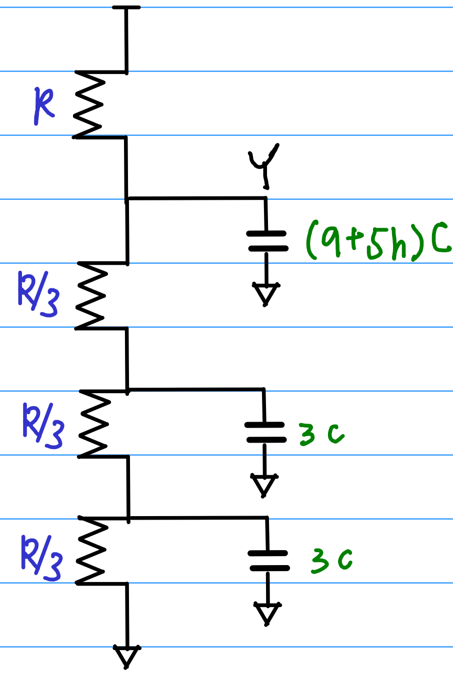


Worst case rising

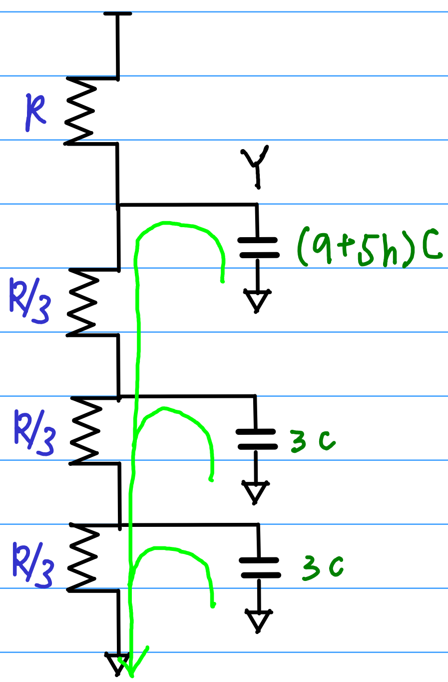


Equivalent RC circuit



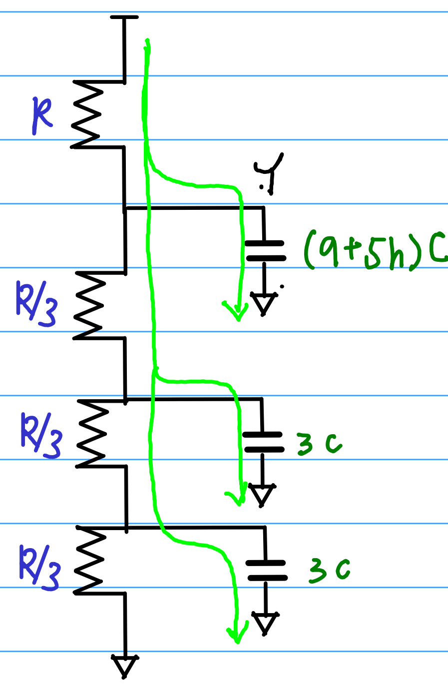


Fall Delay



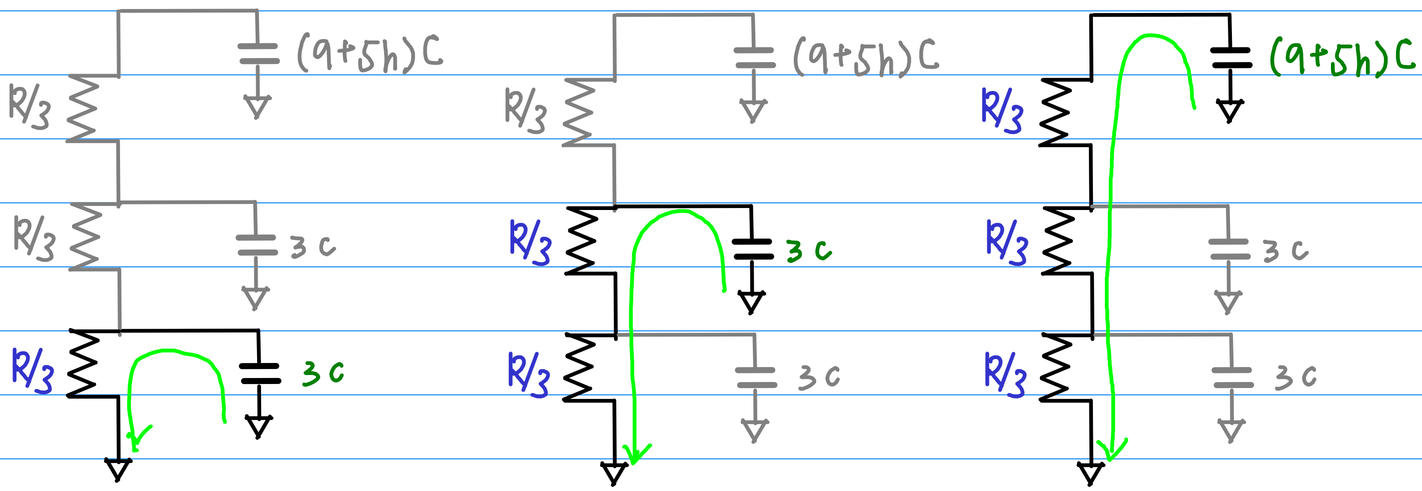
discharge

Rise Delay



charge

Fall Case – Elmore Delay



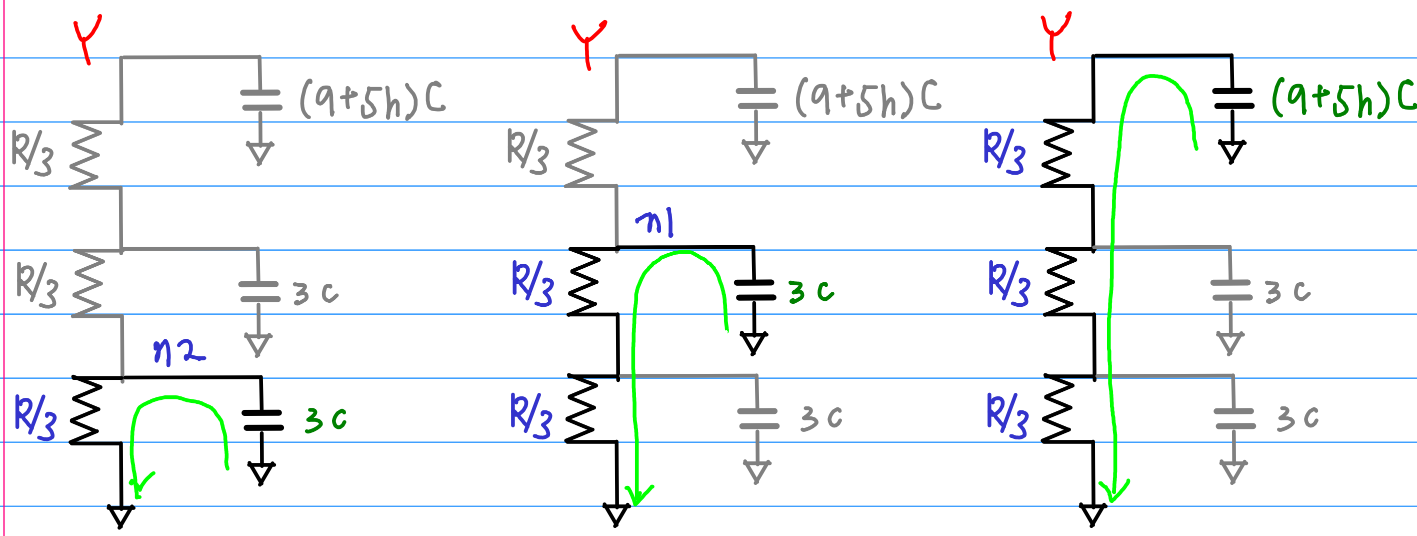
$(R/3)(3C) = RC$

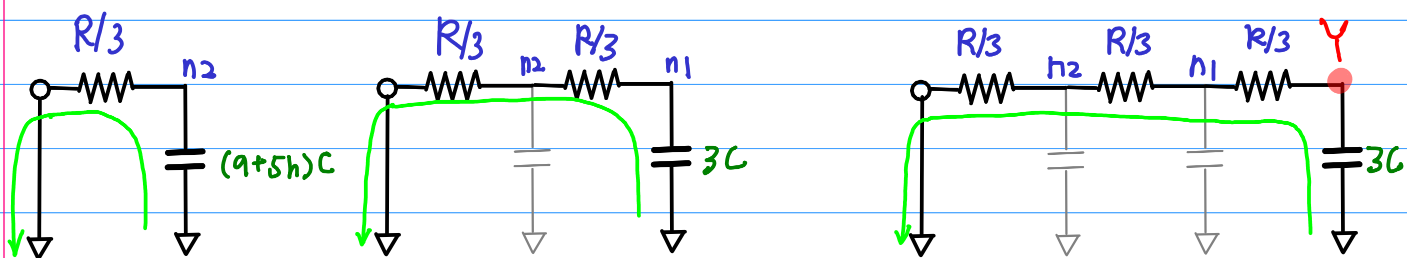
$(R/3 + R/3)(3C) = 2RC$

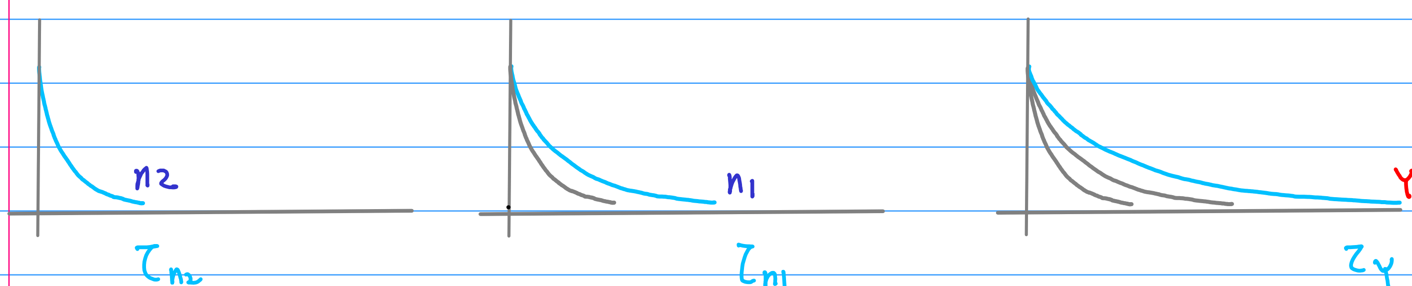
$(R/3 + R/3 + R/3)((9+5h)C) = (9+5h)RC$

$RC + 2RC + (9+5h)RC = (12+5h)RC$

Fall Case – Elmore Delay





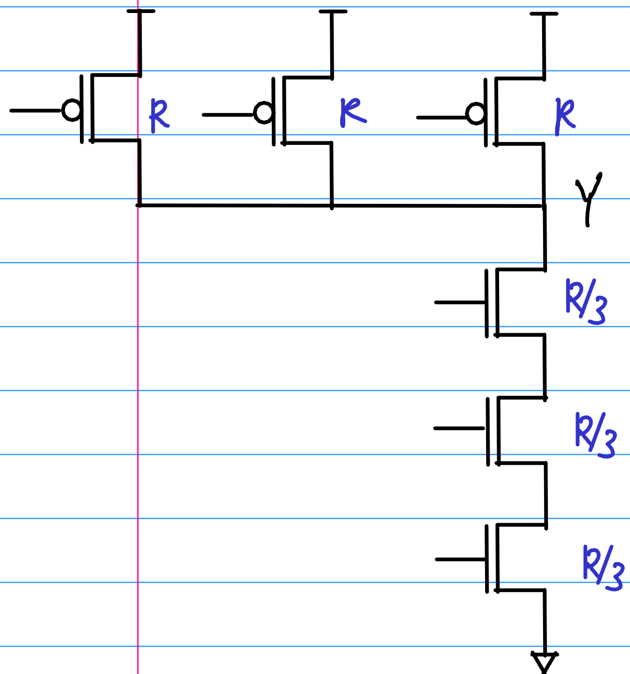


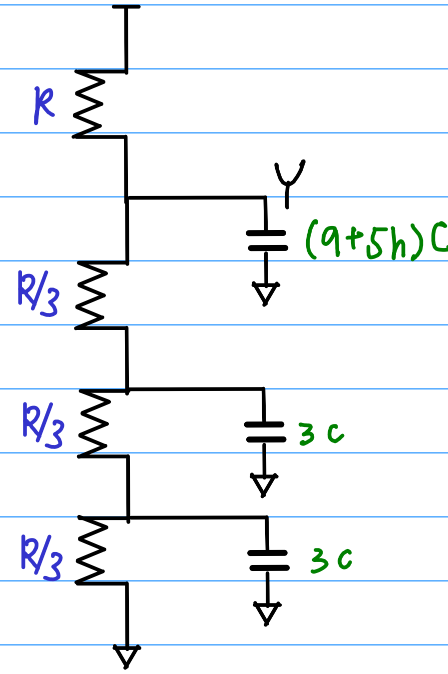
discharge first n2, then n1, finally Y

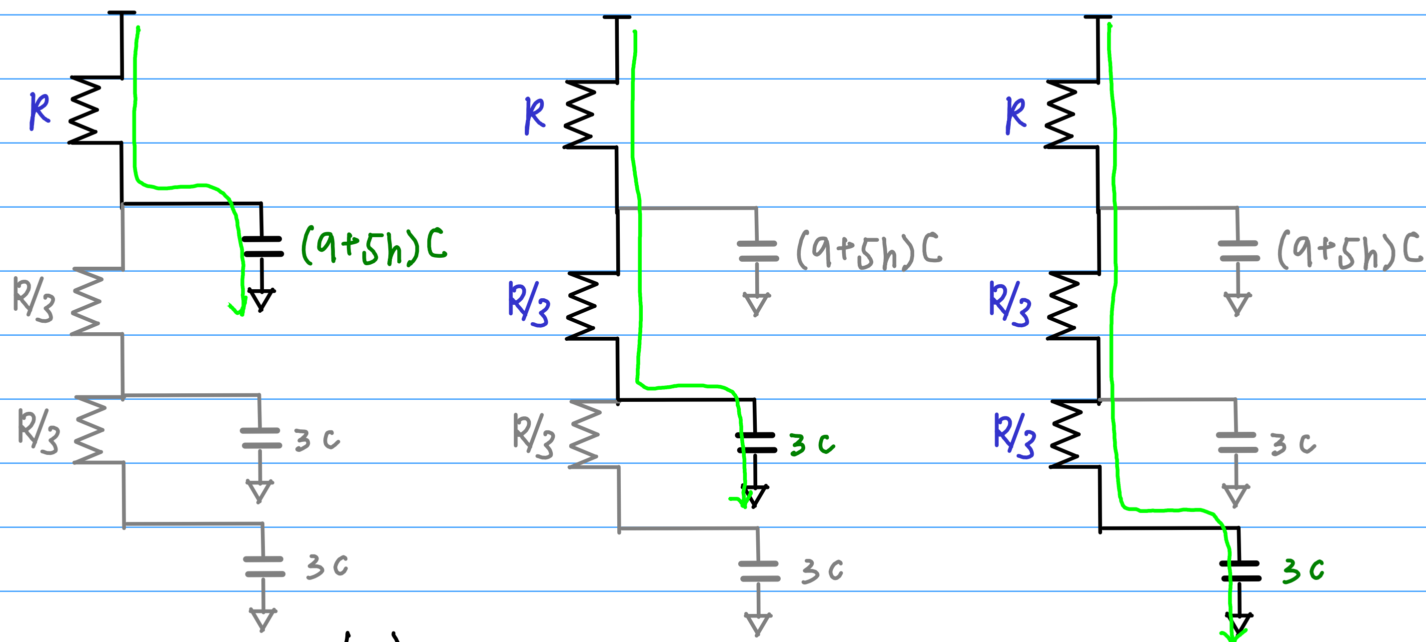
the discharging charge must be added

$$\tau = \tau_{n1} + \tau_{n2} + \tau_Y$$

Rise Case – Elmore Delay







(3c)

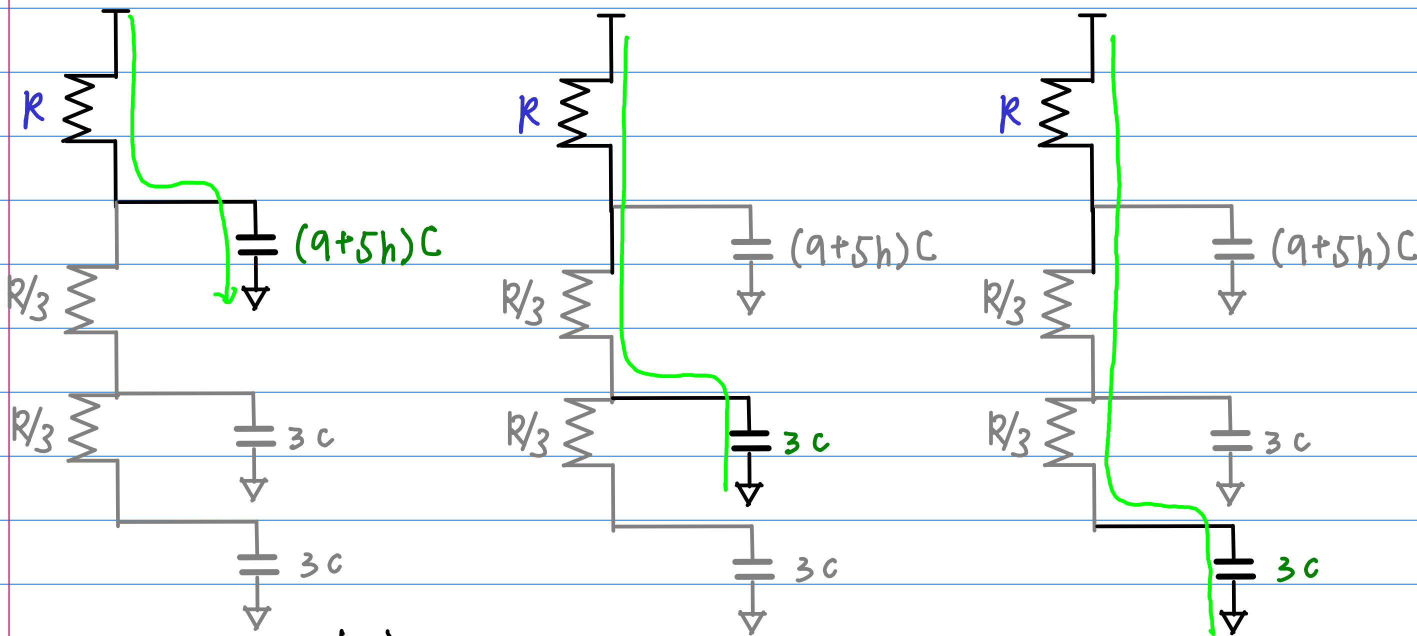
$(R)((9+5h)C)$ $= (9+5h)RC$

$(R + R/3)(3c)$ $= 4RC$

$(R + R/3 + R/3)(3c)$ $= 5RC$

$4RC + 5RC + (9+5h)RC = (18+5h)RC$

Rise Case – Elmore Delay



(3c)

$(R)((9+5h)C)$
$= (9+5h)RC$

$(R)(3c)$
$= 3RC$

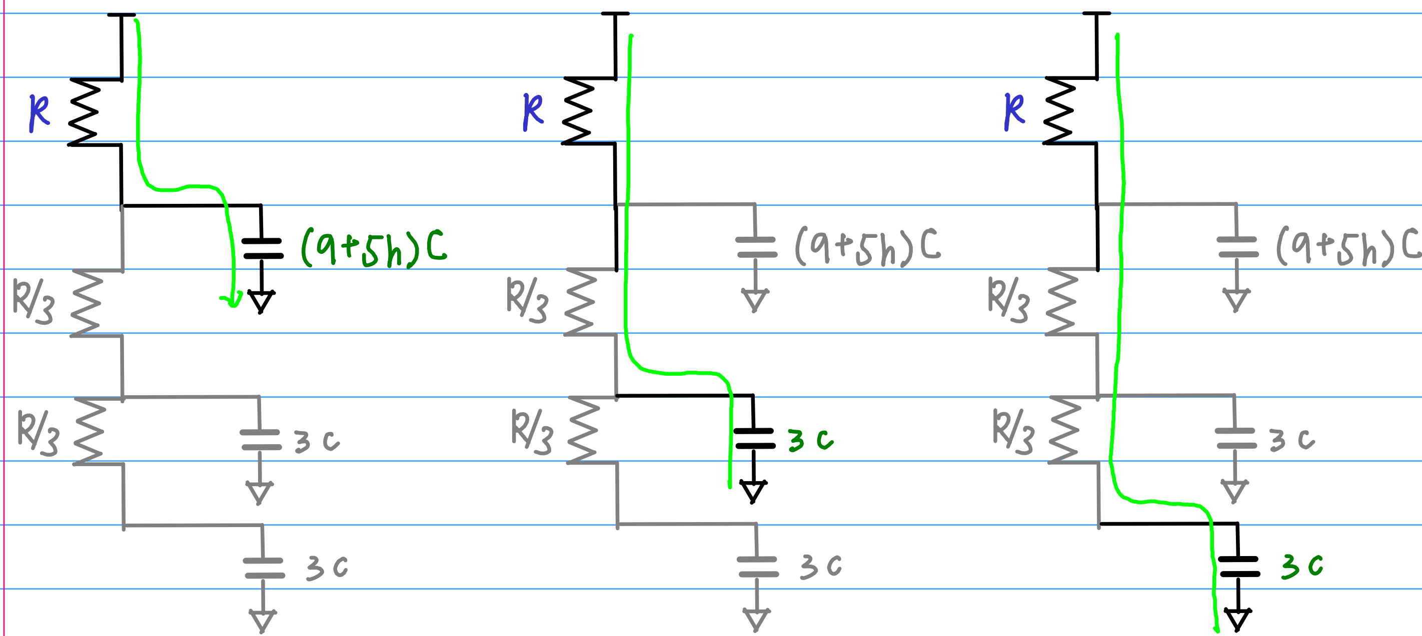
$(R)(3c)$
$= 3RC$

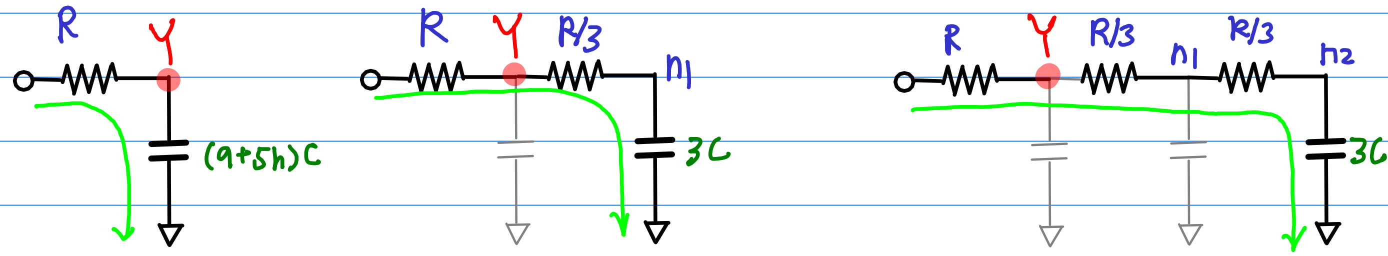
$(9+5h)RC + 3RC + 3RC = (15+5h)RC$

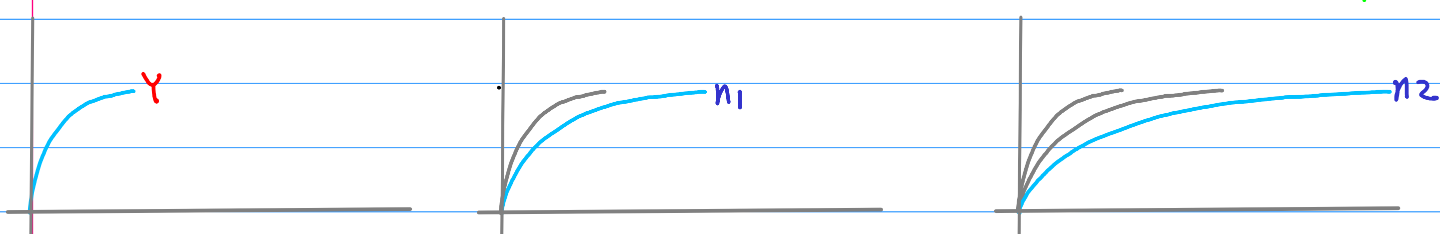
resistance on the shared path

Y is charged only through (R)
R/3 do not contribute!
shield the diffusion capacitance
don't have to charge all the way up before Y rises

Rise Case – Elmore Delay

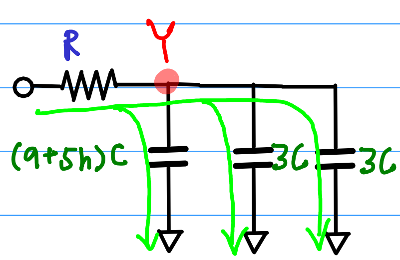






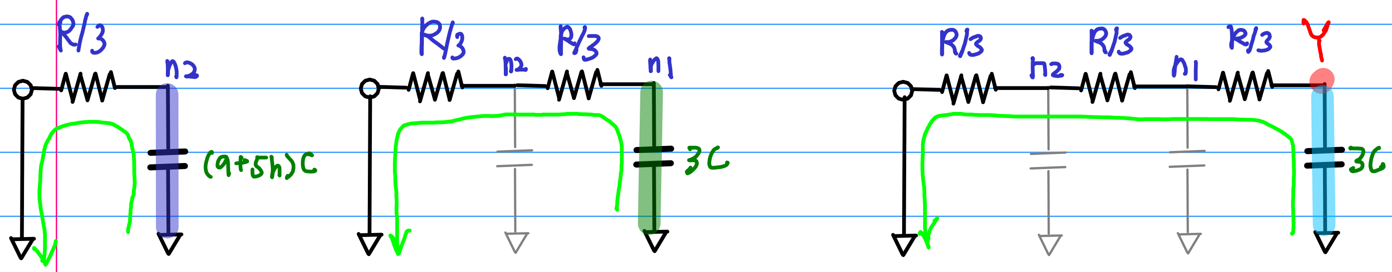
Charge Y then n_1 finally n_2

We concern the delay at Y only.

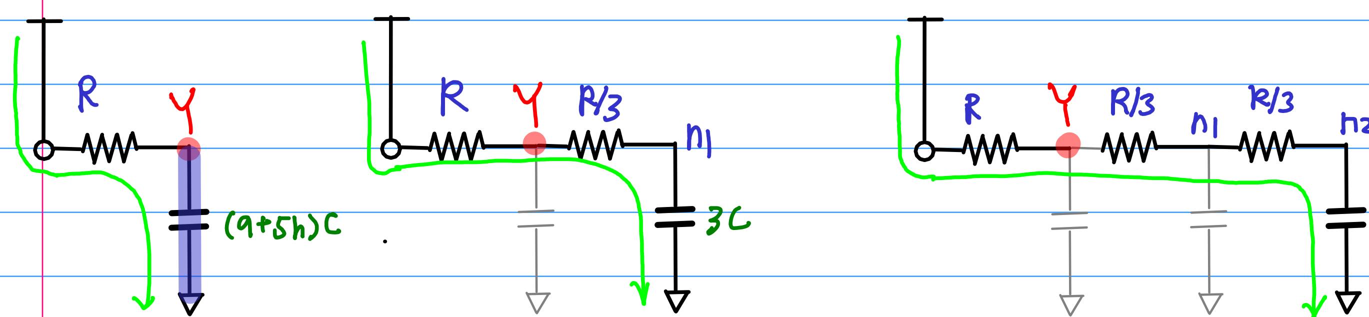


$$R\,(9+5h+3+3)\,C = (15+5h)\,RC$$

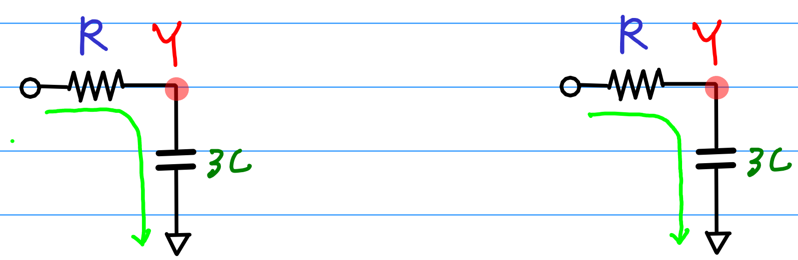
Ⓐ Fall Delay



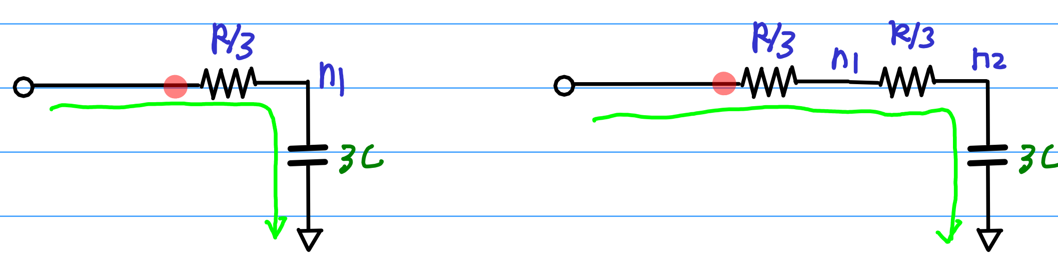
Ⓒ Rise Delay



$3(R + R/3)C$ $3(R + R/3 + R/3)C$

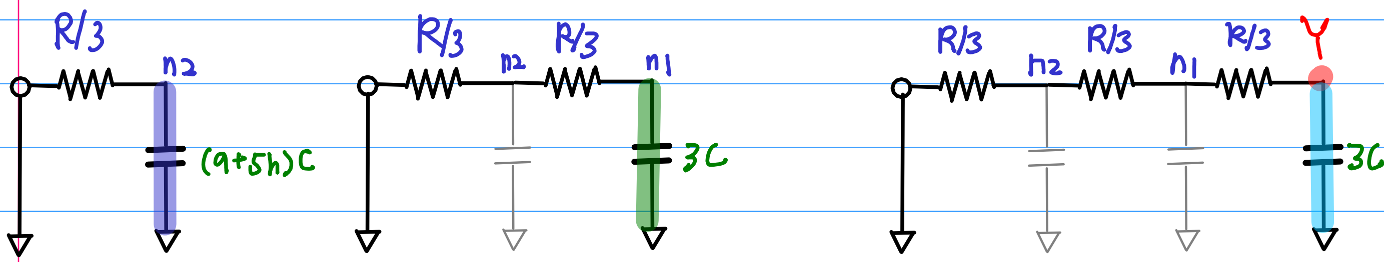


$3(R)C$ $3(R)C$



$3(R/3)C$ $3(R/3 + R/3)C$

(A) Fall Delay



Charge that must discharged

$V_{n2} \rightarrow 0$ &
$V_{n1} \rightarrow 0$ &
$V_Y \rightarrow 0$

all 3 conditions

τ_3 τ_2 τ_1

only this condition

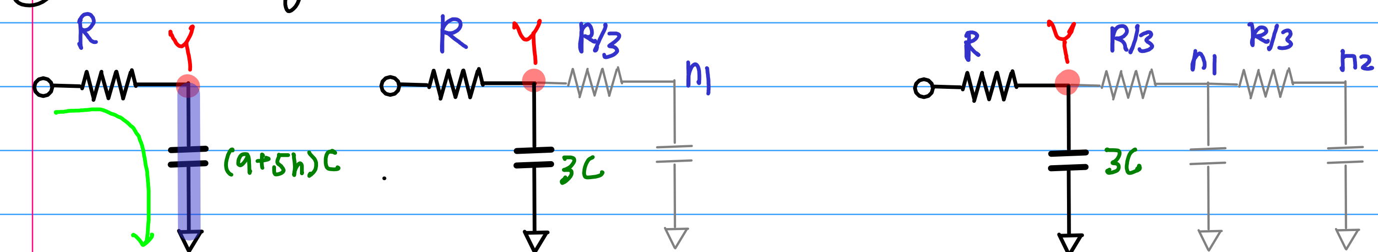
$V_Y \rightarrow V_{DD}$

$V_{n1} \rightarrow V_{DD}$

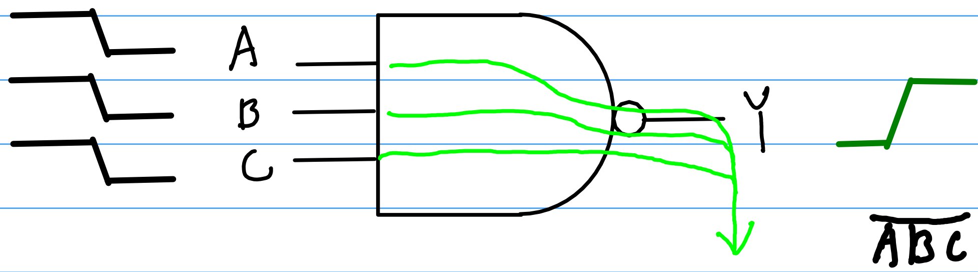
$V_{n2} \rightarrow V_{DD}$

τ_3 τ_2 τ_1

(C) Rise Delay



Input Transitions for a Minimum Delay



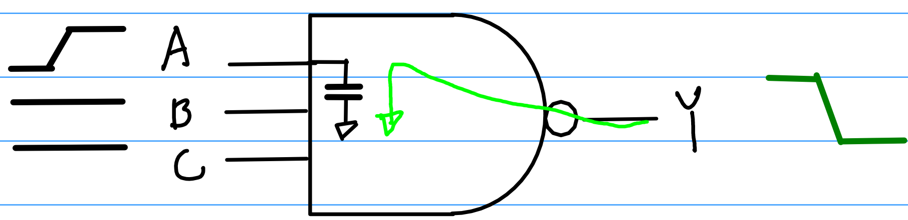
Rise

$\overline{ABC} = 1$

$(\bar{A}+\bar{B}+\bar{C}) = 1$

Simultaneous falling

3 current sources to charge C_L



Fall

$ABC = 1$

One input rising lately
other inputs already "H"

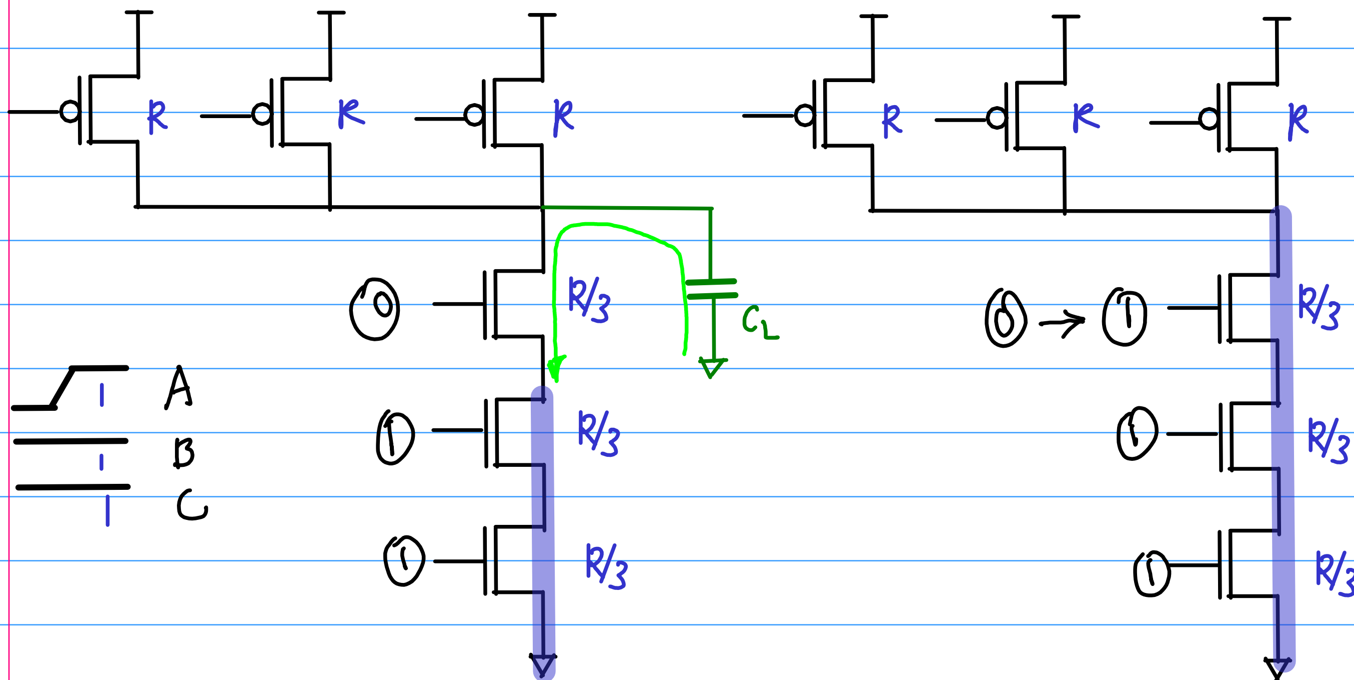
Only have to discharge the parasitic capacitance of one nMOS transistor

Smallest resistance.

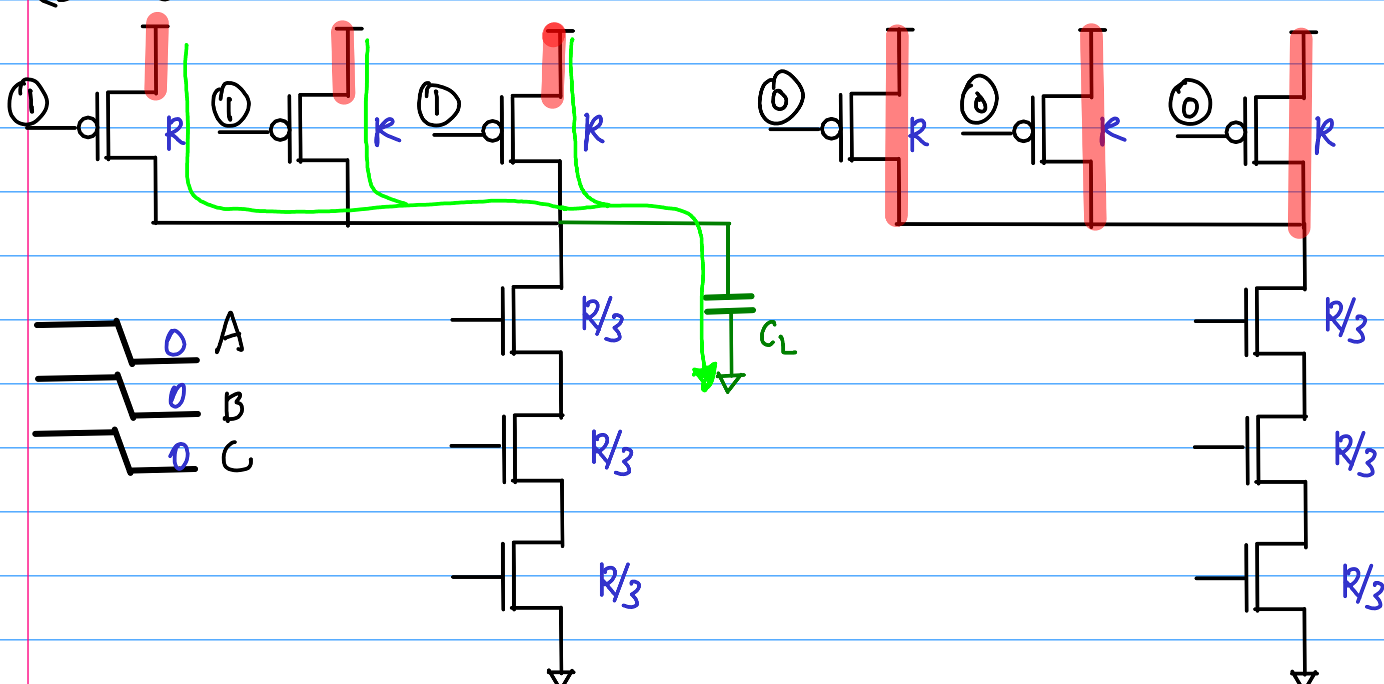
this lately rising input is feed to the nMOS that is close to Y min delay

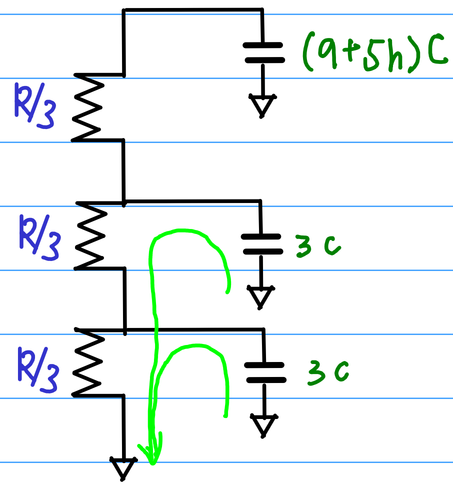
Contamination Delay t_{cdf} t_{cdr}

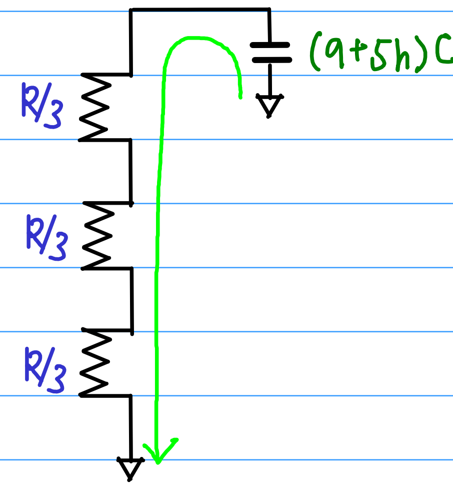
(A) Fall

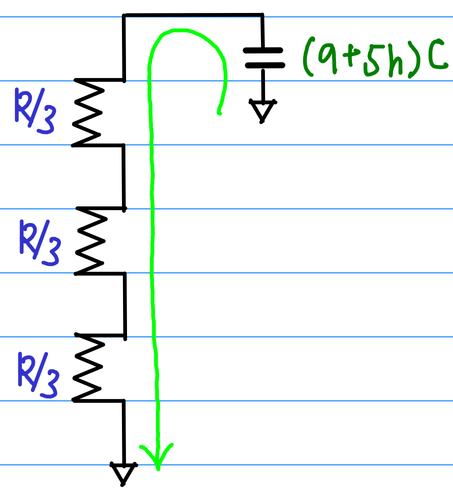


(B) Rise



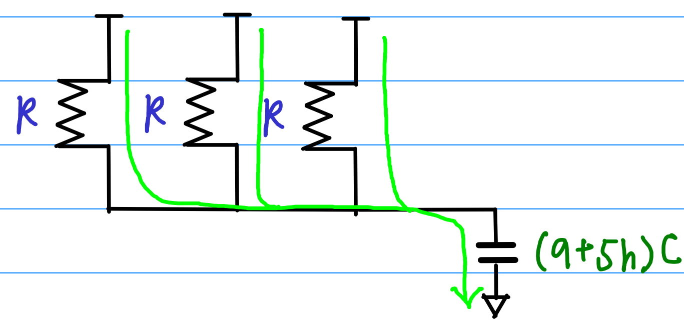






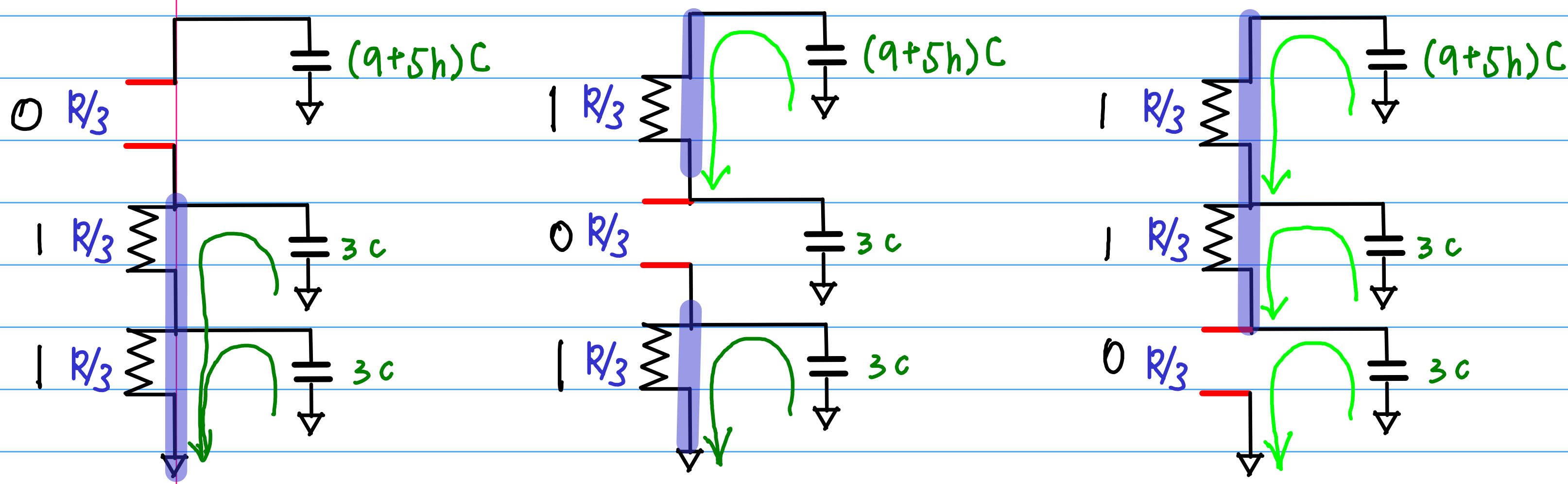
$3 \, R/3 \, (9+5h)C$

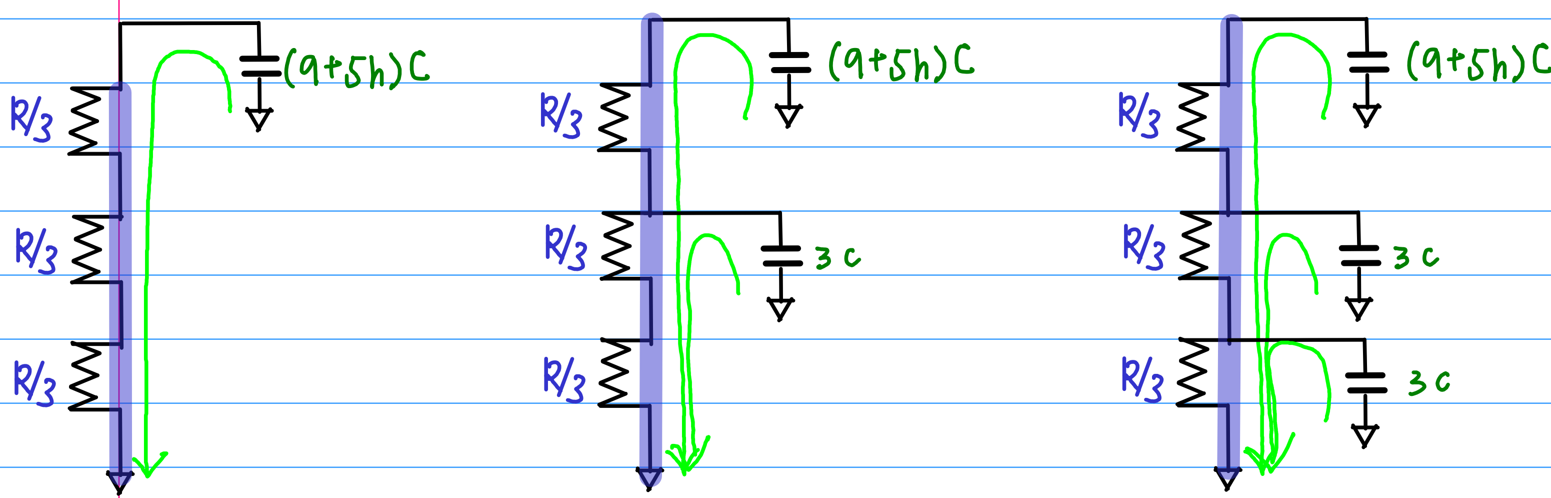
$= (9+5h) RC$



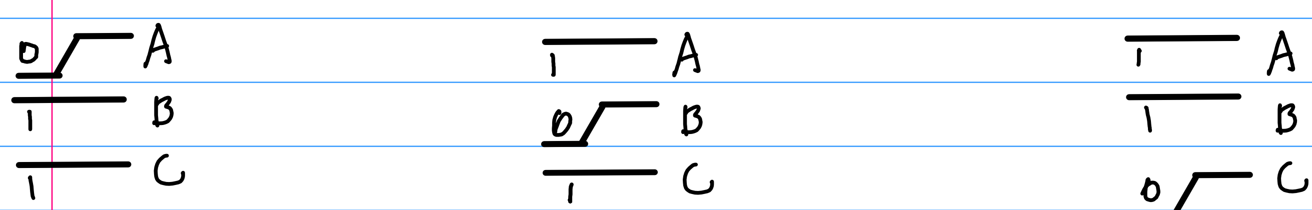
$\frac{R}{3} (9+5h)C$

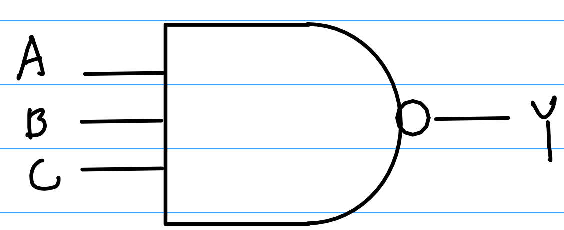
$= (3 + \frac{5}{3} h) RC$


0 R/3
1 R/3
1 R/3
(9+5h)C
3c
3c
1 R/3
0 R/3
1 R/3
(9+5h)C
3c
3c
1 R/3
1 R/3
0 R/3
(9+5h)C
3c
3c


R/3
R/3
R/3
(9+5h)C
R/3
R/3
R/3
(9+5h)C
3c
R/3
R/3
R/3
(9+5h)C
3c
3c

$t_{f1} < t_{f2} < t_{f3}$


0
A
1
B
1
C
1
A
0
B
1
C
1
A
1
B
0
C


A
B
C
Y