CMOS Delay-3 (H.3)
Logical Effort Applications

20160919

Based on

Uyemura
Introduction to VLSI Circuits and Systems

Weste
CMOS VLSI Design

for 1X Inverter

$$C_{in} = C_{ox}(W_n L + W_p L)$$
$$= C_{ox}(W_n L + r W_n L)$$
$$= C_{ox} W_n L (1 + r)$$
$$= C_{Gn}(1 + r) = C_{ref}$$

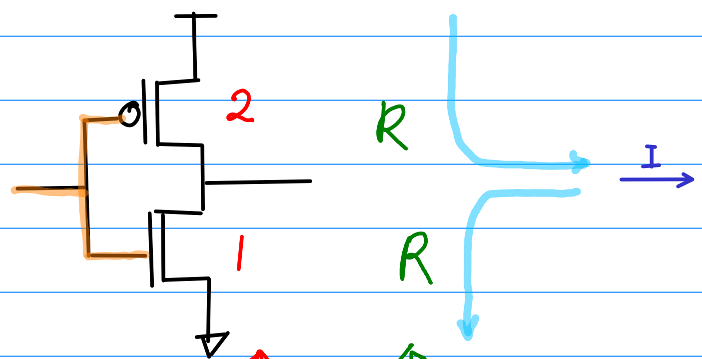
$r = 2 \sim 3$

$$g = \frac{C_{in}}{C_{ref}} = \frac{C_{ref}}{C_{ref}} = 1$$

Comparing the performance of other gates

NOT

$C_{in} = 3 = C_{ref}$

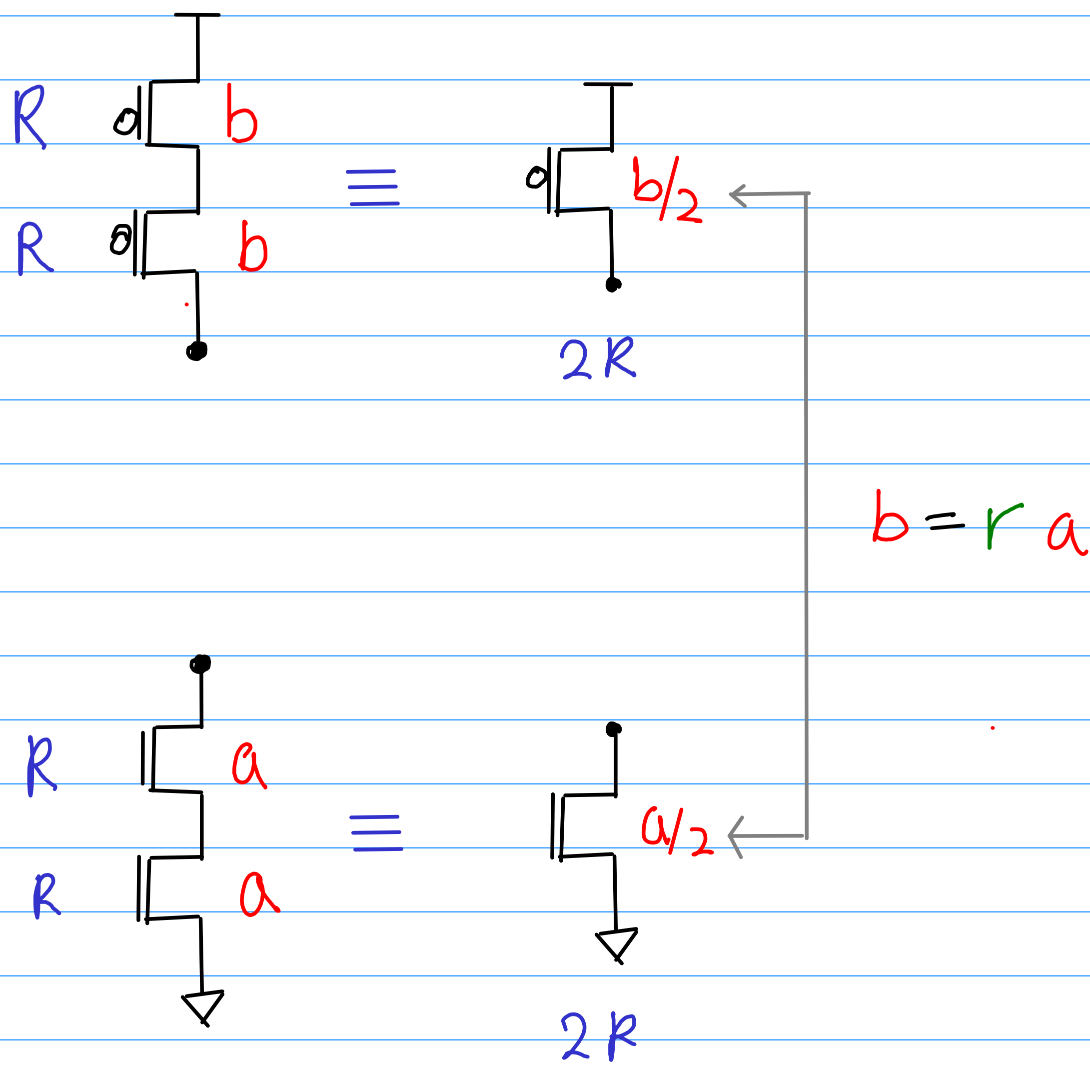


$g = \frac{3}{3} = 1$

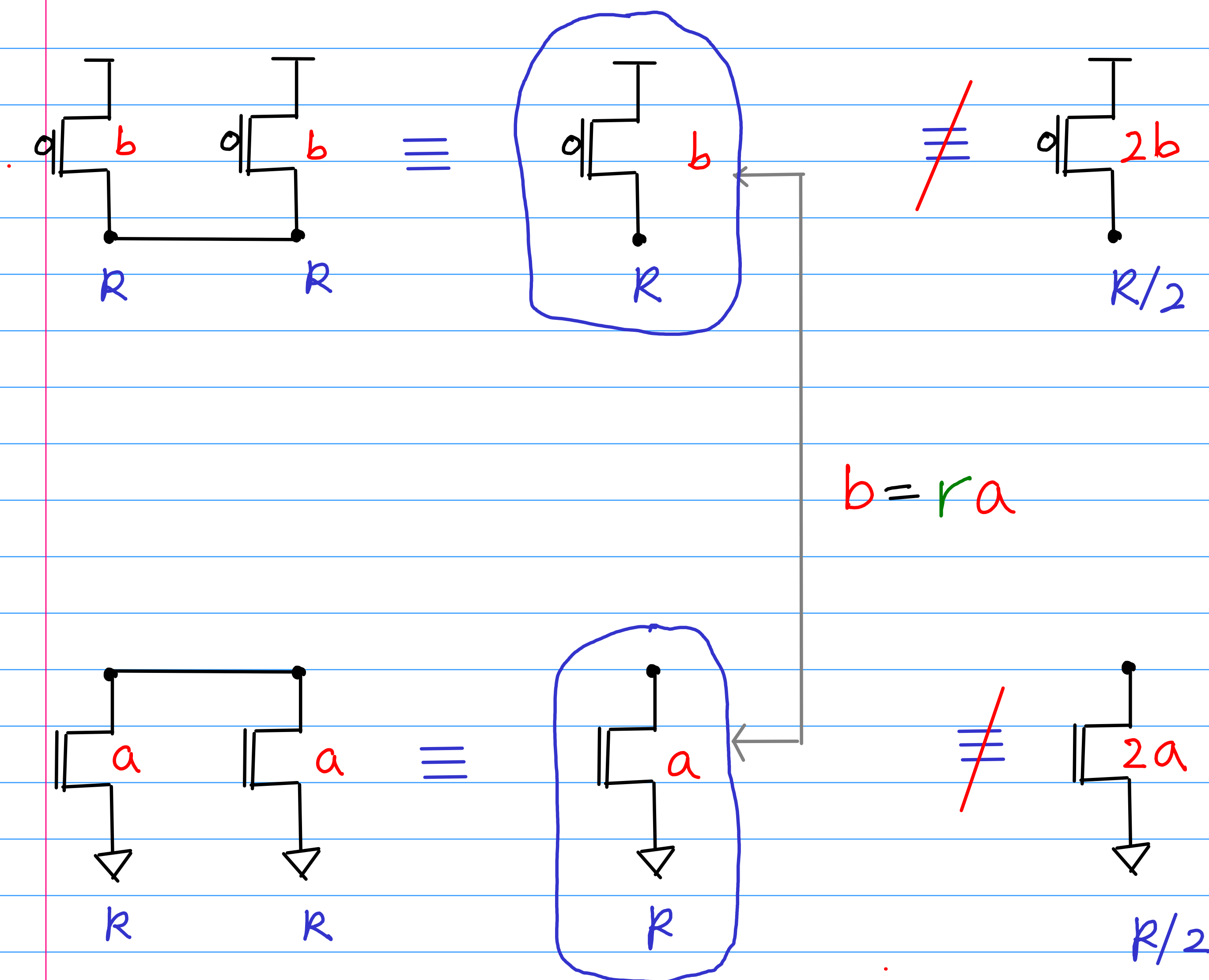
scaling info $\left(\frac{W}{L}\right)$

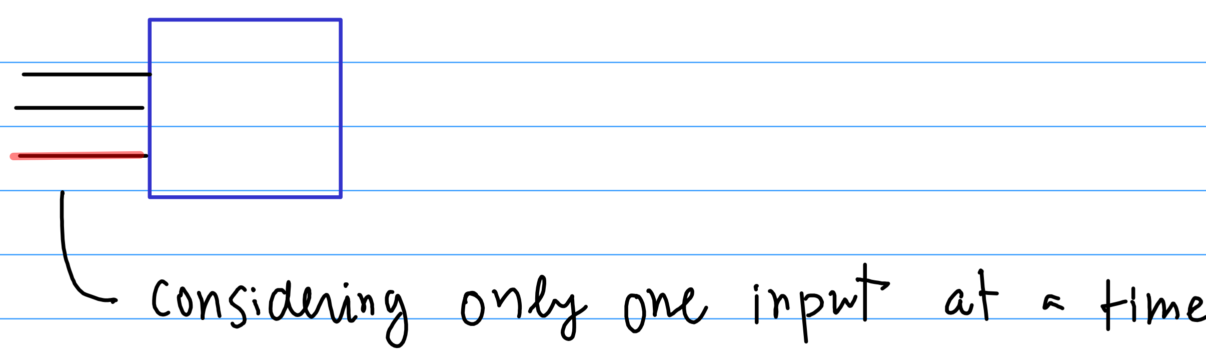
resistance

Series Connection

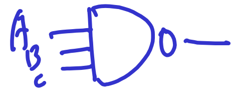


Parallel Connection

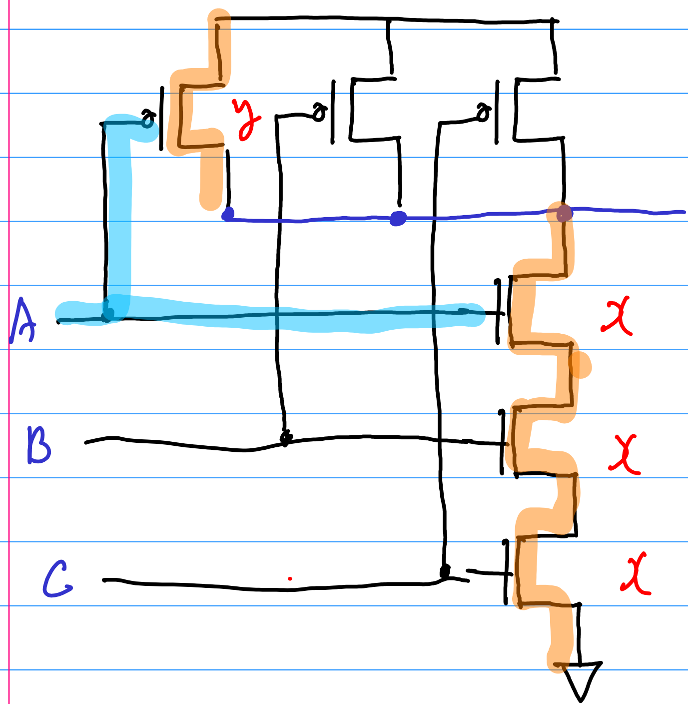




NAND



① goal



⇒ R ⇒ I **for the same output current** of the ref inverter

⇒ R ⇒ I **for the same output current** of the ref inverter

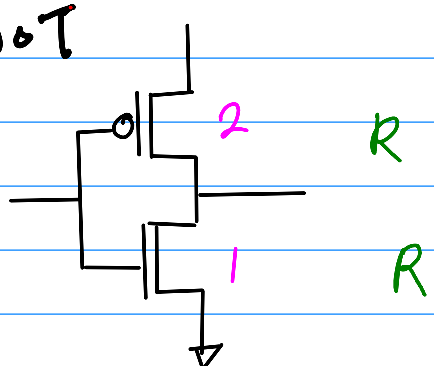
② Find Scaling info

R : $\frac{1}{y} = \frac{1}{2}$ $y = 2$

R : $\frac{1}{x} + \frac{1}{x} + \frac{1}{x} = \frac{1}{1}$ $\frac{3}{x} = 1$ $x = 3$

* reference gate

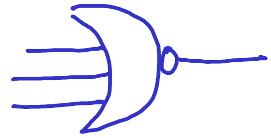
NOT

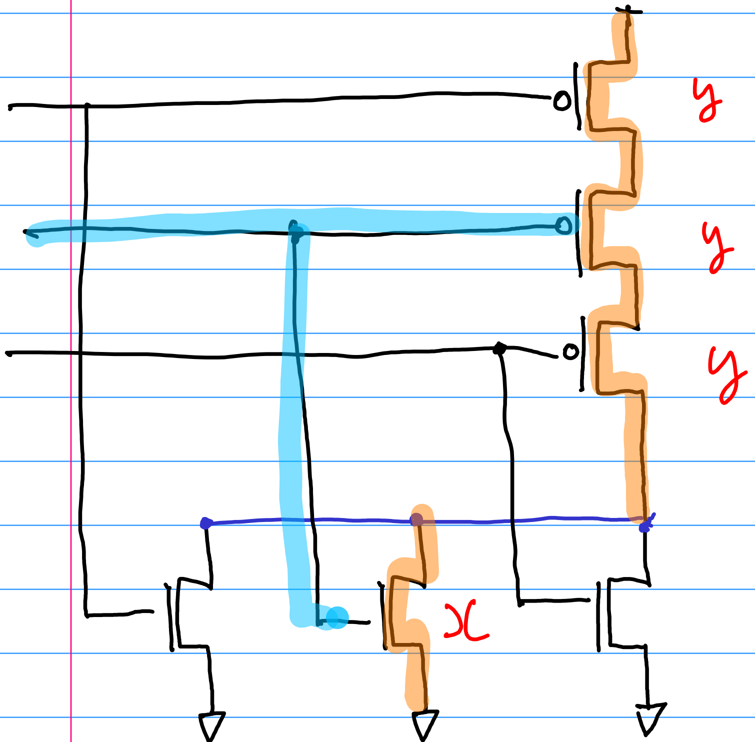


③ Compute Cin = 2+3 = 5 (y+x)
(count x+y in any input)

④ $g = \frac{C_{in}}{C_{ref}}$ = $\frac{2+3}{2+1} = \frac{5}{3}$

NOR





① goal

$\Rightarrow R \Rightarrow I$ **for the same output current** of the ref inverter

$\Rightarrow R \Rightarrow I$ **for the same output current** of the ref inverter

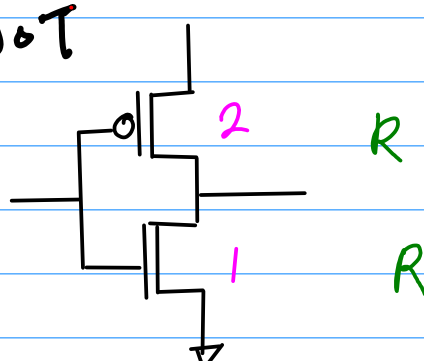
② Find Scaling info

R : $\frac{3}{y} = \frac{1}{2}$ $y = 6$

R : $\frac{1}{x} = \frac{1}{1}$ $x = 1$

* reference gate

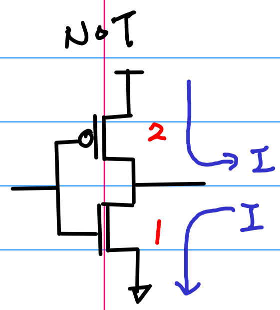
NOT



③ Compute Cin $=$ $\overset{y+x}{6+1} = 7$
(count $x+y$ in any input)

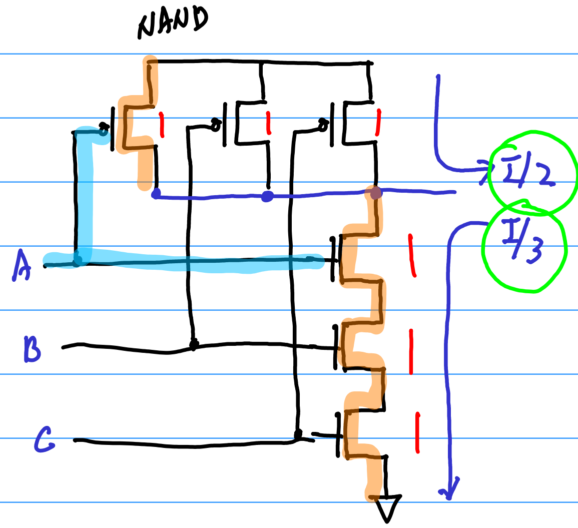
④ $g = \frac{C_{in}}{C_{ref}}$ $= \frac{6+1}{2+1} = \frac{7}{3}$

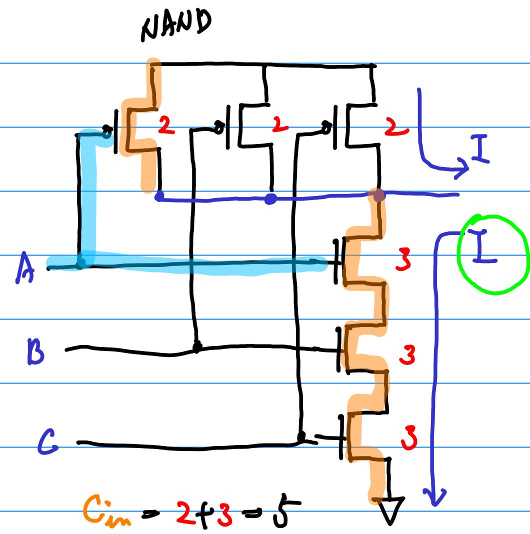
Logical Effort (g): Topological Effect



$C_{in} = 3 = C_{ref}$

$g = \frac{3}{3} = 1.$



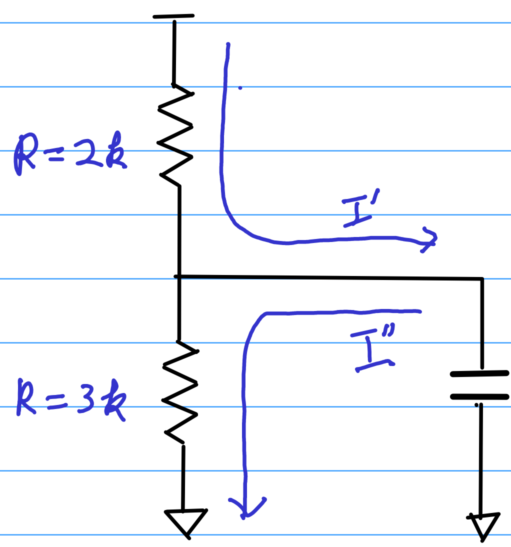


$C_{in} = 2 + 3 = 5$

$g = \frac{5}{3}$

Without proper sizing,
- pMOS's $R' = 2\,m$
- nMOS's $R'' = 3\,m$

- pMOS's $I' = I/2$
- nMOS' $I' = I/3$



to get I,
pMOS enlarged by a factor of 2
nMOS enlarged by a factor of 3

$t_f \propto RC$ $\quad$ $t_r \propto RC$

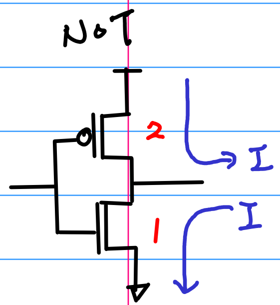
$t_f \propto 3$ $\quad$ $t_r \propto 2$

$$t_{avg} = \frac{t_f + t_r}{2} \propto (3+2)$$

$$t_f + t_r \propto (3+2)$$

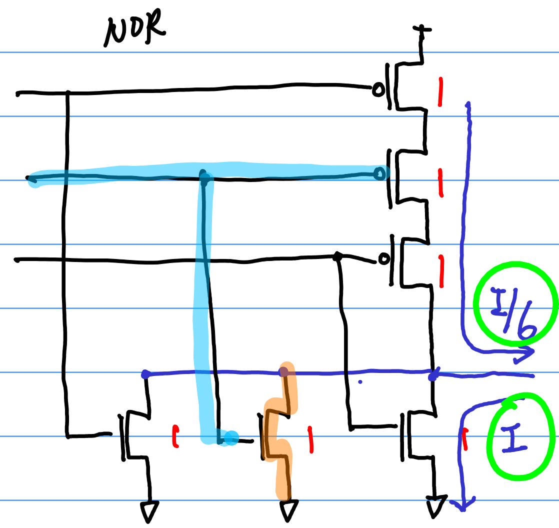
$$\boxed{g = \frac{C_{in}}{C_{ref}}} = \frac{t_{avg} \text{ of NAND}}{t_{avg} \text{ of NOT}}$$

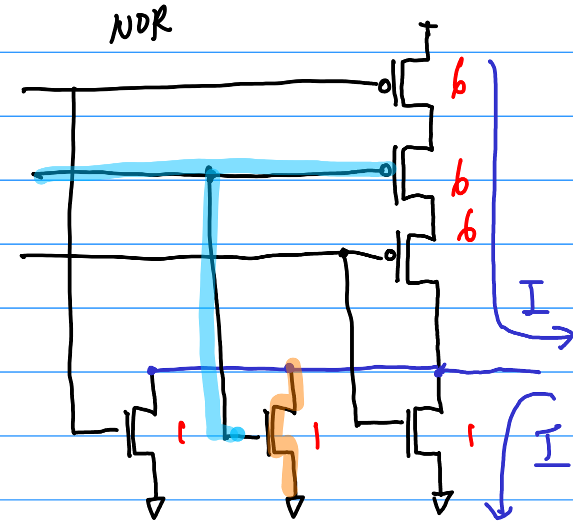
Logical Effort (g): Topological Effect



$C_{in} = 3 = C_{ref}$

$g = \frac{3}{3} = 1.$





$C_{in} = 6 + 1 = 7$

$g = \frac{7}{3}$

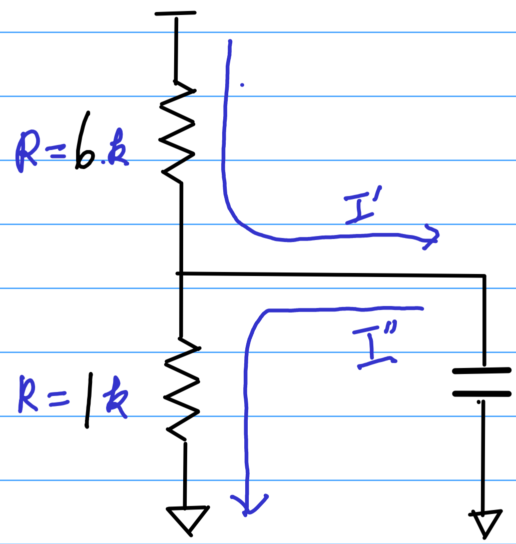
Without proper sizing,

pMOS's $R' = 6\ m$

nMOS's $R'' = 1\ m$

pMOS's $I' = I/6$

nMOS' $I'' = I$



to get I,

pMOS enlarged by a factor of 6

nMOS enlarged by a factor of 1

$t_f \propto RC \qquad t_r \propto RC$

$t_f \propto 1 \qquad t_r \propto 6$

$$t_{avg} = \frac{t_f + t_r}{2} \propto (1 + 6)$$

$$t_f + t_r \propto (1 + 6)$$

$$g = \frac{C_{in}}{C_{ref}} = \frac{t_{avg} \text{ of NOR}}{t_{avg} \text{ of NOT}}$$

Electrical Effort (h) : Fan Out Load

Electrical Effort : the output & input cap ratio

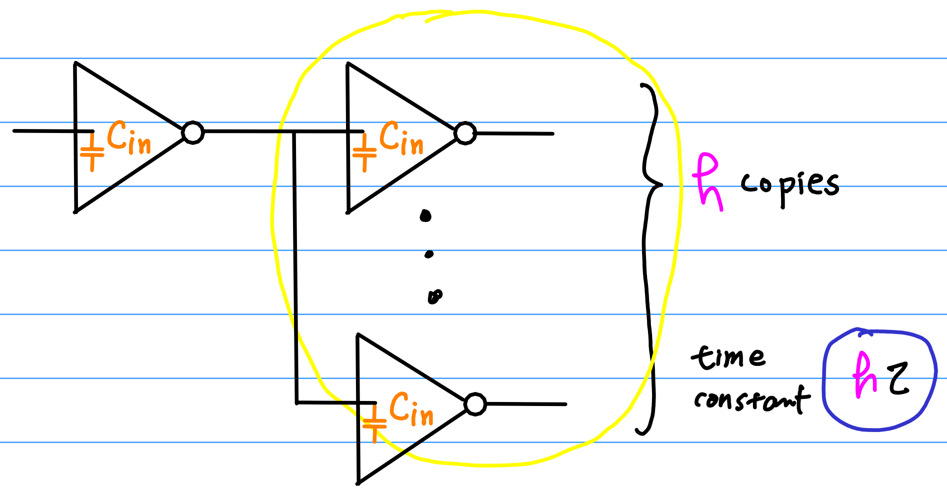
$$h = \frac{C_{out}}{C_{in}}$$

the ratio of the drive strength to drive C_{out} to the drive strength to drive its own capacitance C_{in}

C_{out} is h times larger than C_{in}

$$C_{out} = h\,C_{in}$$

h copies of the same gate

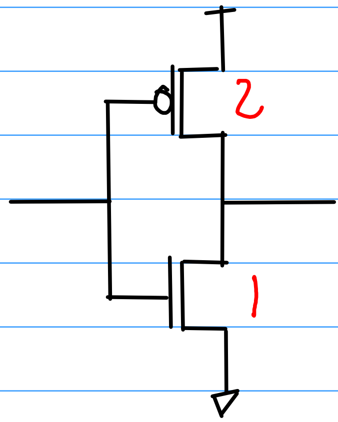


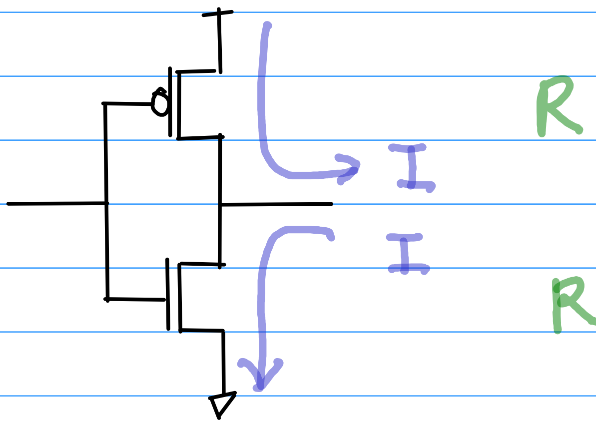
$h \cdot C_{in}$

Parasitic Delay p

- delay due to internal parasitic capacitance (sC_p)
- excluding external load cap (C_{out})
- count only diffusion capacitance of the output
- delay without output load

$$p = \left(\frac{C_{p,ref}}{C_{ref}}\right) = \left(\frac{\text{internal diffusion cap}}{\text{gate cap of ref inv}}\right) = \frac{\tau_{par}}{\tau_{ref}}$$

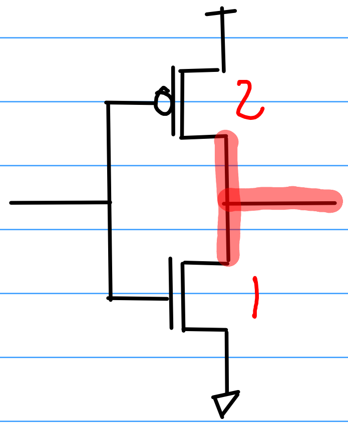




②,①: scaling info in order for PUN & PDN to have the same R, I

$$\tau_{ref} = R \cdot C_{in} = R_{ref} \cdot C_{ref} = R \cdot 3C = 3RC$$

$$\tau_{inv} = R_{ref} \cdot C_{p,ref} = R \cdot 3C = 3RC$$



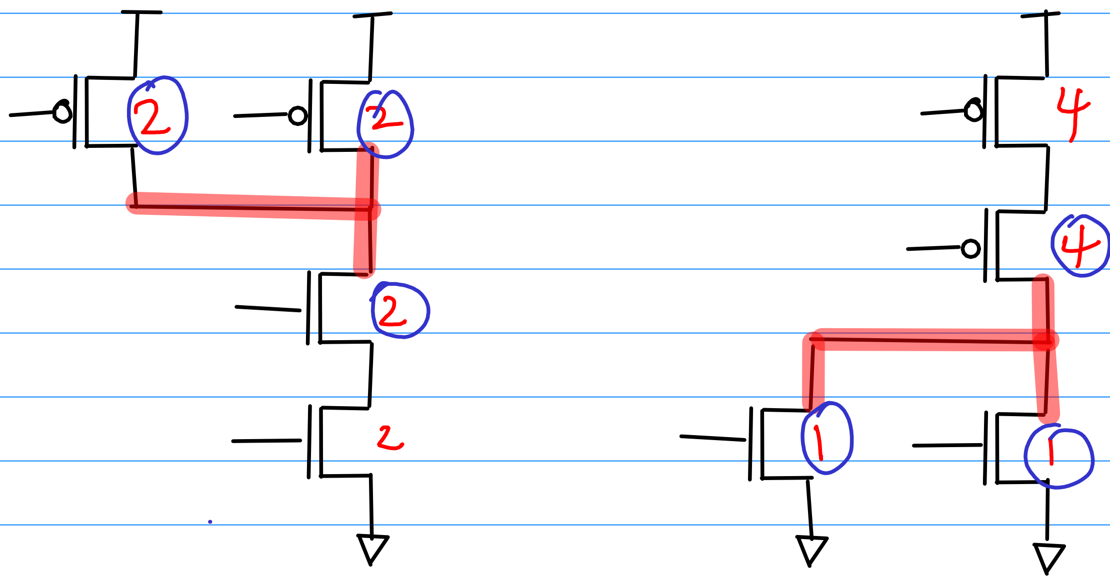
$C_{p,ref}$ ⇒ count scaling factors connected to the output

$$C_{p,ref} = 2 + 1 = 3$$

$$p = \left(\frac{C_{p,ref}}{C_{ref}}\right) = \left(\frac{\text{internal diffusion cap.}}{\text{gate cap of ref inv}}\right) = \frac{\tau_{par}}{\tau_{ref}}$$

$$p = \frac{\tau_{par}}{\tau_{ref}} = \frac{R_{ref} \cdot C_{p,ref}}{R_{ref} \cdot C_{ref}}$$

C_{ref} ← Cin of the reference inverter (Symmetric inverter)



$2 + 2 + 2 = 6$ $\qquad\qquad$ $4 + 1 + 1 = 6$

$p_{NAND2} = \frac{6}{3} = 2$ $\qquad\qquad$ $p_{NOR2} = \frac{6}{3} = 2$

$$P = \frac{\tau_{par}}{\tau_{ref}} = \frac{R_{ref} \cdot C_{p,ref}}{R_{ref} \cdot C_{ref}}$$

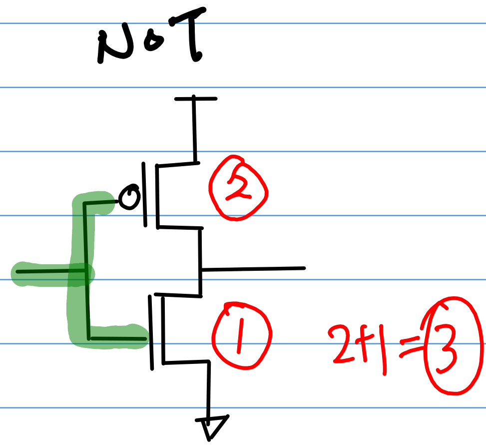
C_{ref} → 3

C_{in} of the reference inverter

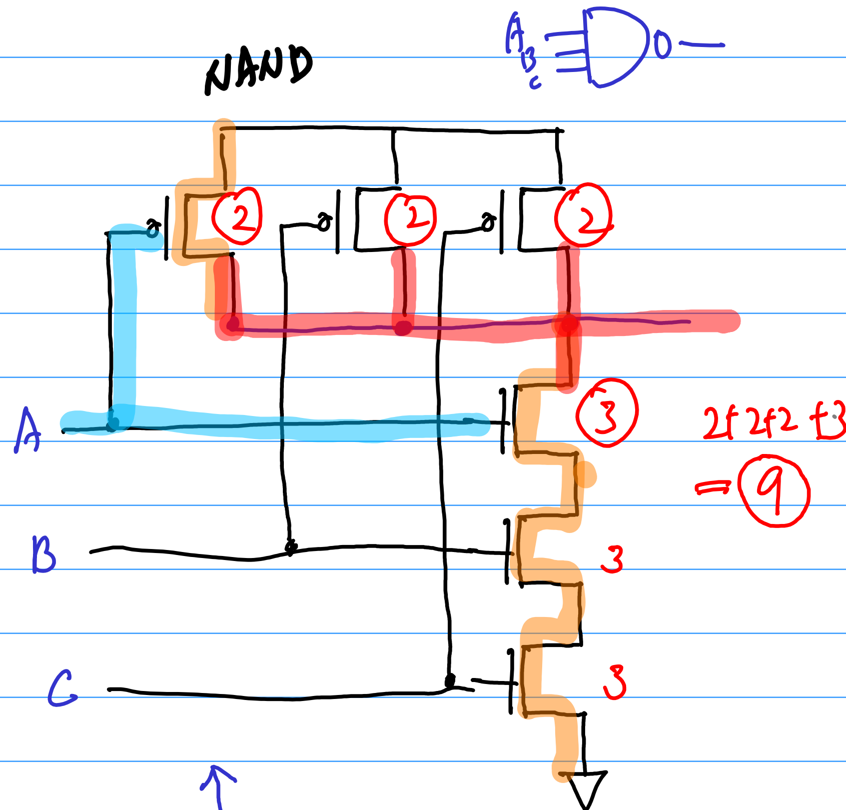
(Symmetric inverter)

$$P = \frac{1}{3}\left(\sum \text{Output scaling factors}\right)$$

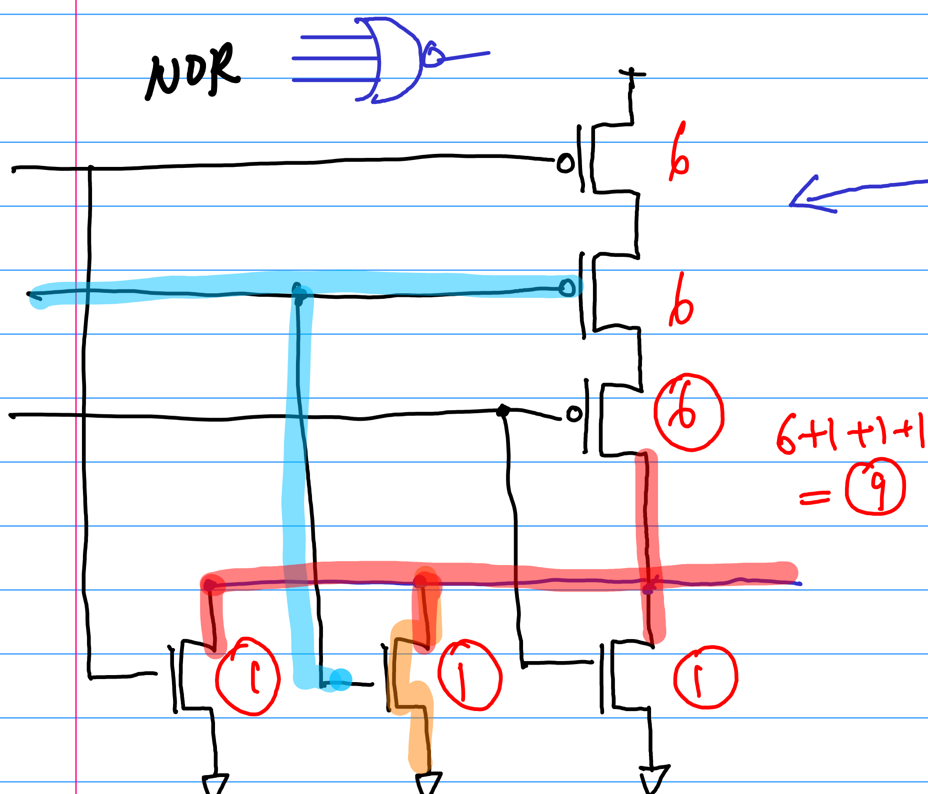
Parasitic Delay



$C_{ref} = 3$

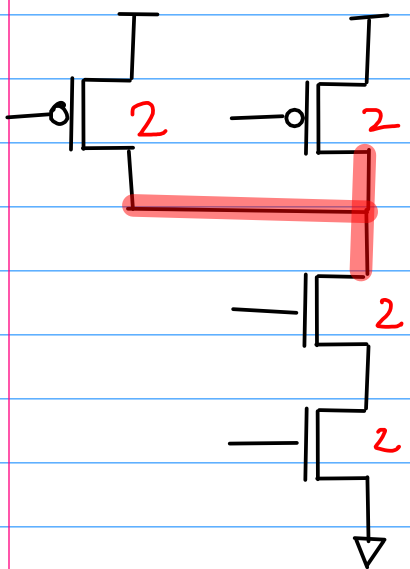


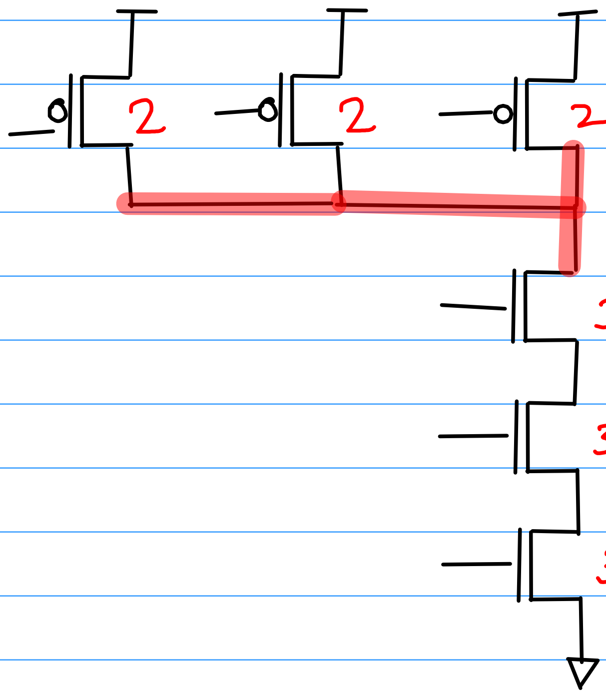
$$\left(\frac{C_{p,ref}}{C_{ref}}\right) = \frac{9}{3} = 3$$



$$\left(\frac{C_{p,ref}}{C_{ref}}\right) = \frac{9}{3} = 3$$

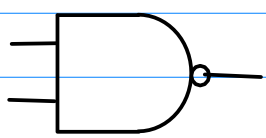
(P) NAND2 NAND3



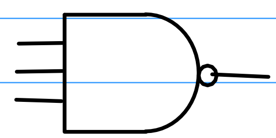


$2+(2+2)=2(1+2)$

$3+(2+2+2)=3(1+2)$

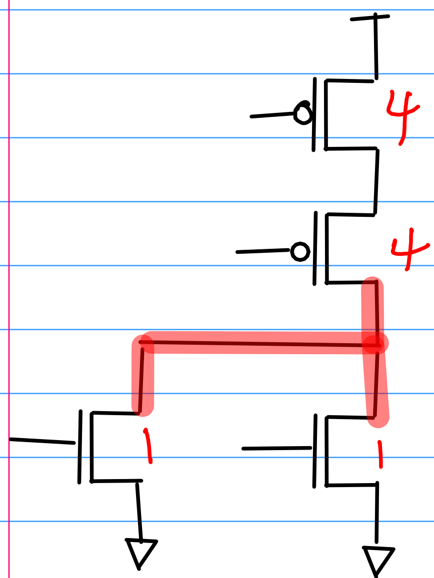


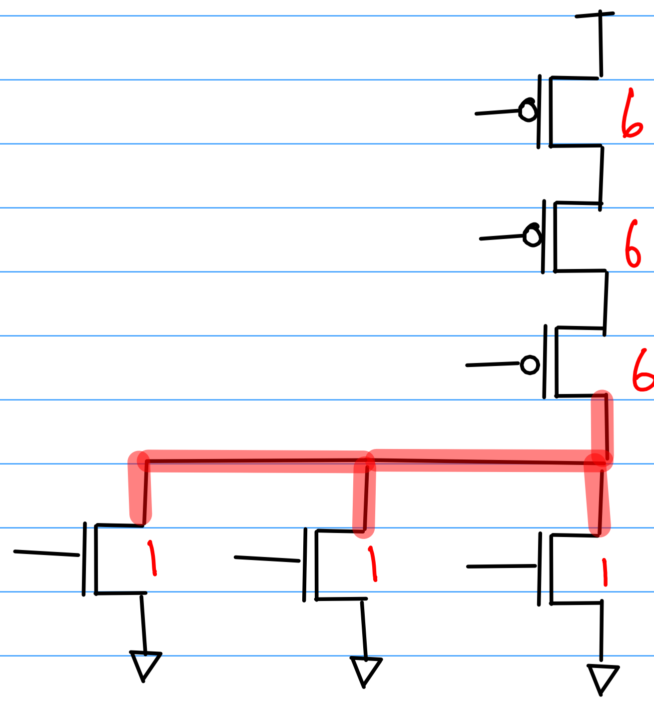
$\frac{2\cdot 3}{3}=2$



$\frac{3\cdot 3}{3}=3$

(p) NOR2 NOR3



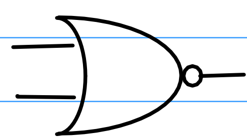


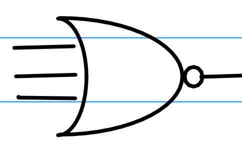
$4+1+1 = 2\cdot 2 + 2\cdot 1 = 6$

$6+6+6+1+1+1 = 3\cdot 2 + 3\cdot 1 = 3(2+1) = 9$

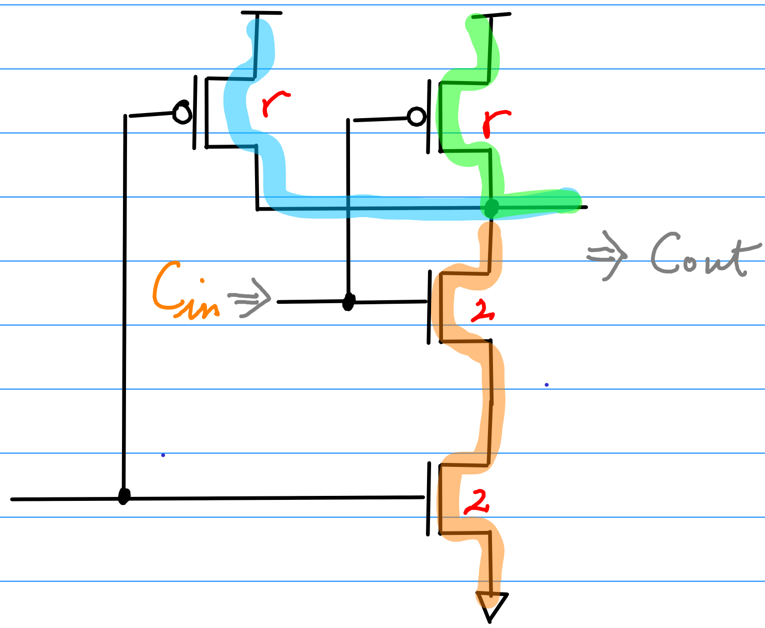
$\frac{6}{3} = 2$

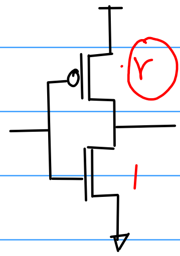
$\frac{9}{3} = 3$





Symmetric NAND2 ⓖ





$R = \frac{1}{2} + \frac{1}{2} = 1$

pMOS size r

⇐ the worst case path from V_{DD} to V_{out} is the same as the reference inverter

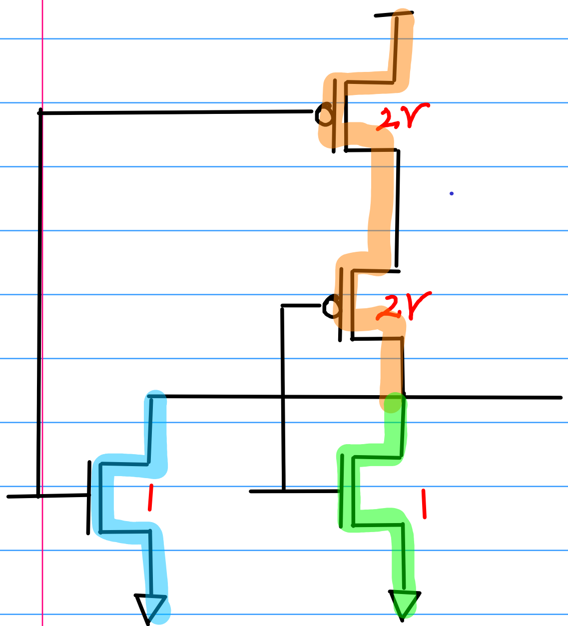
nMOS size ②

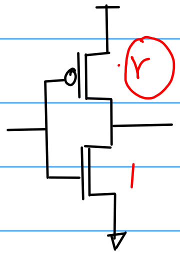
⇐ the worst case path from GND to V_{out} must be twice as large as the inverter (series connection)

$C_{in} = C_{gn}(2+r)$

$$g = \frac{C_{in}}{C_{ref}} = \frac{C_{gn}(2+r)}{C_{gn}(1+r)} = \frac{2+r}{1+r}$$

Symmetric NOR2 (g)





$R = \frac{1}{2r} + \frac{1}{2r} = \frac{1}{r}$

pMOS size 2r

⇐ the worst case path from V_{DD} to V_{out} must be twice as the inverter

(series connection)

nMOS size 1

⇐ the worst case path from GND to V_{out} must be the same as as the inverter

$C_{in} = C_{gn}(1 + 2r)$

$$g = \frac{C_{in}}{C_{ref}} = \frac{C_{gn}(1+2r)}{C_{gn}(1+r)} = \frac{1+2r}{1+r}$$

n-input NAND, NOR (g)

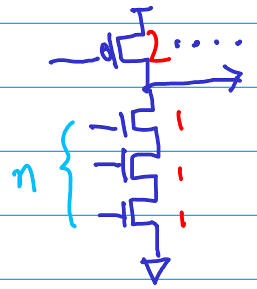
NAND2 $g = \frac{2+r}{1+r}$

NOR2 $g = \frac{1+2r}{1+r}$

n-input NAND $g = \frac{n+r}{1+r}$

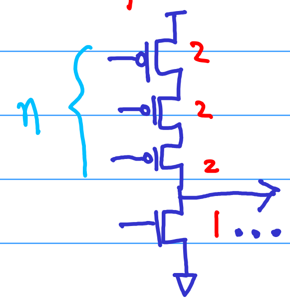
n-input NOR $g = \frac{1+nr}{1+r}$

n-input NAND



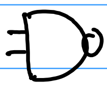
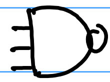
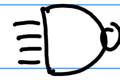
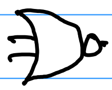
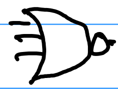
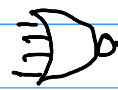
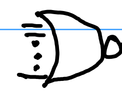
$(1 \cdot n + 2)$

n-input NOR



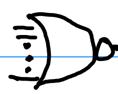
$(1 + 2 \cdot n)$

Logical Effort g

2	3	4	n
			n 
$\frac{4}{3} = \frac{(2+2)}{(1+2)}$	$\frac{5}{3} = \frac{(3+2)}{(1+2)}$	$\frac{6}{3} = \frac{(4+2)}{(1+2)}$	$\frac{(n+2)}{(1+2)}$
			n 
$\frac{5}{3} = \frac{(1+2\cdot 2)}{(1+2)}$	$\frac{7}{3} = \frac{(1+2\cdot 3)}{(1+2)}$	$\frac{9}{3} = \frac{(1+2\cdot 4)}{(1+2)}$	$\frac{(1+2\cdot n)}{(1+2)}$

n 

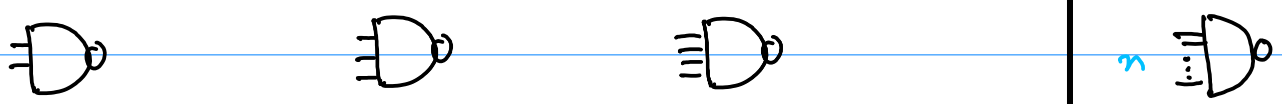
$$g = \frac{(n+r)}{(1+r)}$$

n 

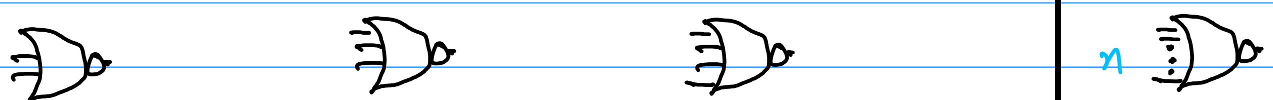
$$g = \frac{(1+r\cdot n)}{(1+r)}$$

Parasitic delay (P)

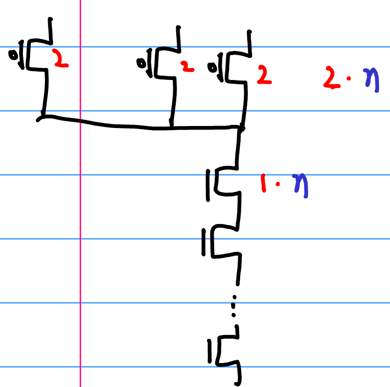
2	3	4	n



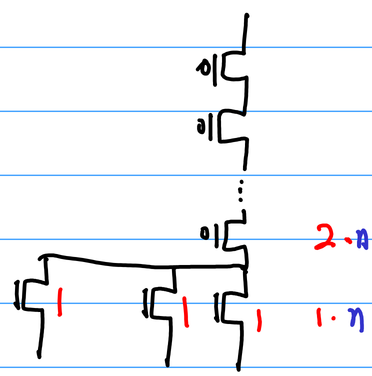
$$\frac{6}{3} = \frac{2(1+2)}{(1+2)} \qquad \frac{9}{3} = \frac{3(1+2)}{(1+2)} \qquad \frac{12}{3} = \frac{4(1+2)}{(1+2)} \qquad \frac{n(1+2)}{(1+2)} = n$$



$$\frac{6}{3} = \frac{2(1+2)}{(1+2)} \qquad \frac{9}{3} = \frac{3(1+2)}{(1+2)} \qquad \frac{12}{3} = \frac{4(1+2)}{(1+2)} \qquad \frac{n(1+2)}{(1+2)} = n$$



3n



3n

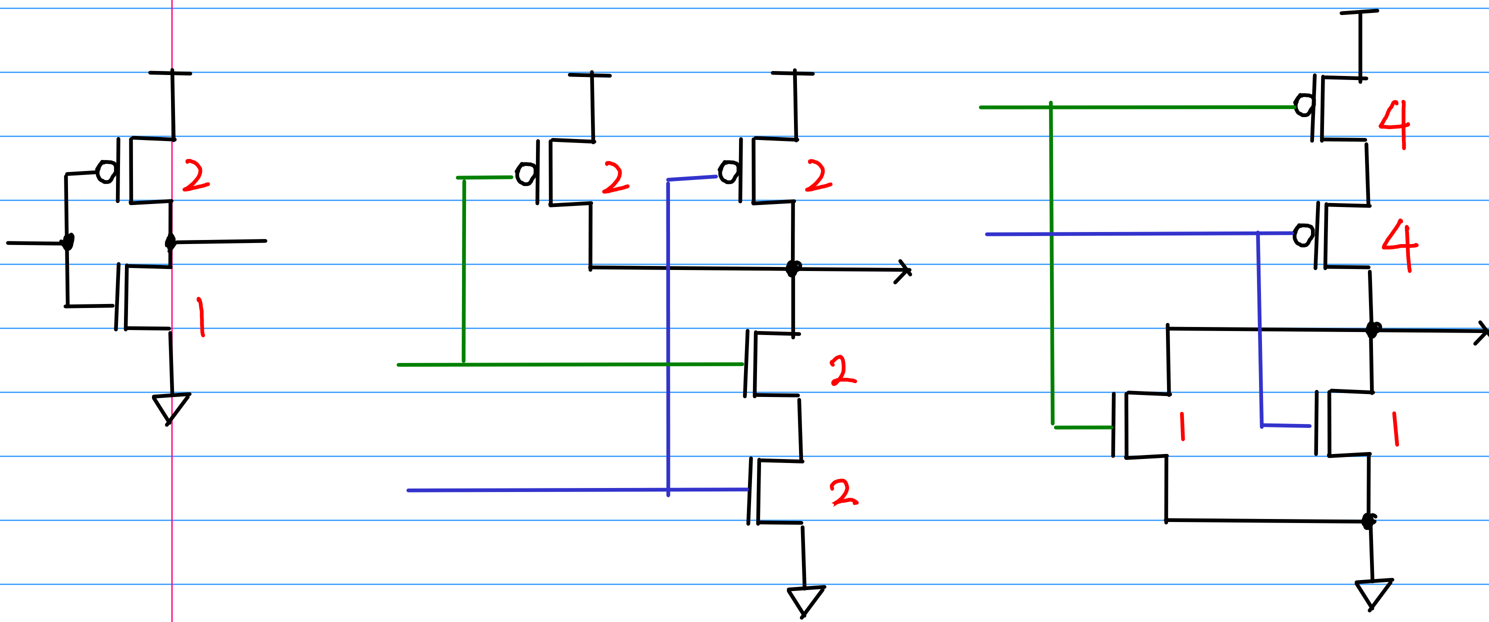
① Logical Effort for the Same R (the same I)

* Fixed output R

② Logical Effort for the Same C_{in}

* Fixed Input C

① Fixed output R



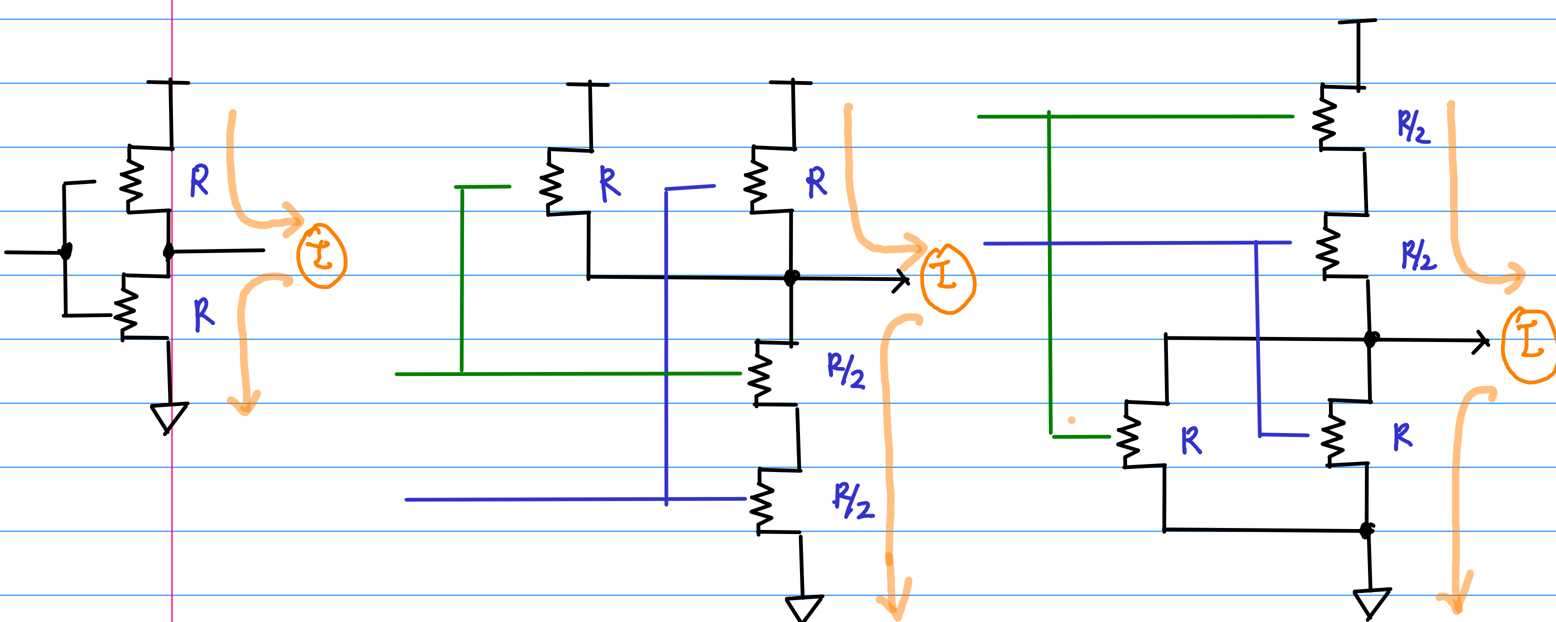
$C_{in} = C_{ref} = 3$

$C_{in} = 4$

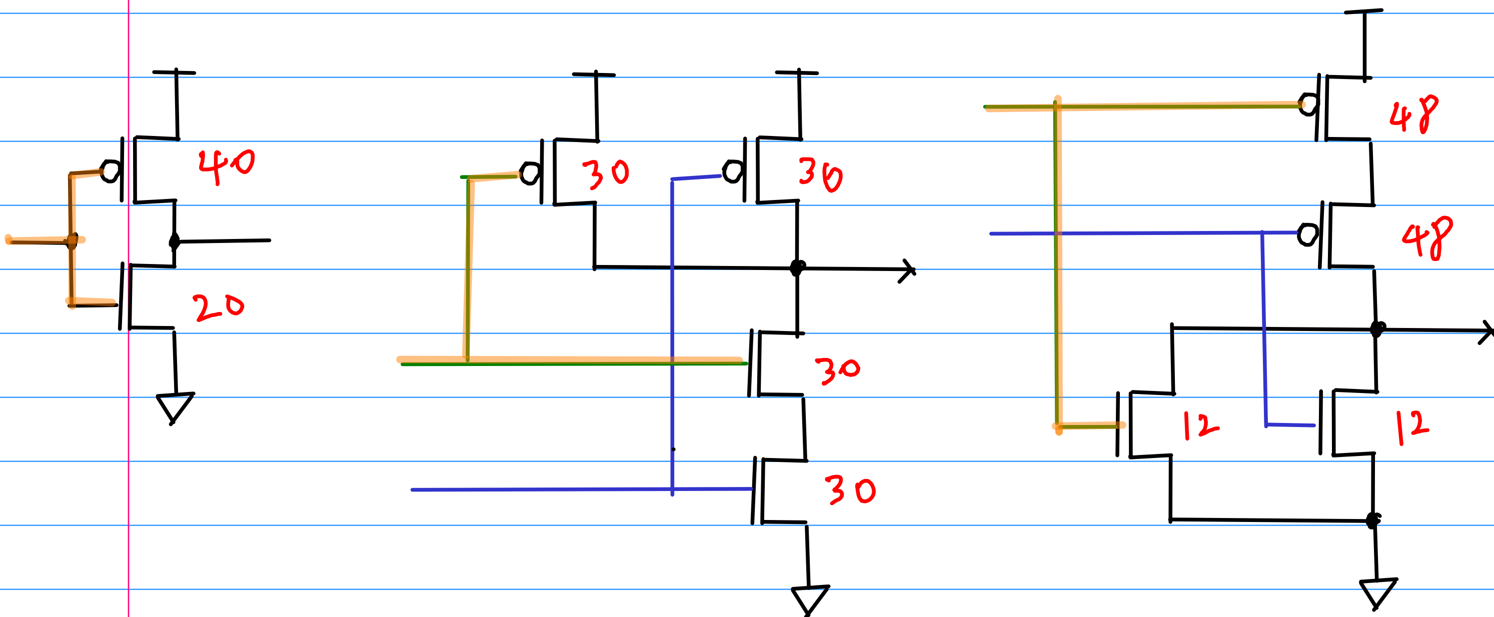
$g = \frac{4}{3}$

$C_{in} = 5$

$g = \frac{5}{3}$



② Fixed Input C



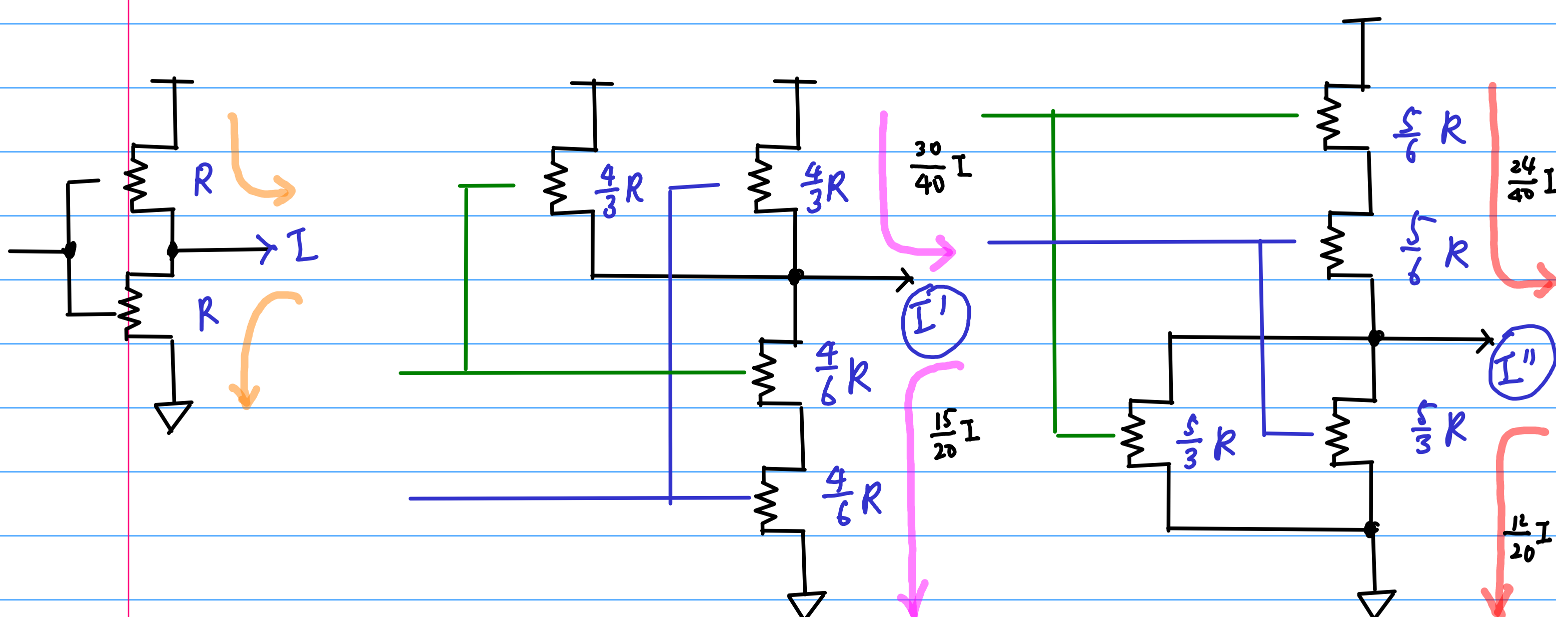
$C_{in} = 60$ $\quad$ $C_{in} = 60$ $\quad$ $C_{in} = 60$

$40 : I = 30 : I'_1$

$20 : I = 15 : I'_2$

$40 : I = 24 : I''_1$

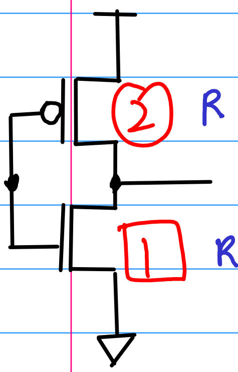
$20 : I = 12 : I''_2$

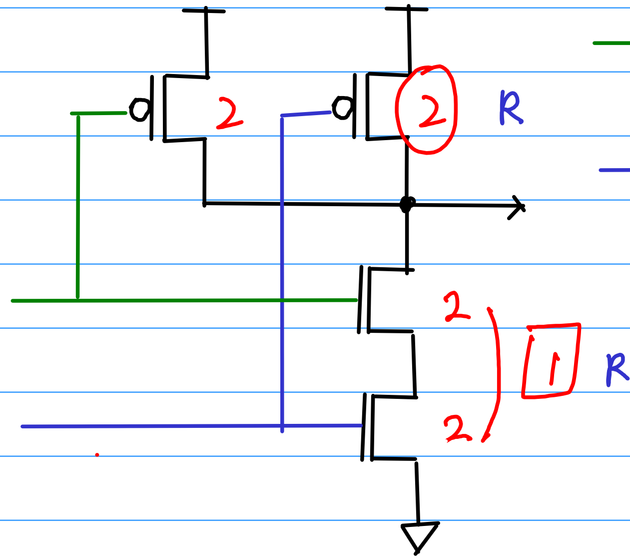


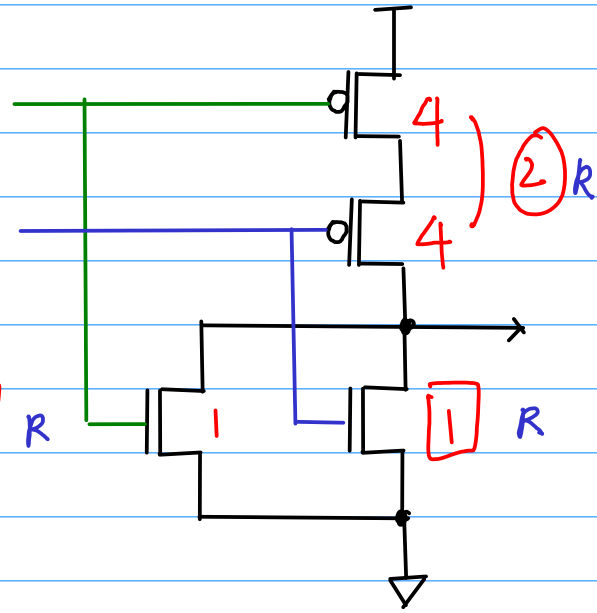
$g = \frac{I}{I'} = \frac{4}{3}$ $\quad$ $g = \frac{I}{I''} = \frac{5}{3}$

"Logical Effort Designing Fast CMOS Circuits", Sutherland, Sproull, Harris

① Fixed output R







$C_{in} = C_{ref} = 3$

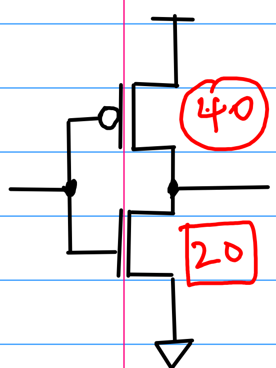
$C_{in} = 4$

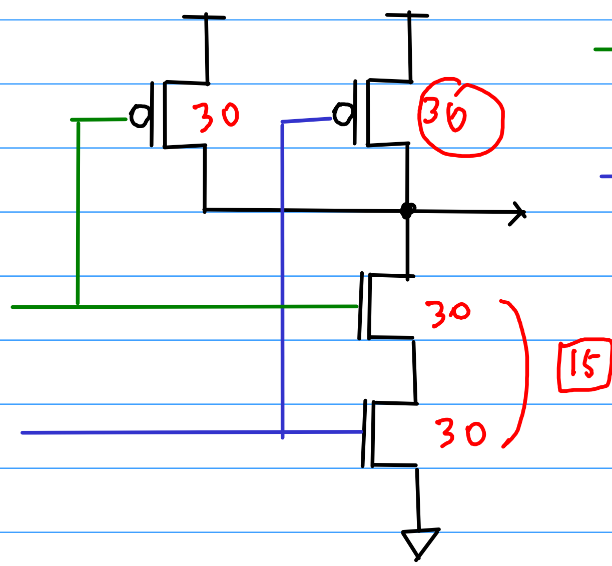
$g = \frac{4}{3}$

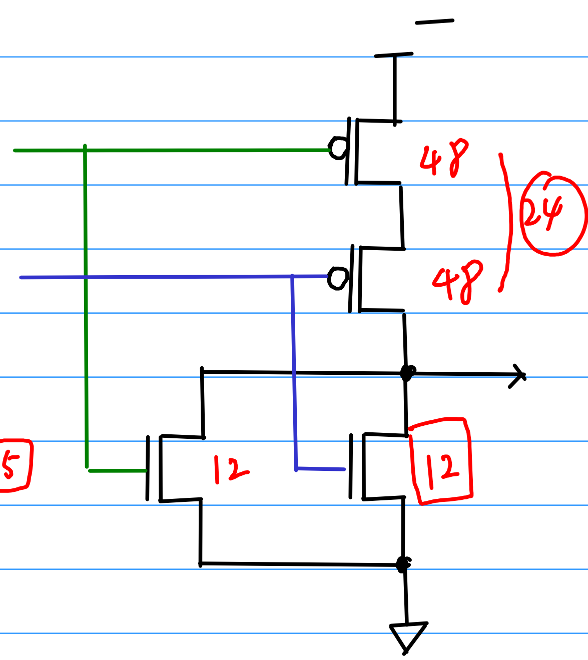
$C_{in} = 5$

$g = \frac{5}{3}$

② Fixed Input C







$C_{in} = 60$

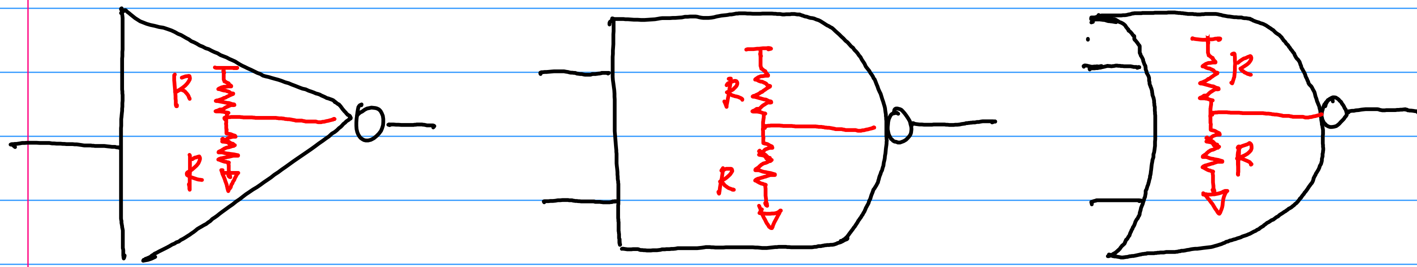
$C_{in} = 60$

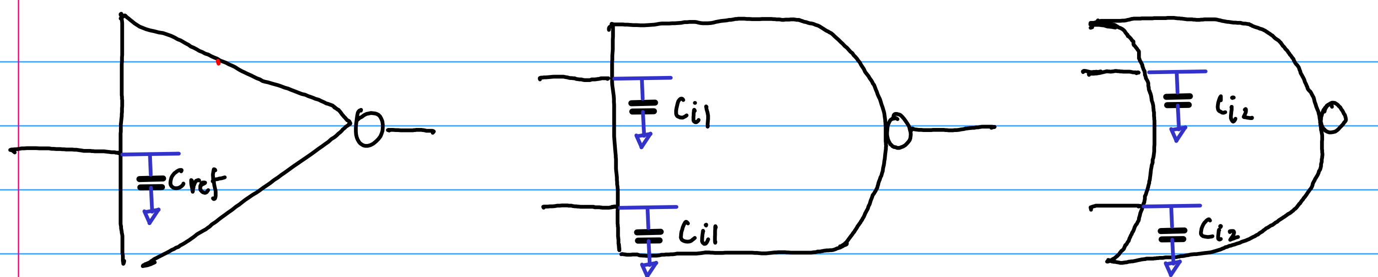
$g = \frac{40}{30} = \frac{20}{15} = \frac{4}{3}$

$C_{in} = 60$

$g = \frac{40}{24} = \frac{20}{12} = \frac{5}{3}$

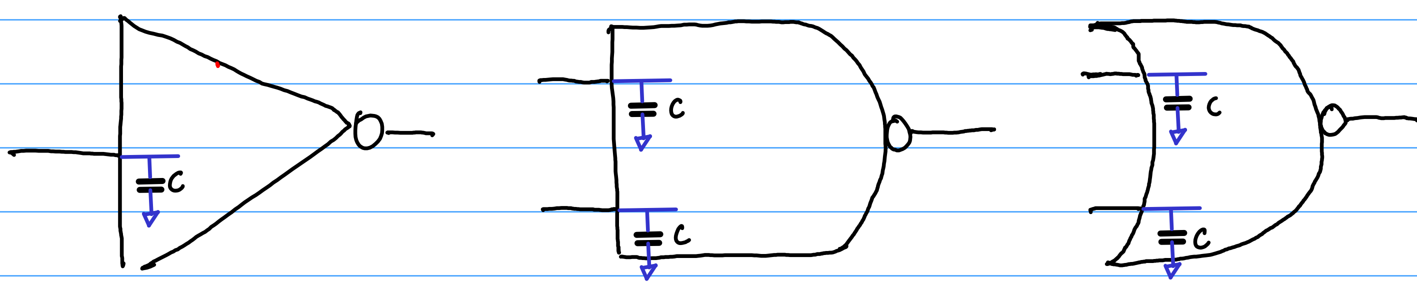
* Fixed output R → must increase size → Cin ↑

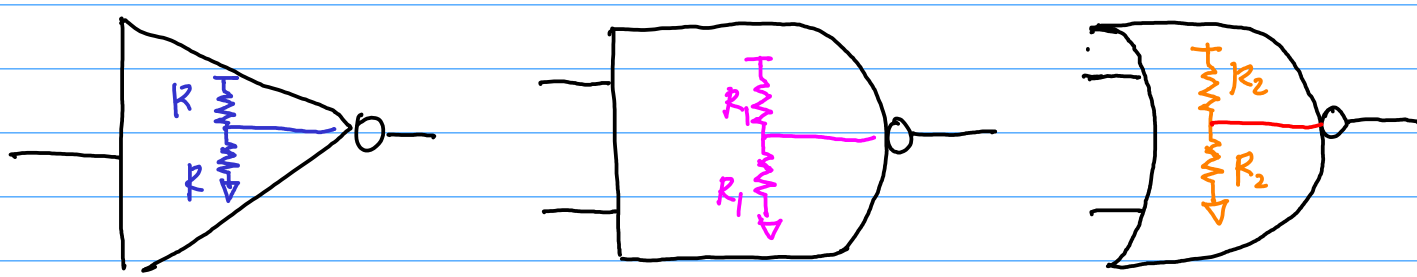




$g = \frac{C_{i1}}{C_{ref}}$ $g = \frac{C_{i2}}{C_{ref}}$

* Fixed Input Cap → Complexity of logic gate increase R ↑

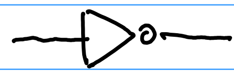
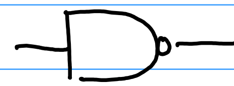




$g = \frac{R_1}{R}$ $g = \frac{R_2}{R}$

* Fixed Output R

the same output I as that of 

 . 

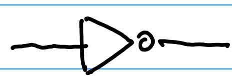
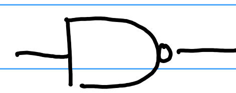
more complex topology than 

for the same I

the size must be increased.

ratio $g = \frac{C_{in}}{C_{ref}}$

* Fixed Input C

 . 

more complex topology than 

the output current becomes smaller

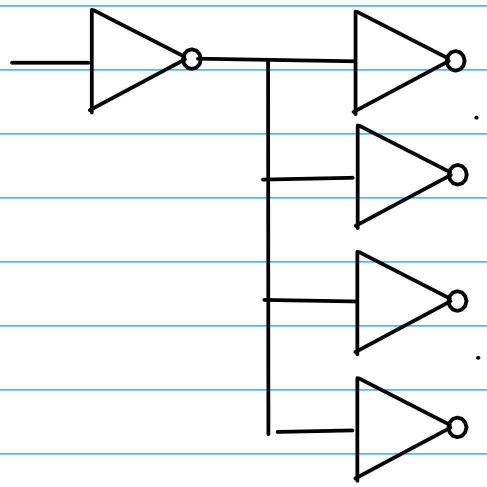
the output R becomes greater

ratio $g = \frac{R}{R_{ref}}$

Symmetric $\Rightarrow$

fall time = rise time

FO4

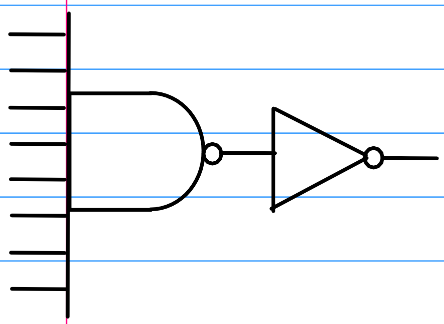


$g = 1$

$p = 1$

$$gh + p = 1 \cdot h + 1 = h+1$$

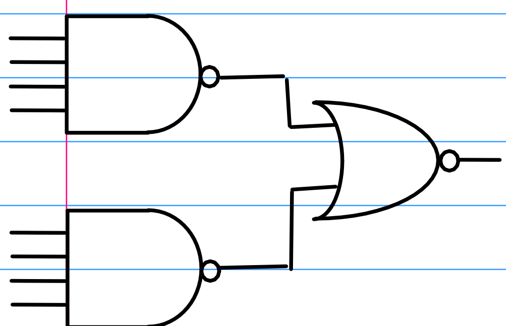
$$g_{NAND} = \frac{n + r}{1 + r} \qquad g_{NOR} = \frac{1 + nr}{1 + r}$$



$g = 10/3$ $g = 1$

$$\frac{8+2}{1+2} = \frac{10}{3} \qquad \frac{1+2}{1+2} = 1$$

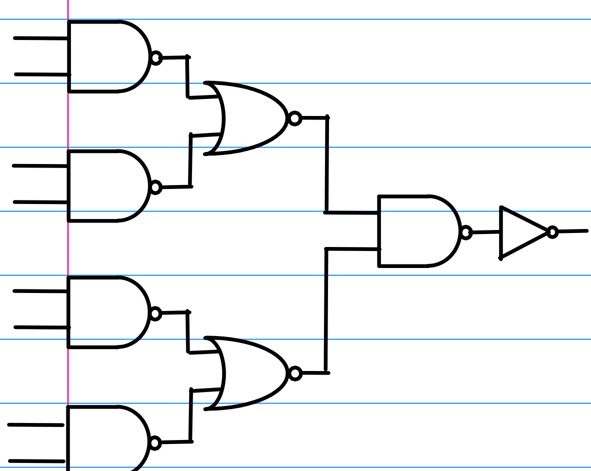
$$G = \frac{10}{3}$$



$g = 2$ $g = 5/3$

$$\frac{4+2}{1+2} = \frac{6}{3} = 2 \qquad \frac{1+2\cdot 2}{1+2} = \frac{5}{3}$$

$$G = \frac{10}{3}$$



$g = 4/3$ $g = 5/3$ $g = 4/3$ $g = 1$

$$\frac{2+2}{1+2} = \frac{4}{3} \qquad \frac{1+2\cdot 2}{1+2} = \frac{5}{3}$$

$$G = \frac{4}{3} \times \frac{5}{3} \times \frac{4}{3} = \frac{80}{27}$$