CMOS Delay-2 (H.2)
Logical Effort

20160826

Based on

Uyemura
Introduction to VLSI Circuits and Systems

Weste
CMOS VLSI Design

Logical Effort Techniqus

- shows how many stages of logic are required
  for the fastest implementation
  of any given logic function

Scaling of logic cascades
Characterize logic gates & their interaction
to provide techniques to minimize the delay

<High speed chains>

estimate

* delays through logic cascades

* scaling information

for minimum delay designs

the logical effort g

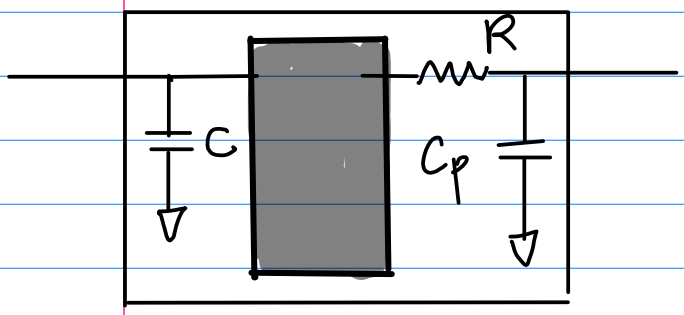
referenced to the 1X reference inverter

with input capacitance Cref
and transistor resitance Rref

Scale for the same current I

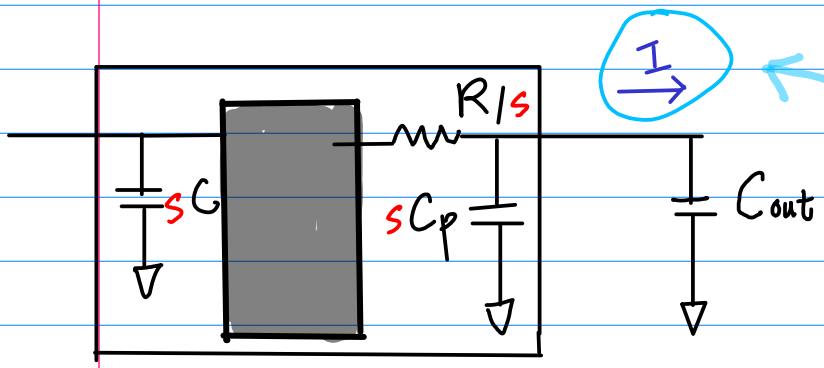
as that of the ref inverter

arbitrary gate



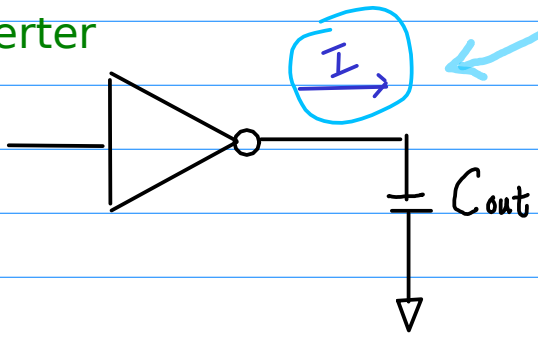
scale S

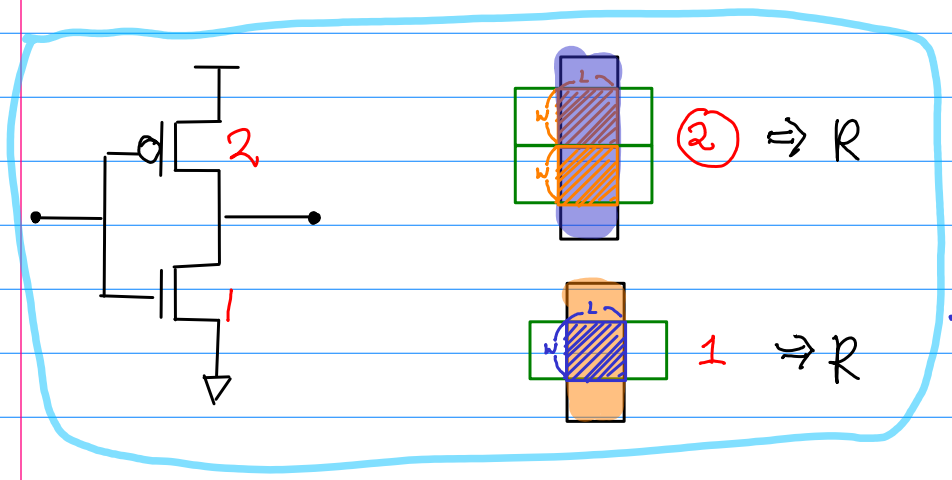
make it bigger by a factor of S



to deliver the same current
as the reference inverter does

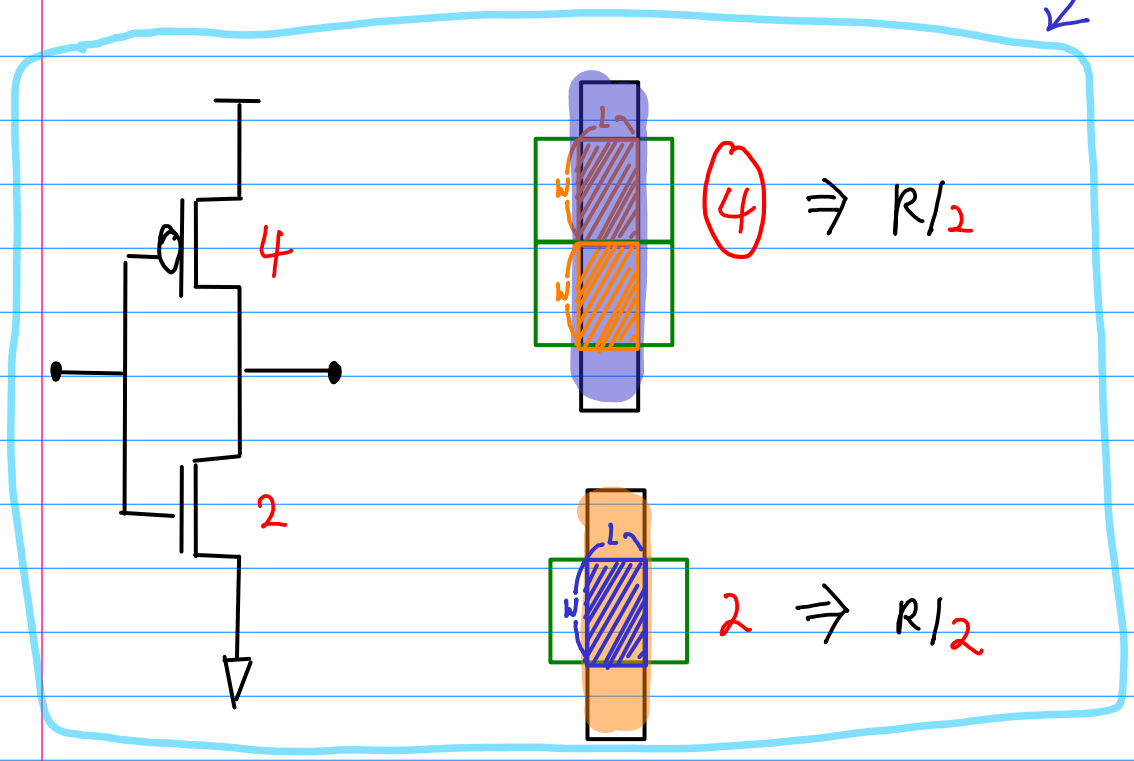
reference
inverter





Scaling Factor

$S = 2$

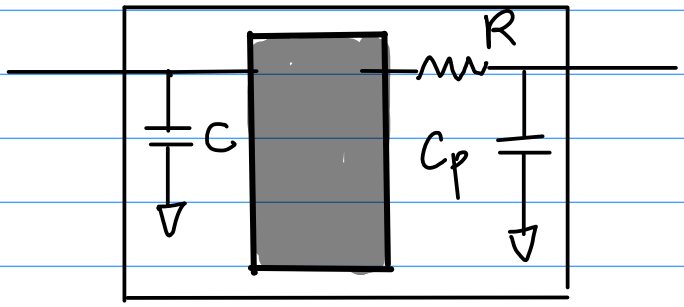


Scaling Effects

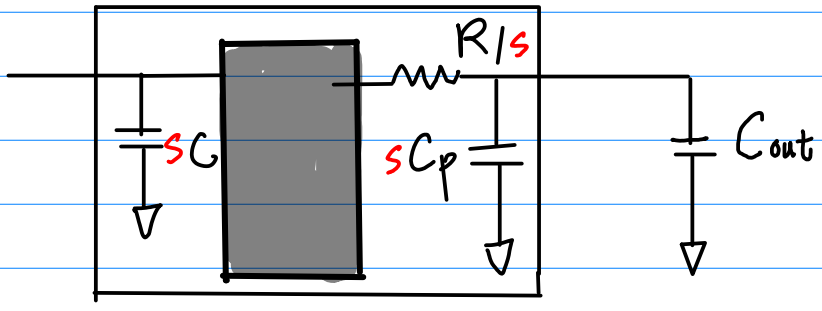
After scaling by S

	R	→	$\frac{R}{S}$
gate	C	→	SC
parasitic	C_p	→	SC_p

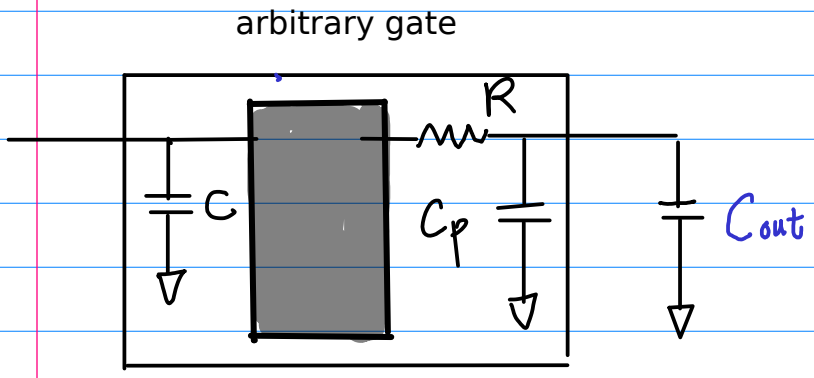
arbitrary gate



scale (S)



delay proportional to time constant



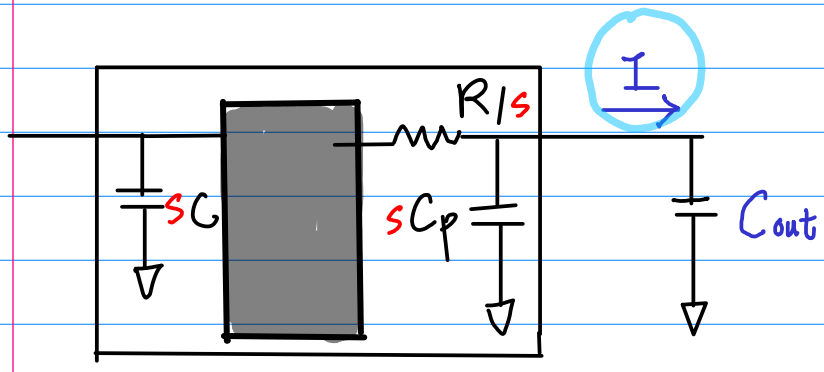
$delay \propto RC$

$R = R$

$C = (C_p + C_{out})$

scale (s)

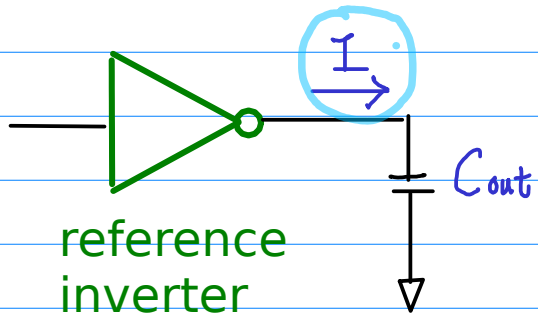
to get the same I



$delay \propto R'C'$

$R' = R/s$

$C' = (sC_p + C_{out})$



=

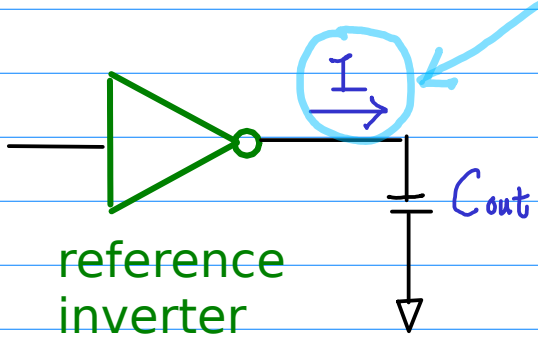
$$d \propto R C_p + R C_{out} = R(C_p + C_{out})$$

scale (s)

to get the same (I)

(make it bigger)

$$d \propto R C_p + \frac{R}{s} C_{out} = \frac{R}{s}(s C_p + C_{out})$$



* Scaling Effects

actual input C → scaled input C_{in}

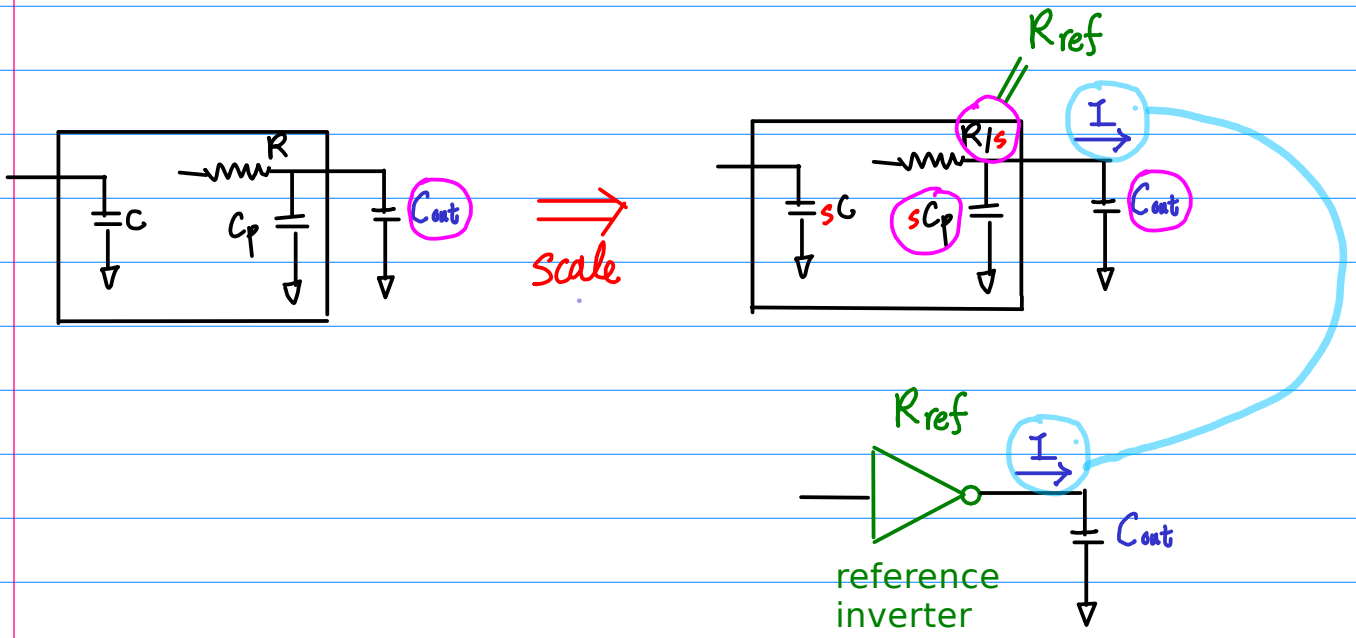
actual output R → scaled output R_{ref}

$C_{in} = sC$

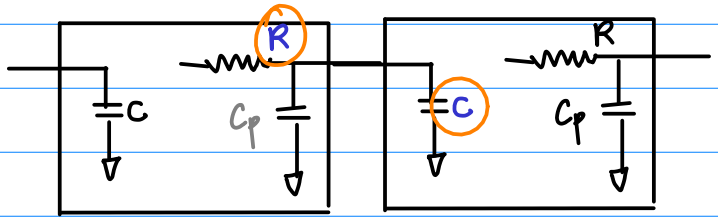
$R_{ref} = R/s$

increased C → sC

decreased R → R/s

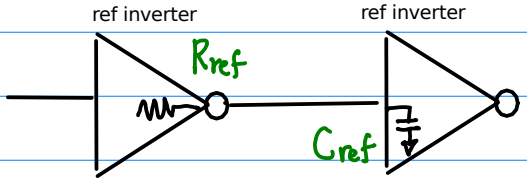


✳ Some time constants



series connection of the same gate under consideration

$$\tau = RC \qquad C_p \ll C$$



series connection of the ref inverter

$$\tau_{ref} = R_{ref} C_{ref} \qquad C_p \ll C_{ref}$$

Logical Effort

Logical Effort (g) of a gate

the **ratio** of the **input cap** of the scaled gate
to the **input cap** of the ref inverter

the gate is scaled to give the same output current
as the ref inverter's output current

$$g = \frac{C_{in}}{C_{ref}}$$

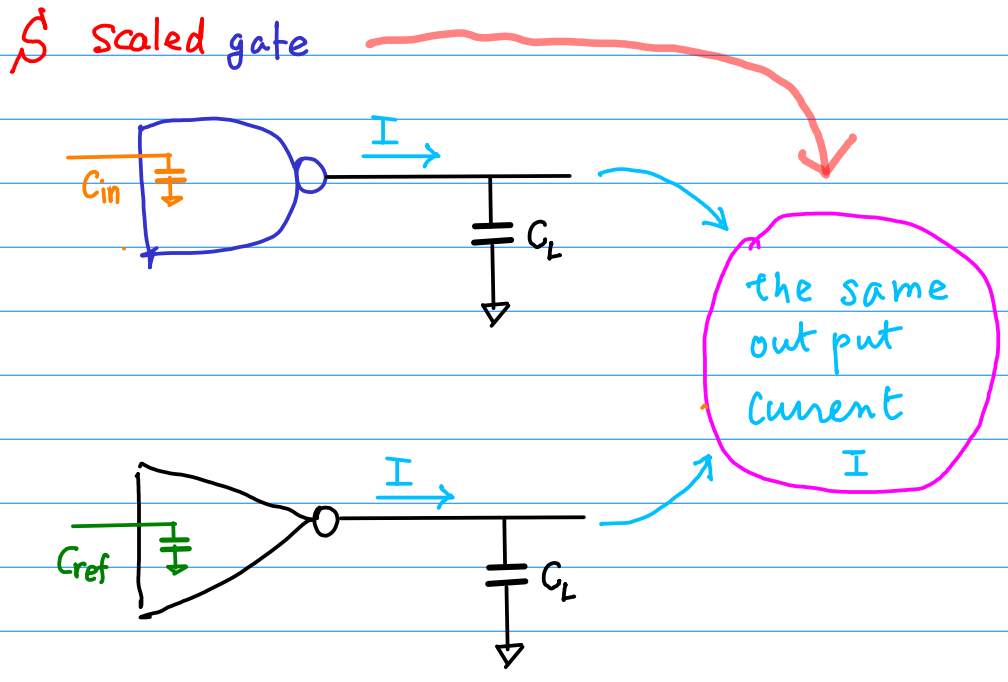
C_{in} after scaling
in order to make its output current
the same as the ref inverter's output current

① Scaling information (how much bigger)

$$g = \frac{C_{in}}{C_{ref}}$$ Logical Effort

the input capacitance ratio
to deliver the same output current
of the reference gate

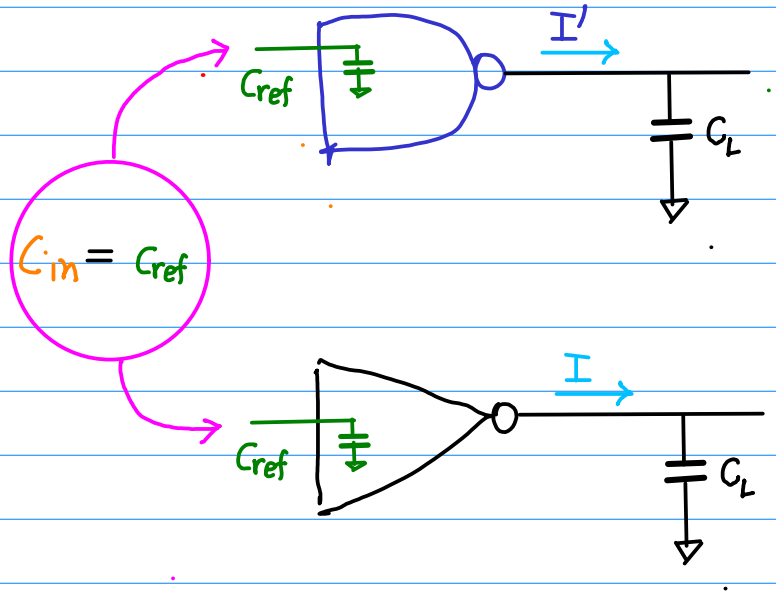
this ratio gives scaling information
about how much **bigger** the gate should be
to deliver the same output current
of the reference gate



② output drive reduction (how much worse)

how much **worse** a gate
at producing output current
as compared to an inverter

given that
each input of the gate may have
as much input capacitance as the inverter



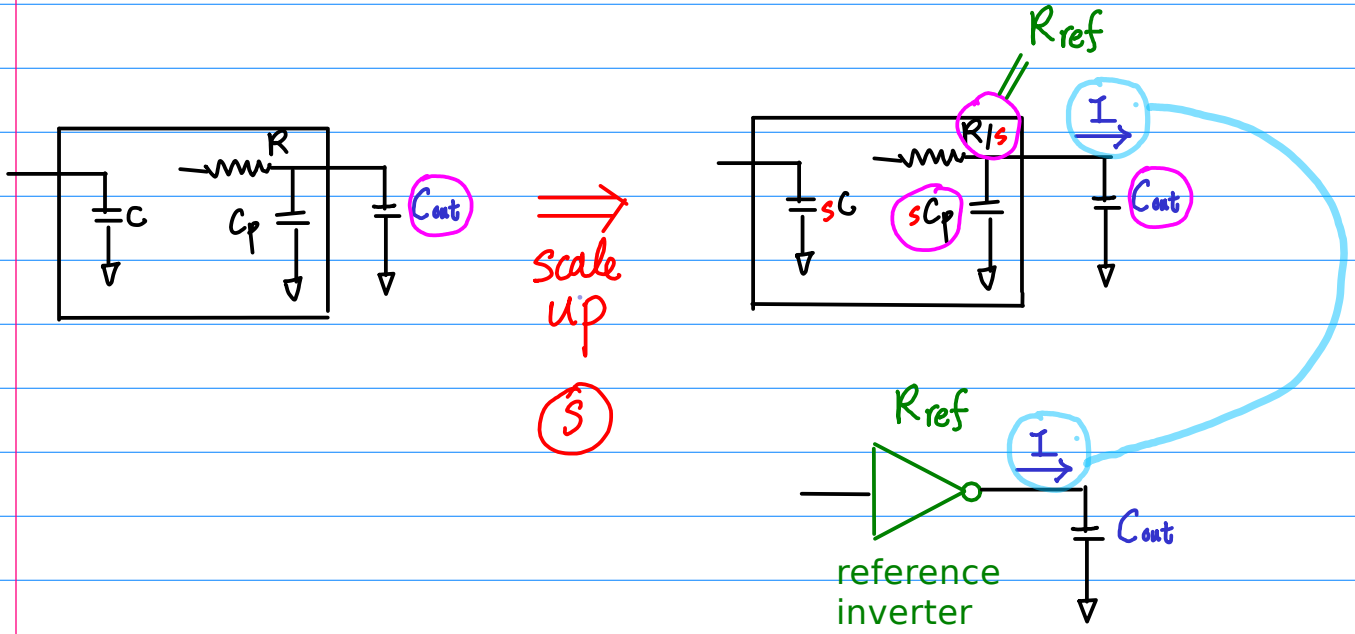
Resistive figure

$\frac{I}{I'}$

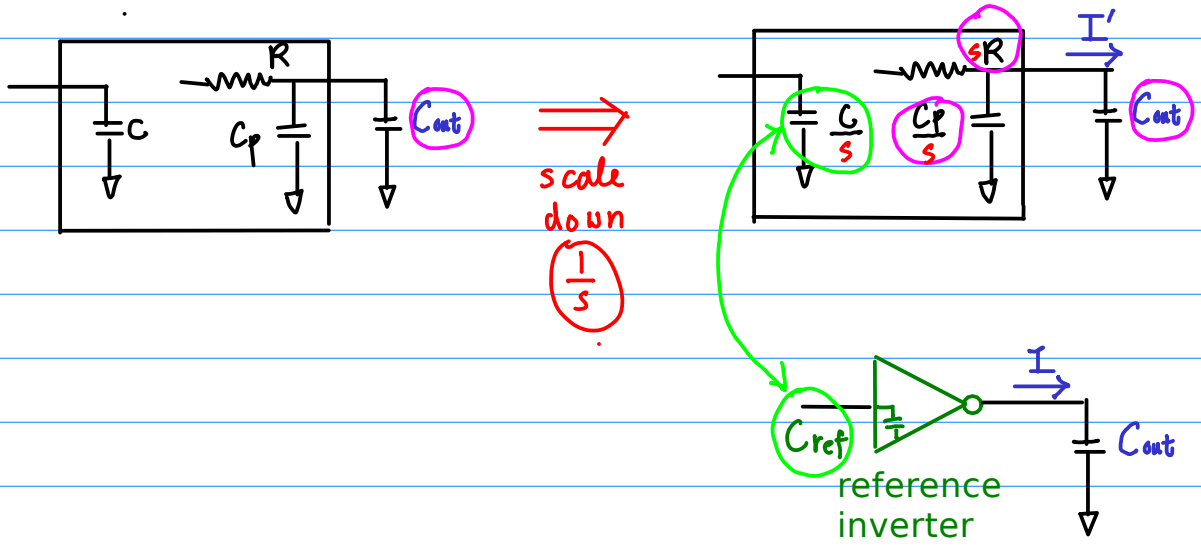
how worse

★ g : output drive reduction
when input cap sized same as inverter

① Scaling information (how much bigger)



② output drive reduction (how much worse)

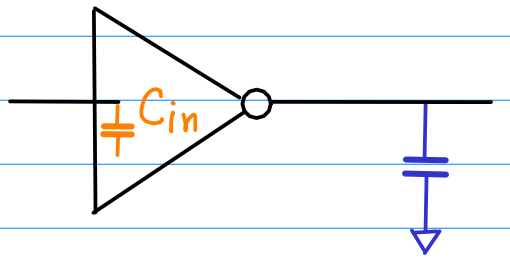


Electrical Effort

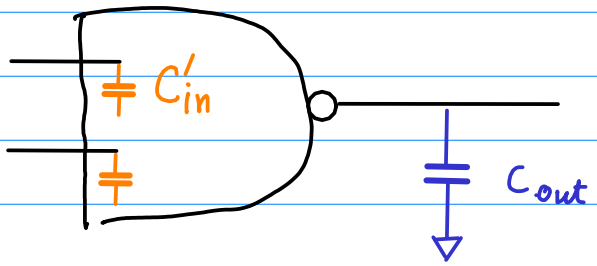
Electrical Effort : the output & input cap ratio

$$h = \frac{C_{out}}{C_{in}}$$

the ratio of the drive strength to drive C_{out} to the drive strength to drive its own capacitance C_{in}



an inverter is driving C_{out}

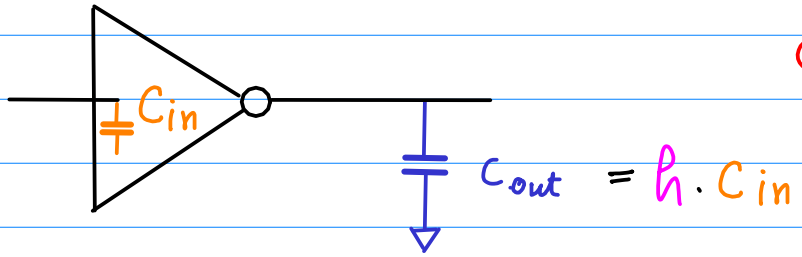


a NAND is driving C_{out}

C_{out} is h times larger than C_{in}

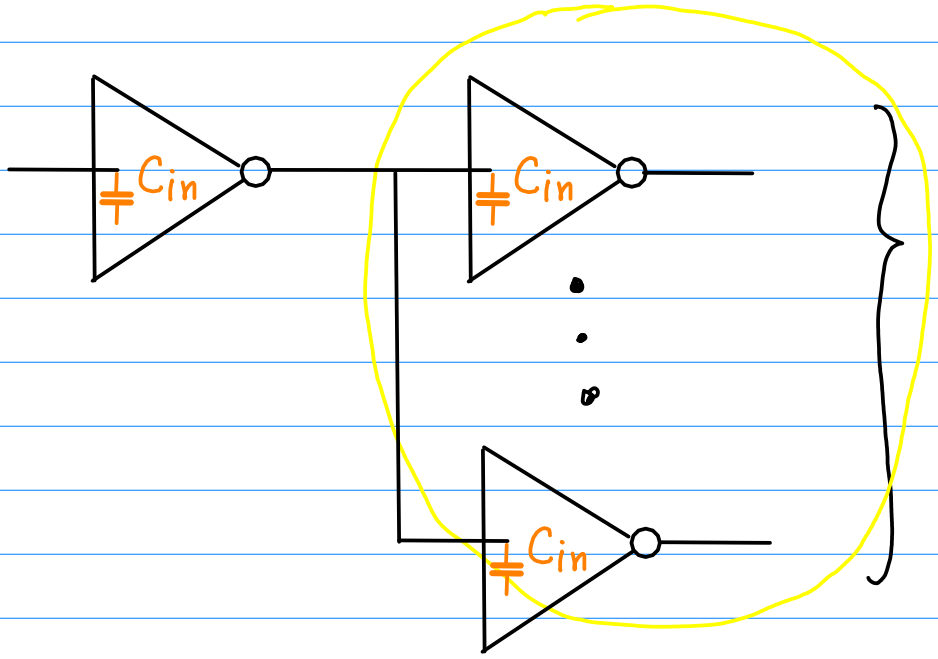
$$h = \frac{C_{out}}{C_{in}}$$

C_{out} is h times larger than C_{in}



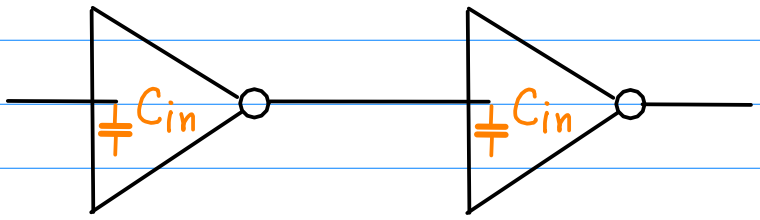
electrical effort h

h copies of the same gate

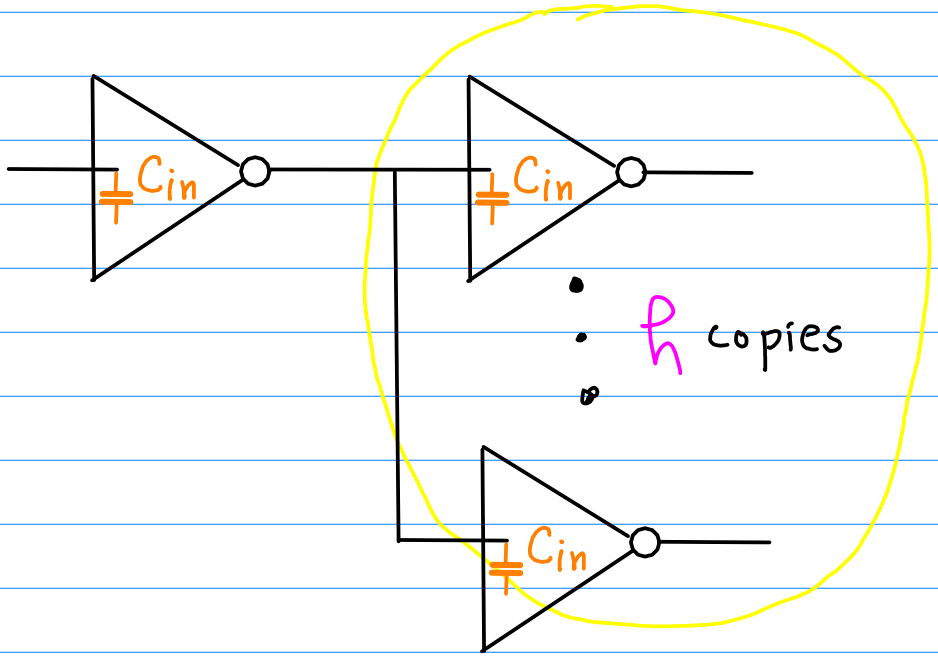


time constant hz

$h \cdot C_{in}$

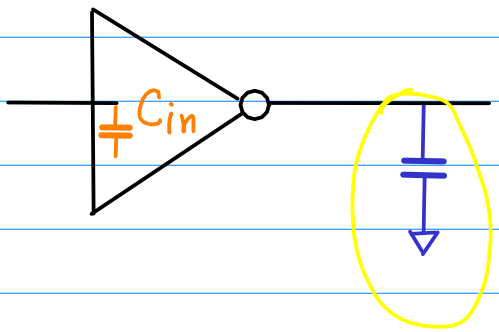


assume
time constant τ



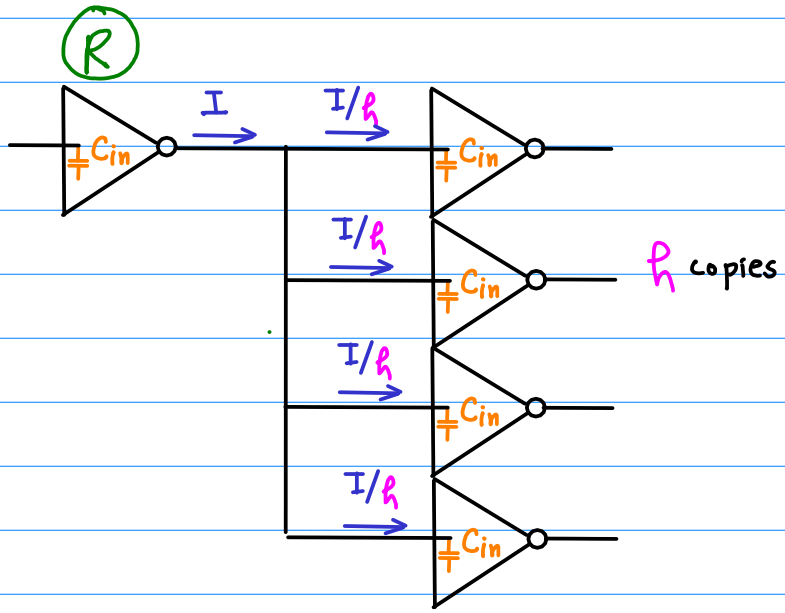
time
constant $h\tau$

$h \cdot C_{in}$



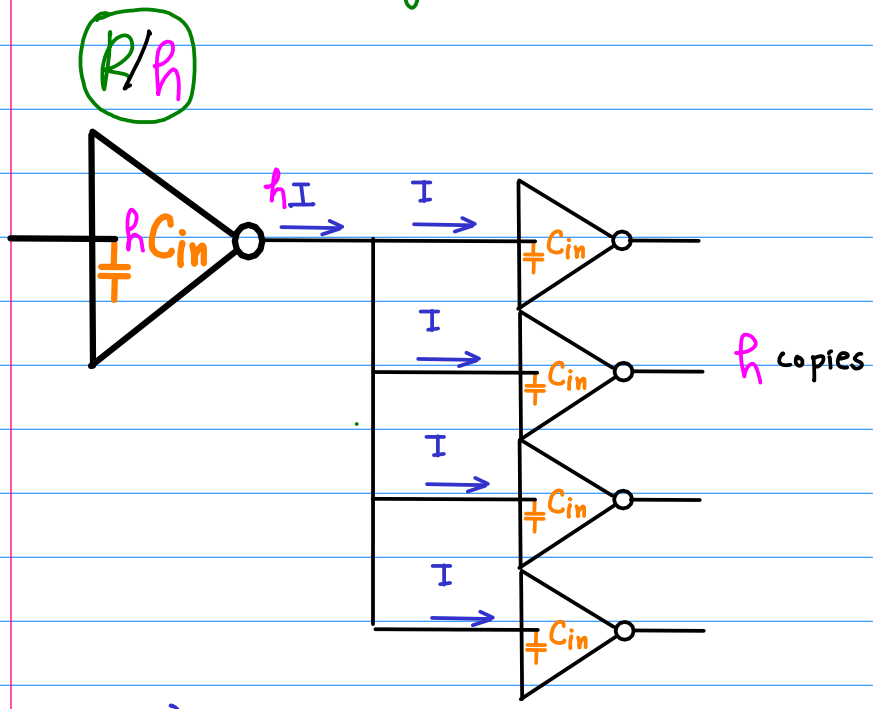
$C_{out} = h \cdot C_{in}$

small drive strength



$R \cdot h\,C_{in} = hz$

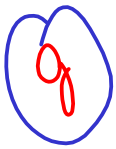
large drive strength



$\frac{R}{h} \cdot h\,C_{in} = z$

Logical Effort: Designing for Speed on the Back of an Envelop

Ivan E. Sutherland
Robert F. Sproull



the logical effort of an inverter is one

how much worse it is than an inverter
at producing output current,
given an equivalent amount of input capacitance

depends mainly on its circuit topology
slightly on the electrical properties

captures the effect of the logic gate's topology
on its ability to produce output current

independent of the size of the transistors

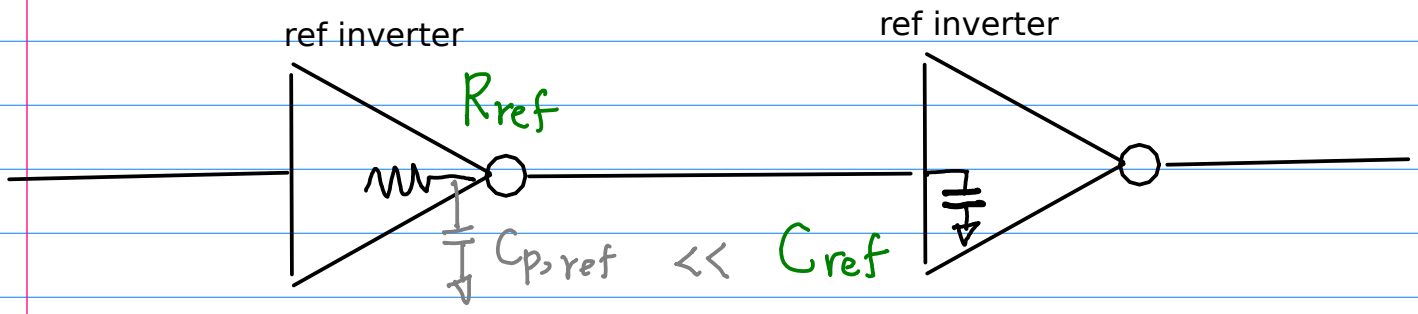
electrical effort describes

how the electrical environment of the logic gate
affects performance and

how the size of the transistors in the gate
determines its load-driving capability

as a ratio of transistor width rather than actual capacitances

Normalized Delay



$$\tau = R_{ref} C_{ref}$$

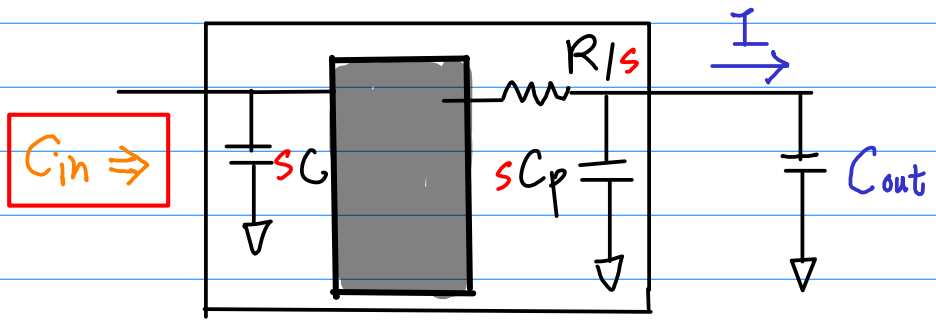
after scaling to get the same I

$$d \propto \frac{R}{S} C_{out} + R C_p$$

$$\frac{d}{\tau} = \frac{d}{R_{ref} C_{ref}} \propto \frac{1}{S} \frac{R C_{out}}{R_{ref} C_{ref}} + \frac{R C_p}{R_{ref} C_{ref}}$$

normalized delay

What is g*h ?



Normalized Delay

$$\frac{d}{R_{ref} C_{ref}} \propto \frac{1}{s}\frac{R C_{out}}{R_{ref} C_{ref}} + \frac{R C_p}{R_{ref} C_{ref}}$$

$$\frac{1}{s}\frac{R C_{in}}{R_{ref} C_{ref}}\left(\frac{C_{out}}{C_{in}}\right)$$

$$= \frac{1}{s}\frac{R}{R_{ref}}\frac{C_{in}}{C_{ref}}\left(\frac{C_{out}}{C_{in}}\right)$$

$$= \left(\frac{C_{in}}{C_{ref}}\right)\left(\frac{C_{out}}{C_{in}}\right)$$

$$= g \cdot h$$

$R_{ref} = R/s$

scale for the same current I

I

Normalized Delay

$$\frac{d}{R_{ref} C_{ref}} \propto \boxed{\frac{1}{s}\frac{R C_{out}}{R_{ref} C_{ref}}} + \frac{R C_p}{R_{ref} C_{ref}}$$

$$\frac{1}{s}\frac{R C_{in}}{R_{ref} C_{ref}}\left(\frac{C_{out}}{C_{in}}\right)$$

$$= \boxed{\frac{1}{s}\frac{R}{R_{ref}}\frac{C_{in}}{C_{ref}}}\left(\frac{C_{out}}{C_{in}}\right)$$

$$= \left(\frac{C_{in}}{C_{ref}}\right)\left(\frac{C_{out}}{C_{in}}\right)$$

$$= g \cdot h$$

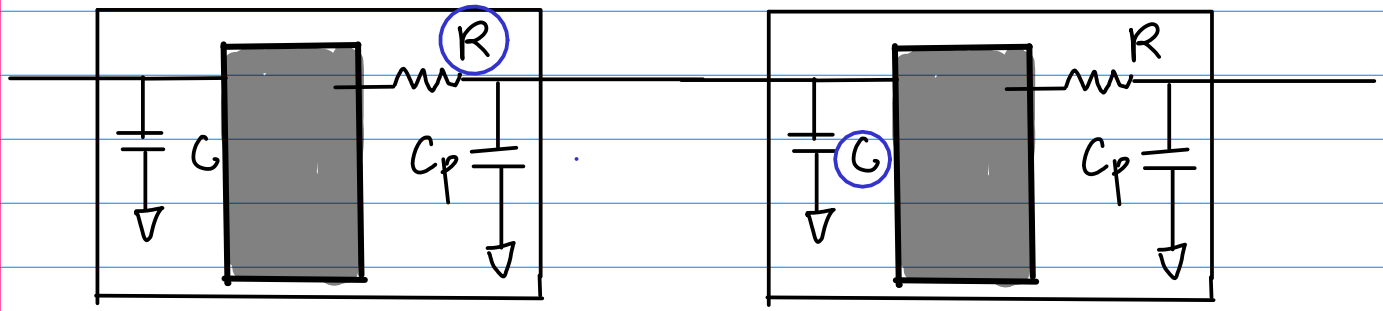
$C_{in} = s\hat{C}$

$$= \boxed{\frac{1}{s}\frac{R\, s\hat{C}}{R_{ref} C_{ref}}}\left(\frac{C_{out}}{C_{in}}\right)$$

$$= \left(\frac{RC}{R_{ref} C_{ref}}\right)\left(\frac{C_{out}}{C_{in}}\right)$$

$$= \left(\frac{\tau}{\tau_{ref}}\right)\left(\frac{C_{out}}{C_{in}}\right)$$

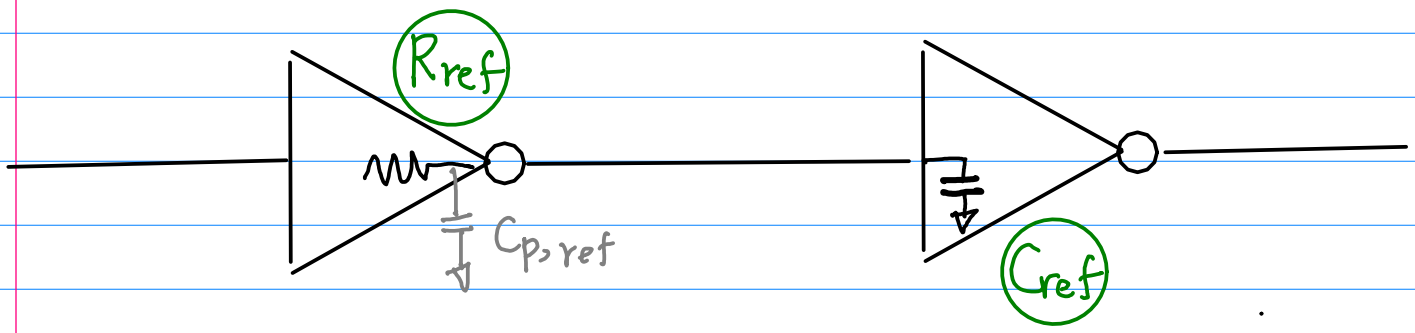
arbitrary gate without scaling



$$\tau = R C$$

time constant
before scaling by S

ref inverter



$C_{p,ref} << C_{ref}$

ideal inverter :
no parasitic delay

$$\tau_{ref} = R_{ref} C_{ref}$$

The 1st component of the normalized delay

$$g \cdot h = \left(\frac{C_{in}}{C_{ref}}\right)\left(\frac{C_{out}}{C_{in}}\right)$$

$$= \left(\frac{\tau}{\tau_{ref}}\right)\left(\frac{C_{out}}{C_{in}}\right)$$

$$= \left(\frac{C_{out}}{C_{ref}}\right)$$

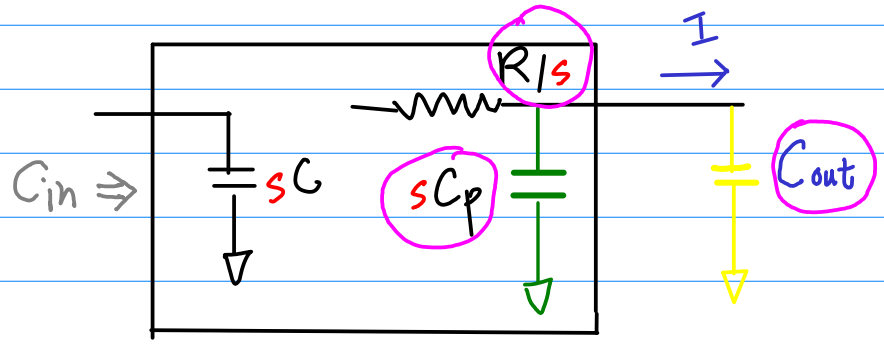
$$\Downarrow$$

$$\frac{d}{R_{ref} C_{ref}} \propto \frac{1}{s}\frac{R C_{out}}{R_{ref} C_{ref}} + \frac{R C_p}{R_{ref} C_{ref}}$$

What is p ?

parasitic delay (p)

- delay due to internal parasitic capacitance sC_p
- excluding external load cap C_{out}
- count only diffusion capacitance of the output
- delay without output load



$R/s \;\; sC_p = RC_p$

* Scaling Effects revisited

$C_{in} = sC$

$R_{ref} = R/s$

scale for the same current I

$C_{p,ref} = sC_p$

internal parasitic cap : diffusion cap of the output node

after scaling

input : $C \rightarrow sC$ ↑

output : $R \rightarrow R/s$ ↓

output : $C_p \rightarrow sC_p$ ↑

$RC_p = \frac{1}{s} R \cdot sC_p$

no change

Normalized Delay

$$\frac{d}{R_{ref} C_{ref}} \propto \frac{1}{s}\frac{R C_{out}}{R_{ref} C_{ref}} + \frac{R C_p}{R_{ref} C_{ref}}$$

$$\frac{1}{s}\frac{R\, sC_p}{R_{ref}\, C_{ref}}$$

$$= \frac{1}{s}\frac{R}{R_{ref}}\left(\frac{C_{p,ref}}{C_{ref}}\right)$$

$C_{in} = sC$

$R_{ref} = R/s$

scale for the same current I

$C_{p,ref} = sC_p$

$$\left(\frac{\text{internal diffusion cap}}{\text{gate cap of ref inv}}\right) = \left(\frac{C_{p,ref}}{C_{ref}}\right)$$

$$\approx p$$

Normalized Delay

$$\frac{d}{R_{ref} C_{ref}} \propto \frac{1}{s} \frac{R C_{out}}{R_{ref} C_{ref}} + \frac{R C_p}{R_{ref} C_{ref}}$$

$$\frac{1}{s} \frac{R s C_p}{R_{ref} C_{ref}}$$

$$= \frac{1}{s} \frac{R}{R_{ref}} \left(\frac{C_{p,ref}}{C_{ref}} \right)$$

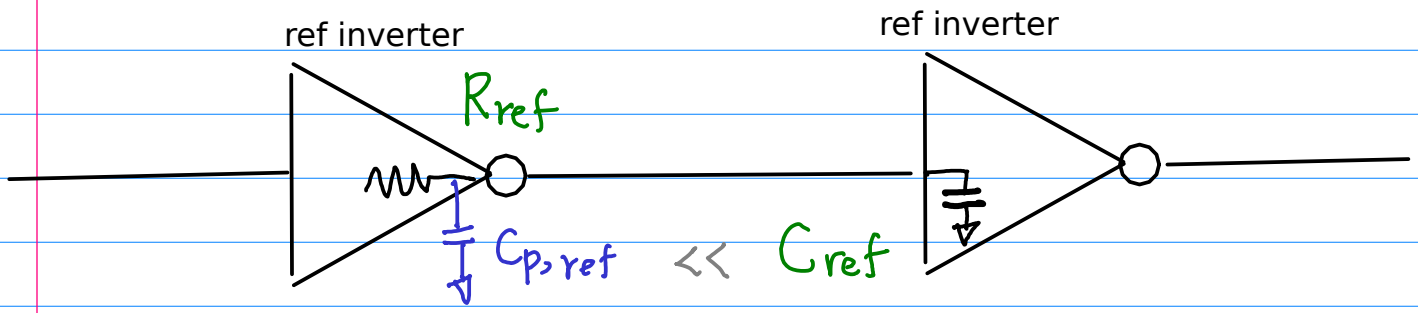
$$\left(\frac{\text{internal diffusion cap}}{\text{gate cap of ref inv}} \right) = \left(\frac{C_{p,ref}}{C_{ref}} \right)$$

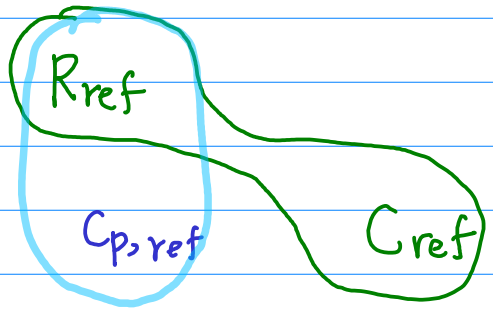
$$= p$$

$$= \frac{R C_p}{R_{ref} C_{ref}}$$

internal diff cap

$$\left(\frac{\text{RC value of a gate}}{\text{RC value of ref inv}} \right) = \frac{\tau_{par}}{\tau_{ref}}$$



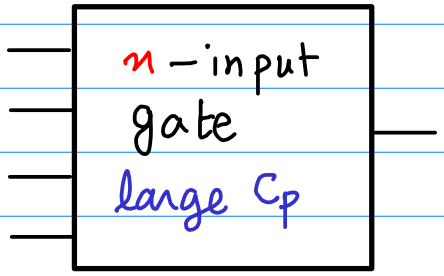


$$\tau_{par} = R_{ref} C_{p,ref}$$

$$\tau_{ref} = R_{ref} C_{ref}$$

$$p = \frac{\tau_{par}}{\tau_{ref}}$$

$$p_{ref} = 1$$



$$\eta\, p_{ref} = \eta$$

The 2nd component of the normalized delay

$$p = \frac{R C_p}{R_{ref} C_{ref}}$$

$$= \left(\frac{C_{p,ref}}{C_{ref}}\right) = \left(\frac{\text{internal diffusion cap.}}{\text{gate cap of ref inv}}\right)$$

$$= \frac{\tau_{par}}{\tau_{ref}} = \left(\frac{\text{RC value of a gate}}{\text{RC value of ref inv}}\right)$$

internal diff cap only

$$\frac{d}{R_{ref} C_{ref}} \propto \frac{1}{S} \frac{R C_{out}}{R_{ref} C_{ref}} + \boxed{\frac{R C_p}{R_{ref} C_{ref}}}$$

$$\frac{d}{R_{ref} C_{ref}} \propto \frac{1}{5}\frac{R C_{out}}{R_{ref} C_{ref}} + \frac{R C_p}{R_{ref} C_{ref}}$$

$$= g \cdot h + p$$

$$g \cdot h = \left(\frac{C_{in}}{C_{ref}}\right)\left(\frac{C_{out}}{C_{in}}\right)$$

$$= \left(\frac{\tau}{\tau_{ref}}\right)\left(\frac{C_{out}}{C_{in}}\right)$$

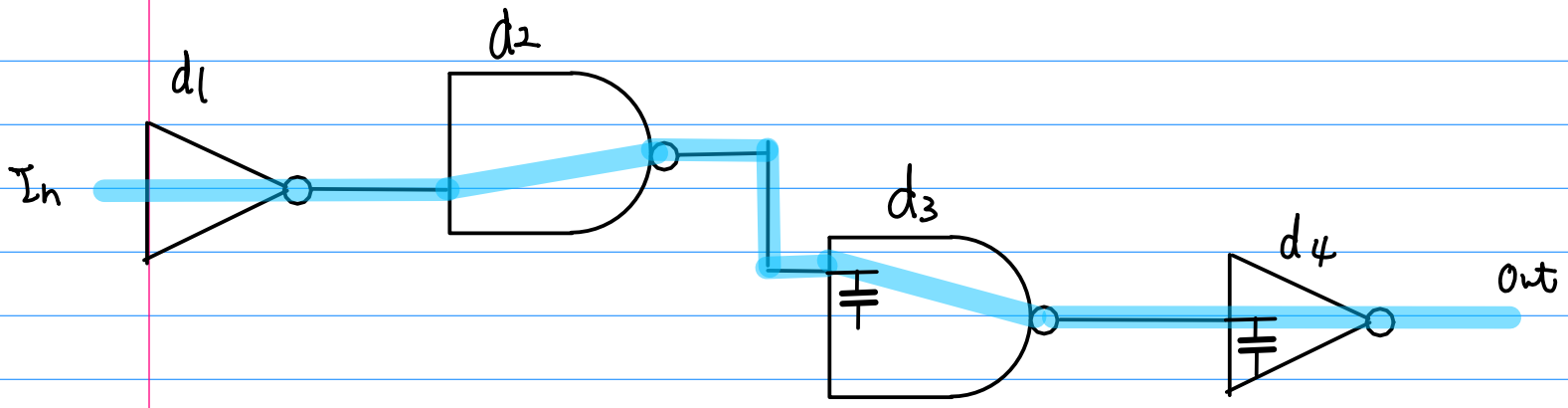
$$= \left(\frac{C_{out}}{C_{ref}}\right)$$

$$p = \frac{R C_p}{R_{ref} C_{ref}}$$

$$= \frac{\tau_{par}}{\tau_{ref}}$$

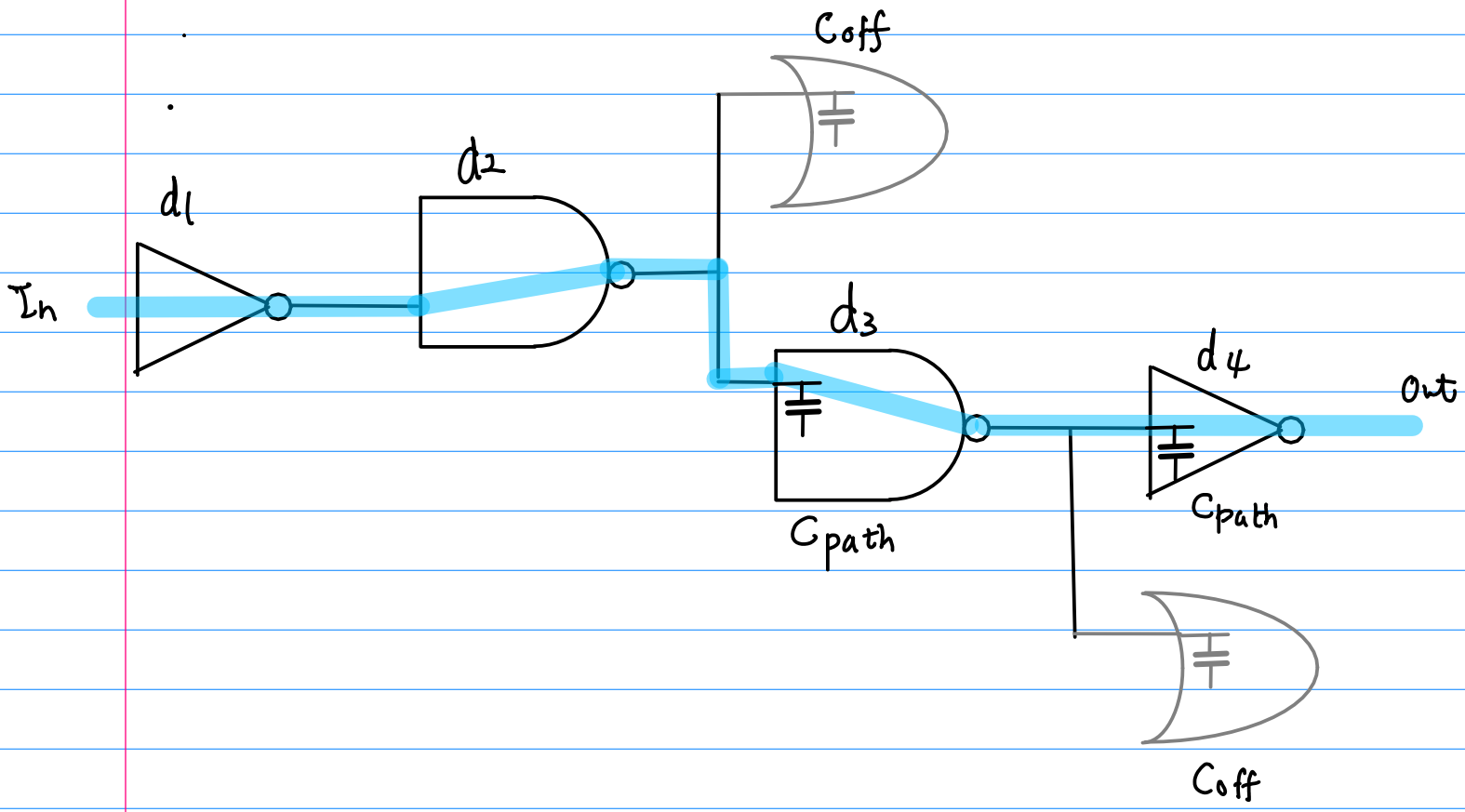
$$= \left(\frac{C_{p,ref}}{C_{ref}}\right)$$

Path Delay



$$\sum d_i = d_1 + d_2 + d_3 + d_4$$

Branch Effect



$$b_3 = \frac{C_{path} + C_{off}}{C_{path}} \qquad b_4 = \frac{C_{path} + C_{off}}{C_{path}}$$

gate capacitance that are not in the path but contribute to path delay

$$\boxed{b > 1}$$

all capacitance contributions that are off the main path

Path Branch Effort $B = \prod b_i$

Path Delay

$$d = gh + p$$

$$d_i = g_i h_i + p_i$$

Total Path Delay

$$D = \sum d_i = \sum (g_i h_i + p_i)$$

Path Logical Effort

$$G = g_1 \cdot g_2 \cdots g_N$$

Path Electrical Effort

$$H = h_1 \cdot h_2 \cdots h_N$$

Path Effort

$$F = GH = (g_1 h_1)(g_2 h_2) \cdots (g_N h_N)$$
$$= f_1 f_2 \cdots f_N$$

$$f_i = g_i \cdot h_i$$

$$d = d_1 + d_2 + \cdots + d_N$$

$$= (g_1 h_1 + P_1) + (g_2 h_2 + P) + \cdots + (g_N h_N + P_N)$$

$$= (g_1 h_1 + g_2 h_2 + \cdots + g_N h_N) + (P_1 + P_2 + \cdots + P_N) = (f_1 + f_2 + \cdots + f_N) + P$$

$$\geq N \sqrt[N]{(g_1 h_1)(g_2 h_2) \cdots (g_N h_N)} + P = N \sqrt[N]{f_1 \cdot f_2 \cdots f_N} + P$$

minimum when $f_1 = f_2 = \cdots = f_N = \hat{f}$

$g_i h_i = \hat{f}$ constant

$$d = (g_1h_1 + g_2h_2 + \cdots + g_Nh_N) + (p_1 + p_2 + \cdots + p_N)$$

$$= (f_1 + f_2 + \cdots + f_N) + P$$

$$\geq N\sqrt[N]{(g_1h_1)(g_2h_2)\cdots(g_Nh_N)} + P$$

$$= N\sqrt[N]{f_1 \cdot f_2 \cdots f_N} + P$$

$$F = f_1 \cdot f_2 \cdots f_N$$
$$G = g_1 \cdot g_2 \cdots g_N$$
$$H = h_1 \cdot h_2 \cdots h_N \qquad P = p_1 + p_2 + \cdots + p_N$$

$$F = G \cdot H$$

$$d \geq N\sqrt[N]{F} + P$$

minimum when $\forall i \quad g_i h_i = f = \sqrt[N]{F} = \sqrt[N]{GH}$

$$D = \sum d_i = \sum (g_i h_i + p_i)$$

$$\geq N F^{\frac{1}{N}} + P$$

$$P = \sum p_i$$

$$h_i = \frac{f}{g_i}$$

$P = \sum p_i$ sum of parasitic delay

Logical Effort	$g = \frac{C_{in}}{C_{ref}}$	$G = \prod g_i$
Electrical Effort	$h = \frac{C_{out}}{C_{in}}$	$H = \frac{C_{out\ (path)}}{C_{in\ (path)}}$
Branching Effort	X	$B = \prod b_i$
Effort	$f = gh$	$F = GBH$
Effort Delay	f	$N F^{\frac{1}{N}}$
# of Stages	1	N
parasitic delay	p	$P = \sum p_i$
delay	$f + p$	$N F^{\frac{1}{N}} + P$