# CMOS Delay-1 (H.1)
# Transistor Sizing

20160905

Based on

Uyemura
Introduction to VLSI Circuits and Systems

Weste
CMOS VLSI Design

# Logical Effort Techniqus

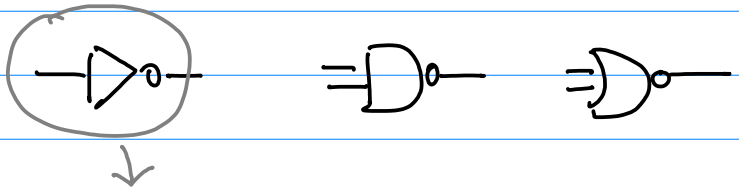
shows how many stages of logic are required
for the fastest implementation
of any given logic function

Scaling of logic cascades
Characterize logic gates & their interaction
to provide techniques to minimize the delay

<High speed chains>

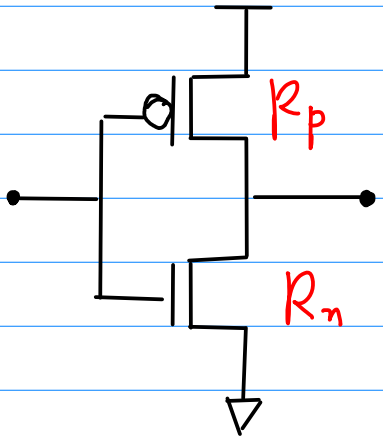
# reference gate

which gate?



an inverter

What kind of inverters?

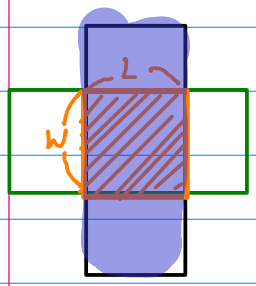



a **Symmetric** inverter

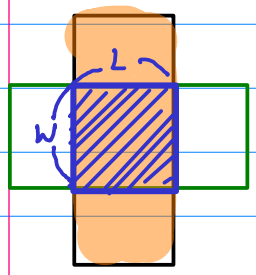
$R_n = R_p$

$\beta_n = \beta_p$

# Unit nMOS, pMOS




a unit pMOS
with minimum size
min W & min L




a unit nMOS
with minimum size
min W & min L

| | $V_{DD} = 5V$ | $V_{DD} = 3.3V$ |
|---|---|---|
| $R_{n,unit}$ | 3.9 kΩ | 6.8 kΩ |
| $R_{p,unit}$ | 14 kΩ | 25 kΩ |

a unit nMOS effective resistance (R)

a unit pMOS effective resistance (2R)

$$\begin{cases} R_p = 2R_n \\ \beta_n = 2\beta_p \end{cases} \qquad \begin{cases} R_p = 3R_n \\ \beta_n = 3\beta_p \end{cases}$$

# Transconductance

$$\frac{\beta_n}{\beta_p} = \frac{k_n' \left(\frac{W}{L}\right)_n}{k_p' \left(\frac{W}{L}\right)_p}$$

$$\beta \propto \frac{1}{R} \qquad \beta \propto \left(\frac{W}{L}\right) \qquad \beta \propto k.$$

$$\frac{k_n'}{k_p'} = 2 \sim 3$$ different mobility

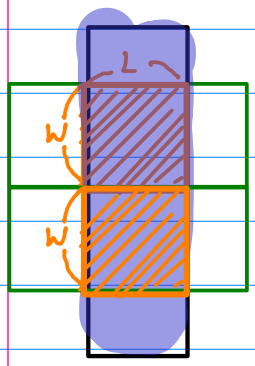
physical property

a unit nMOS
a unit pMOS

$$\frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p} = 1$$

$$\frac{\beta_n}{\beta_p} = \frac{k_n'}{k_p'} = r = 2 \sim 3$$

# the Same resistance $R_p = R_n$



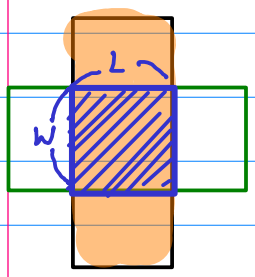

(2) $\rightarrow W_p$

make wider PMOS

to have the same resistance

$R_p$

$\|$




1 $\rightarrow W_n$

$R_n$

$$\frac{\beta_n}{\beta_p} = \frac{k'_n \left(\frac{W}{L}\right)_n}{k'_p \left(\frac{W}{L}\right)_p} = 1$$

process transconductance ratio

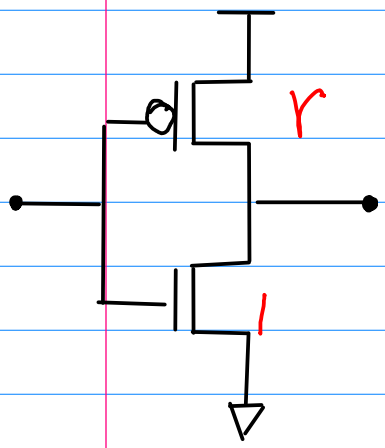
$$r = \boxed{\frac{k'_n}{k'_p}} = \boxed{\frac{\left(\frac{W}{L}\right)_p}{\left(\frac{W}{L}\right)_n}}$$

fixed — adjustable

# aspect ratio for the same (R)

a <u>symmetric</u> inverter

$\beta_n = \beta_p \qquad R_n = R_p$




a relative aspect ratio (r)

$\left(\beta_p\right) = \left(\beta_n\right) \qquad r = 2 \sim 3$

$$\left(\frac{W}{L}\right)_p = r \left(\frac{W}{L}\right)_n$$

$$k_n = r\, k_p$$

for a fixed (L),

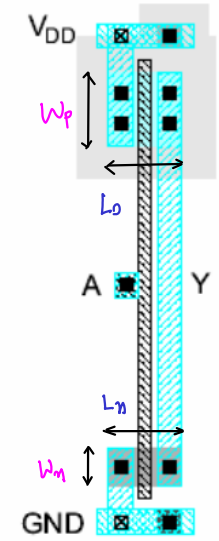
$$W_p = r\, W_n$$

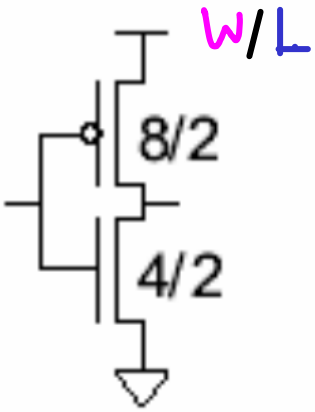
↑ consider a scale factor

# Transistor Dimensions

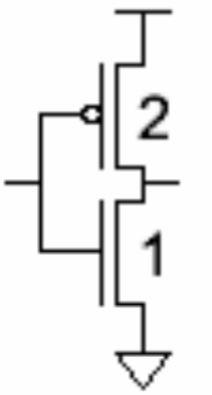
# Inverter Layout

- Transistor dimensions specified as Width / Length
  - Minimum size is 4λ / 2λ, sometimes called 1 unit
  - In *f* = 0.6 μm process, this is 1.2 μm wide, 0.6 μm long




fixed L



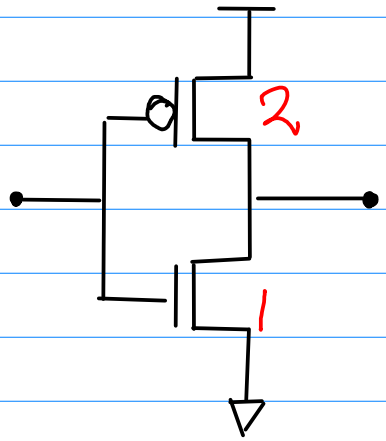
# A Unit Inverter

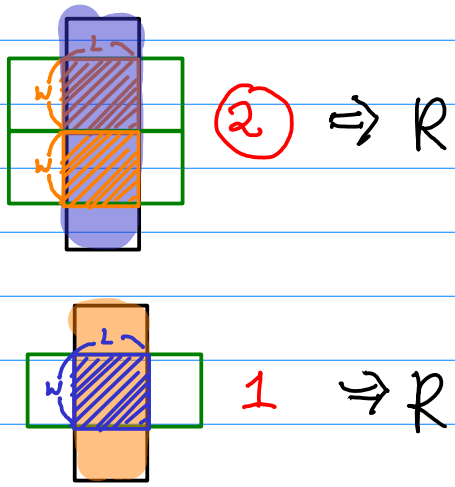
x1 reference gate

a **Symmetric** inverter

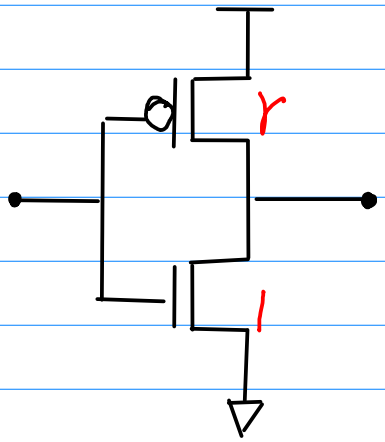
$\beta_n = \beta_p$

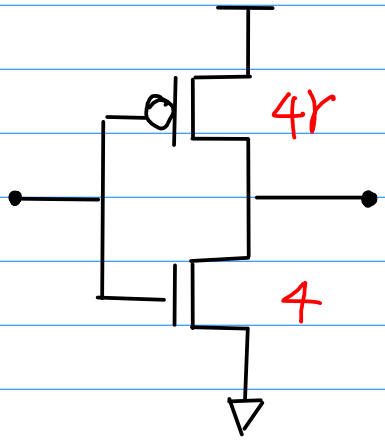
$R_n = R_p$



# Sizing, Scaling




1X ref

4X ref

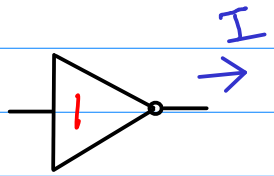
the smallest sizing in the logic chain

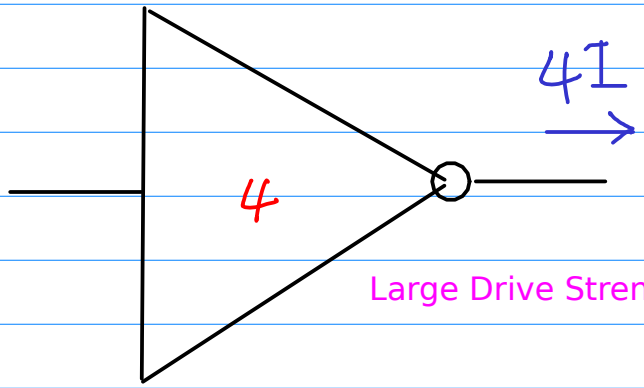
$$\left(\frac{W}{L}\right)_p = r\left(\frac{W}{L}\right)_n$$

$$\left(4\frac{W}{L}\right)_p = r\cdot\left(4\cdot\frac{W}{L}\right)_n$$

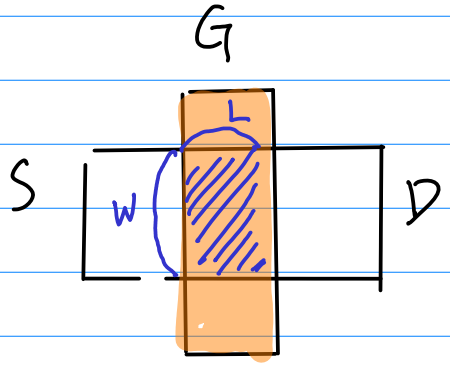
for the same L,

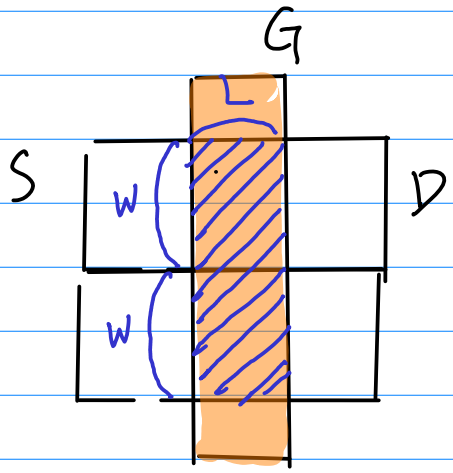
$$\left(\frac{4W}{L}\right)_p = r\cdot\left(\frac{4W}{L}\right)_n$$




Large Drive Strength

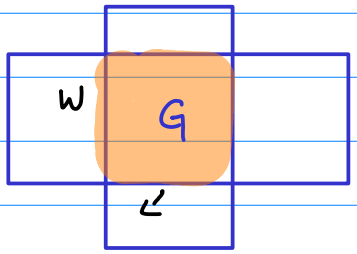


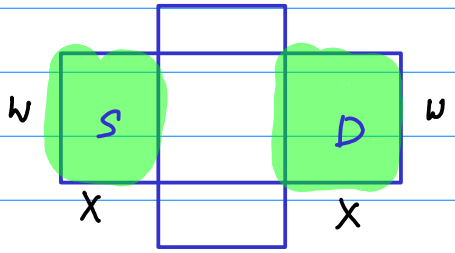

| | | | |
|---|---|---|---|
| physical property | $k_n$ large mobility | $>$ | $k_p$ small mobility |
| design aspect ratio | $\left(\frac{W}{L}\right)_n$ small size | $<$ | $\left(\frac{W}{L}\right)_p = 2\left(\frac{W}{L}\right)_n$ large size |
| trans conductance | $\beta_n$ | $=$ | $\beta_p$ |
| resulting resistance | $R_n$ large resistance | $=$ | $R_p$ small resistance |
| current drive capability | $I_{ds1}$ | $=$ | $I_{ds2}$ |

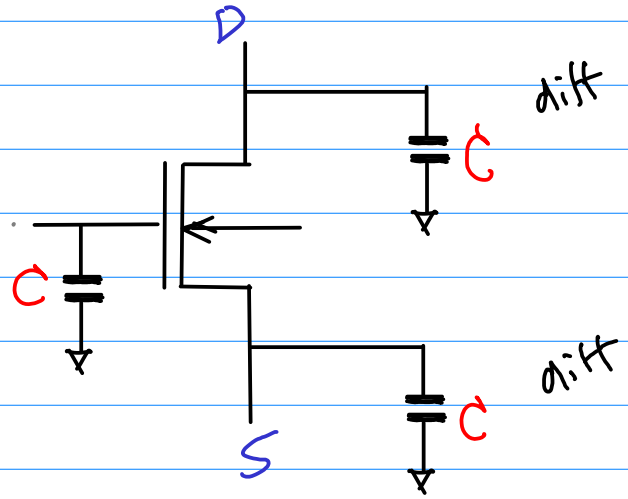
# Capacitance for hand calculations

$C_G = C$




$C_S = C_D = C$




Gate Capacitance

Junction Capacitance (Diffusion, depletion)

$C = C_{GS} + C_{GD}$

$C_G$

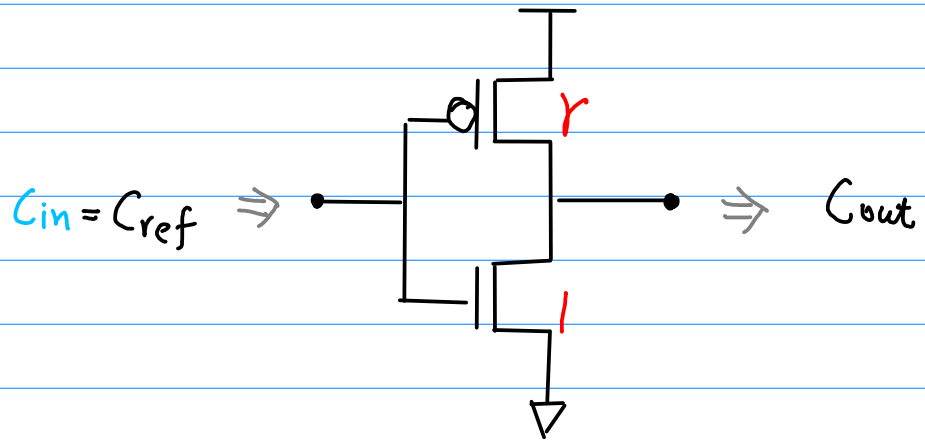
$C_{SB} = C_S$ $= C$

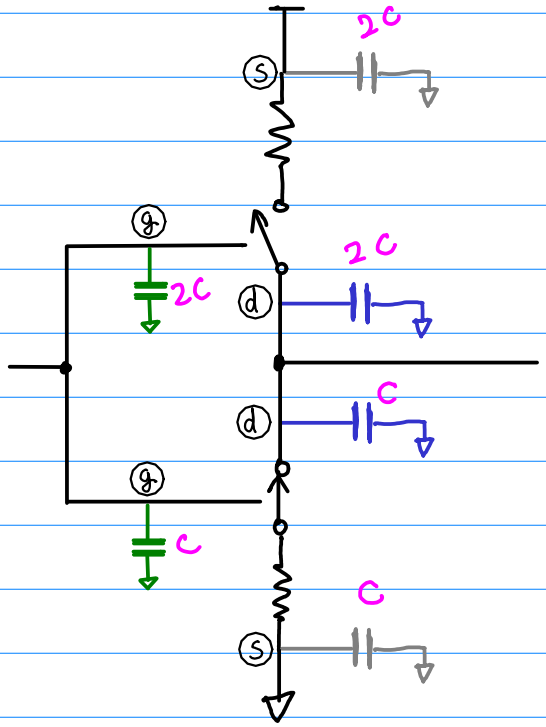
$+$

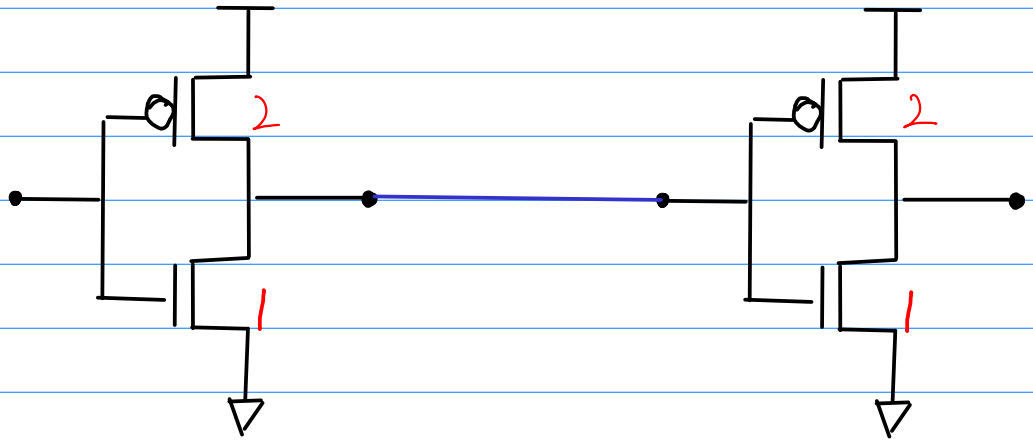
$C_{DB} = C_D$ $= C$

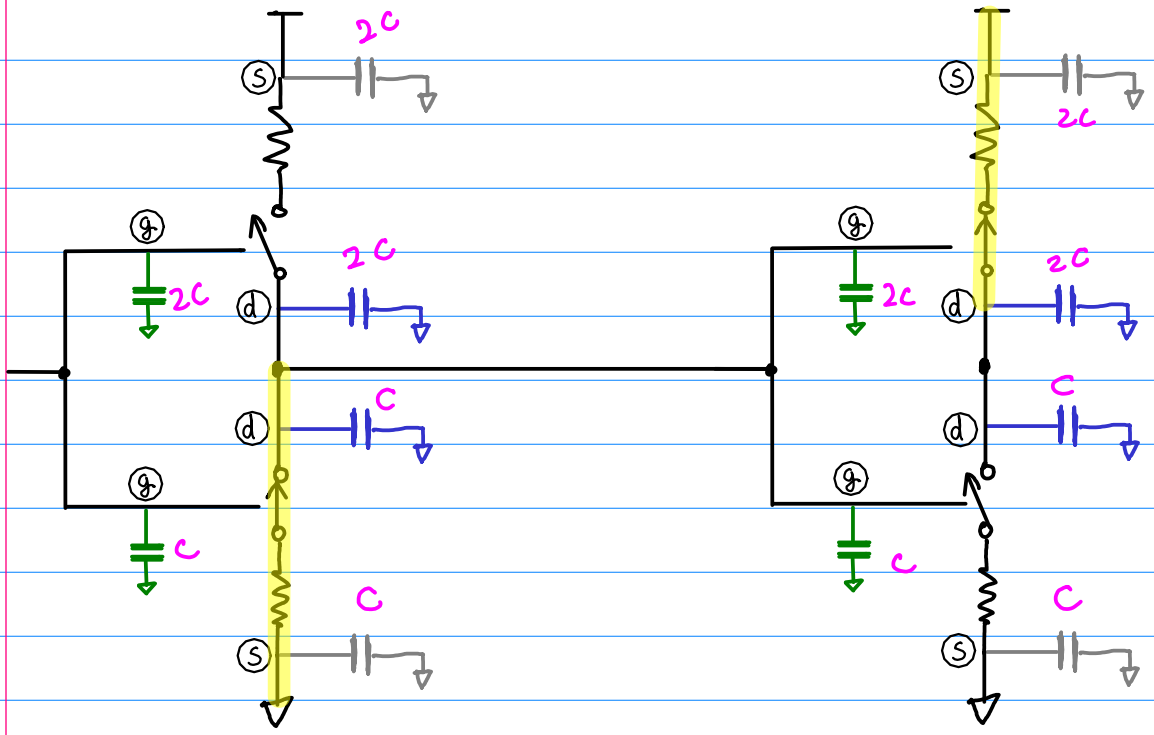
$\| \; C_{diff}$

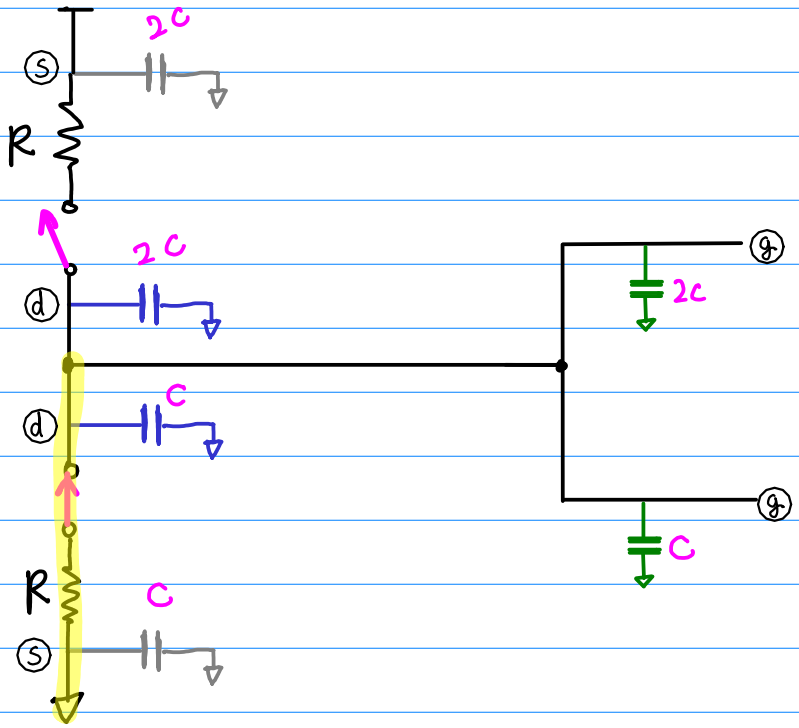
# Equivalent Circuits

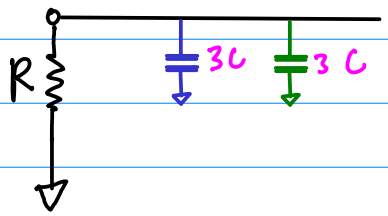


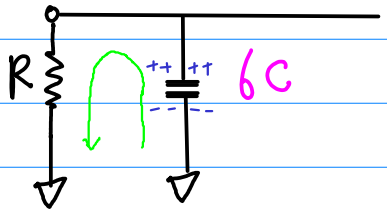



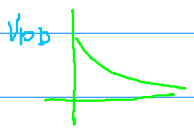

2
1
2
1


2C
S
g
2C
d
2C
C
g
C
S
C
2C
S
2C
g
2C
d
2C
C
g
C
S
C

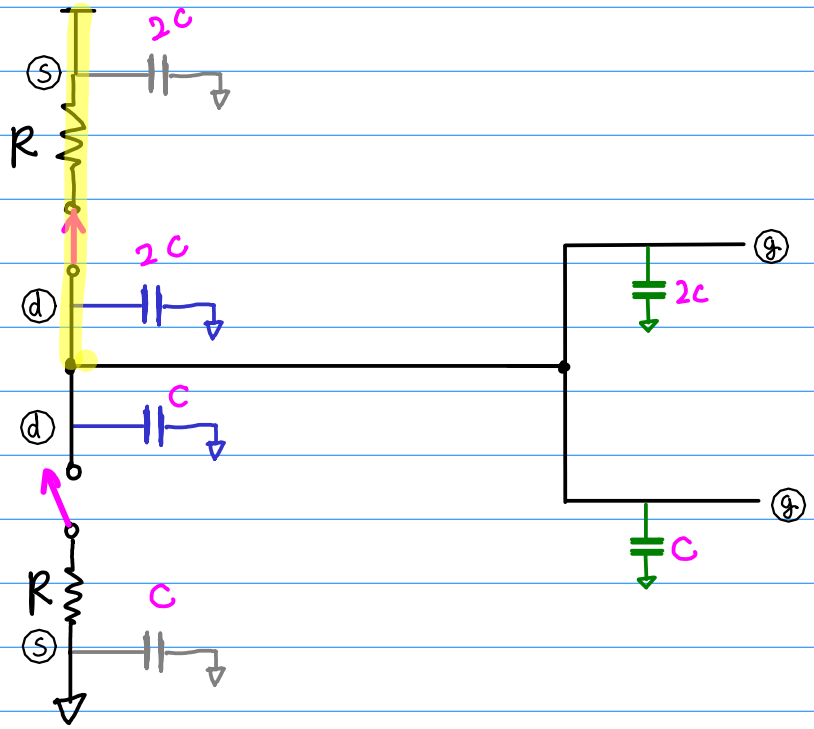


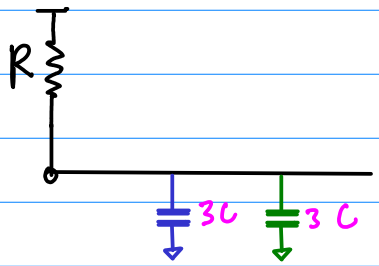



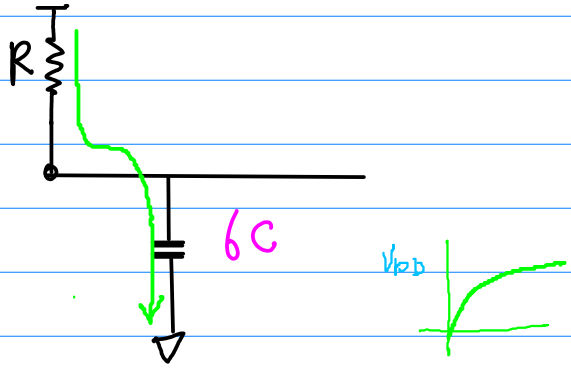



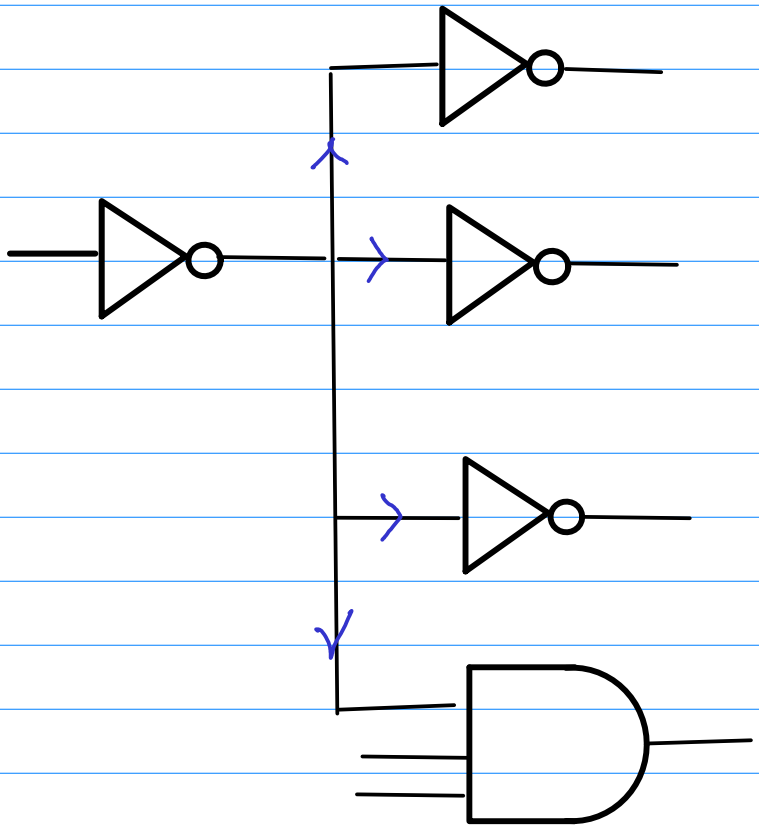

discharge


2C
S
R
2C
d
C
d
R
C
S
2C
g
C
g


R
3C
3C

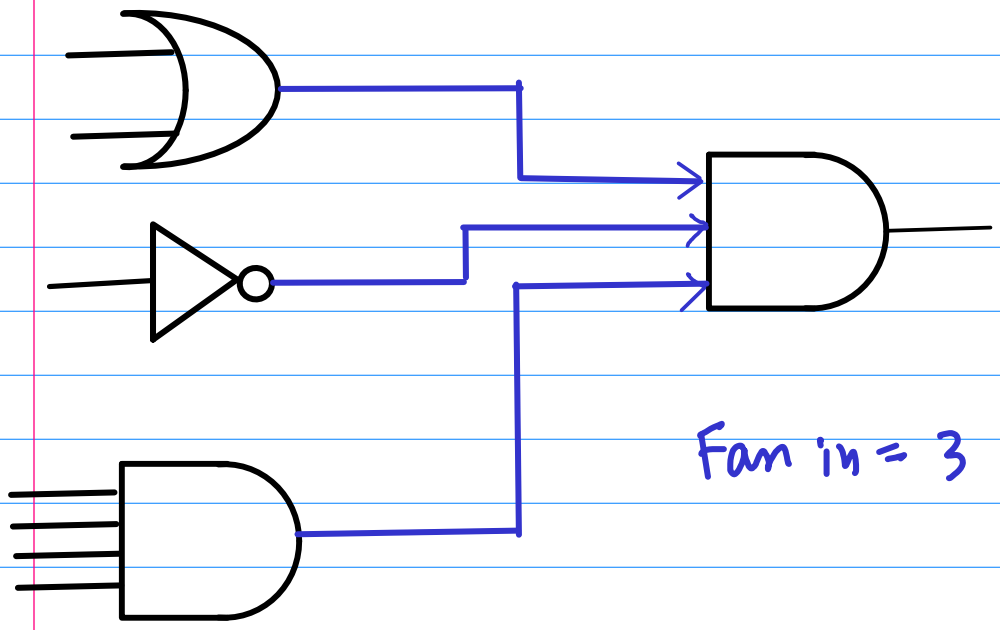

R
6C
Vpp
Charge

# Fan-out

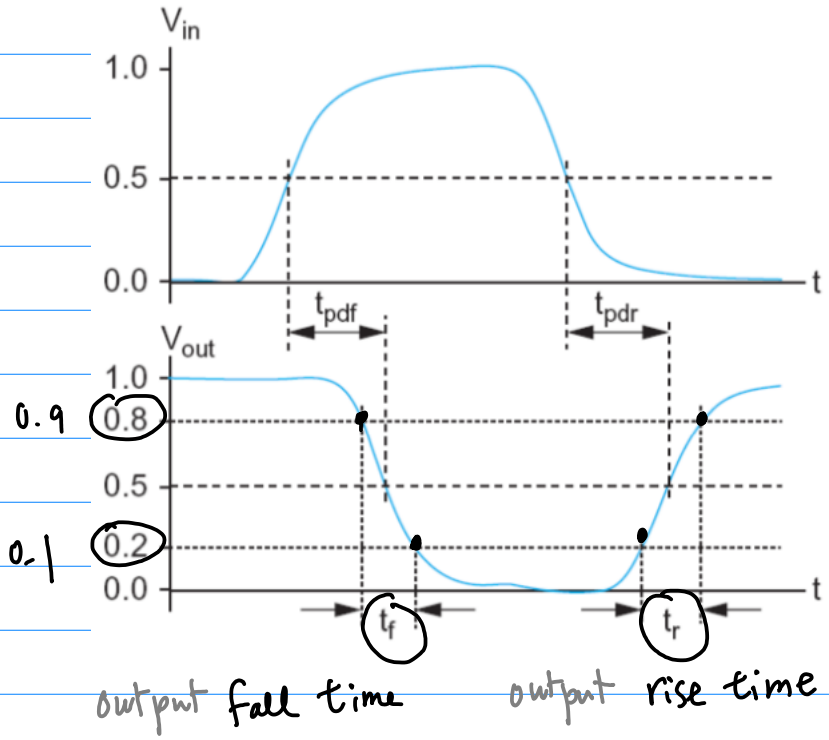


Fan out = 4

# Fan-in

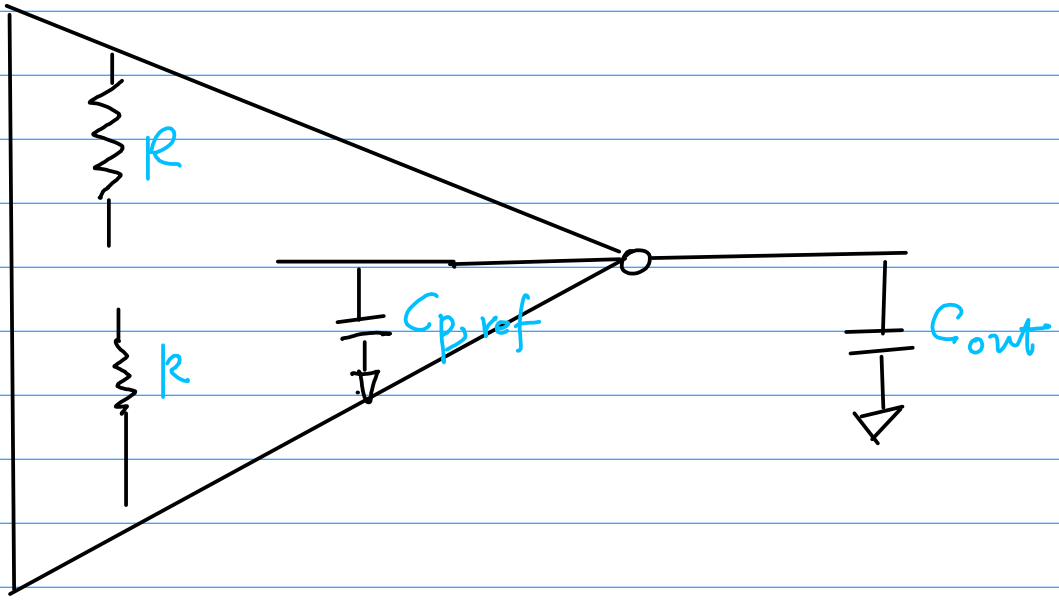


# Fall Delay & Rise Delay




$$t_f = 2.2\,\tau_n$$

$$t_r = 2.2\,\tau_p$$




$$\text{delay} = k \cdot R \cdot C$$

# Transistor Sizing

determination of the appropriate $(\frac{W}{L})$'s for transistors for performance or other design goals

**Transistor sizing algorithm**

- individually tune the widths of all transistors in a circuit to meet delay requirement
- or make efficient use of layout area → power efficient
  every transistor with different size → difficult to layout
- approximation in standard cells
  → selecting different sized transistors

transistor sizing is used in circuits
that inherently requires long wires.

Varying the sizes of transistors at strategic points
→ improve delay

full custom layout : arbitrary transistor sizing

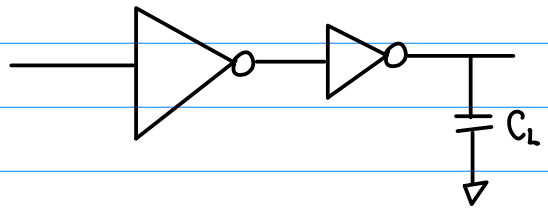
Standard cell : limited transistor sizing
several versions of differently-sized transistors

driving large load

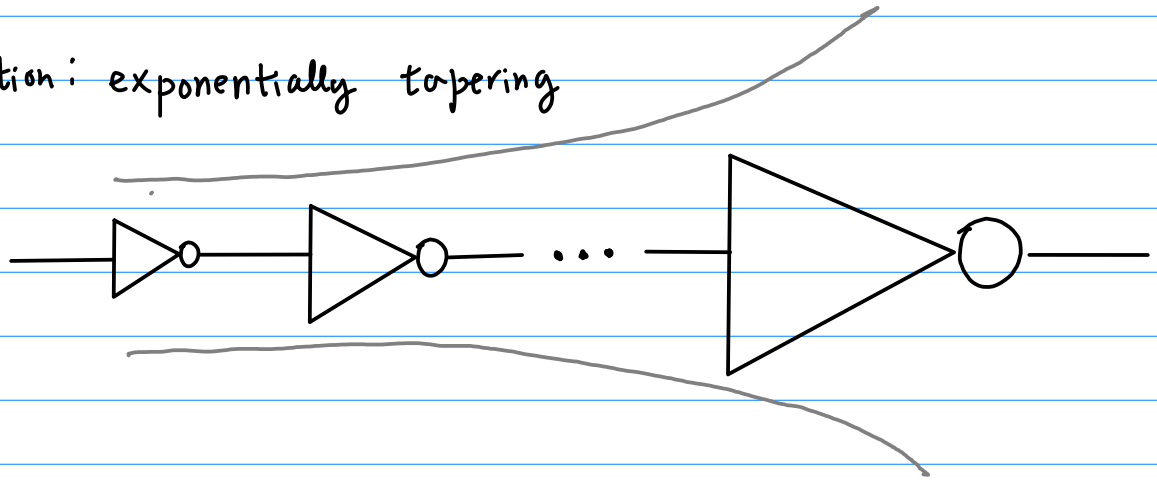
- off chip load
- long signal wire
- clock, reset wire (large fan out)

large fan out → large capacitance

to increase current by large transistor
also increase the gate capacitance
— problem back one level of logic




Solution: exponentially tapering



① use a minimum sized device throughout

② then optimize paths
from a critical path timing analysis