DRAM (H.1)

20151217

Static RAM (SRAM)

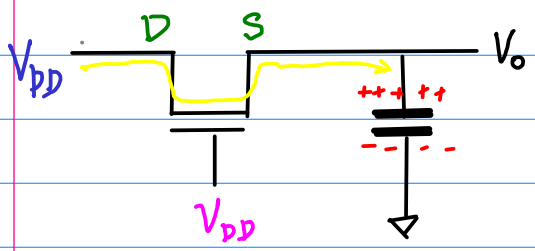
* Data stored as long as power is on
* Large area (6 transistors / cell)
* Fast access time
* Differential

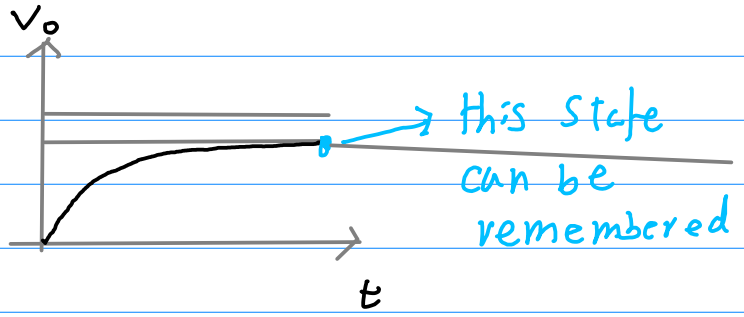
Dynamic RAM (DRAM)

* Periodic refresh necessary
* Small area (1~3 transistors / cell)
* Slow access time
* Single ended

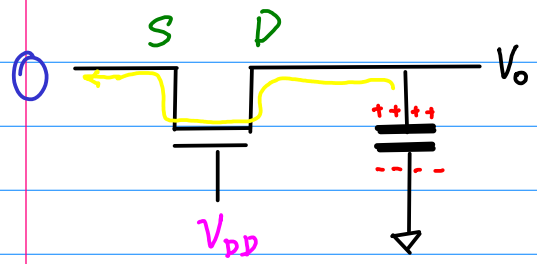
Pass Transistor

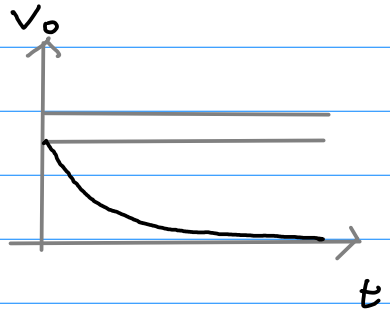
Charge

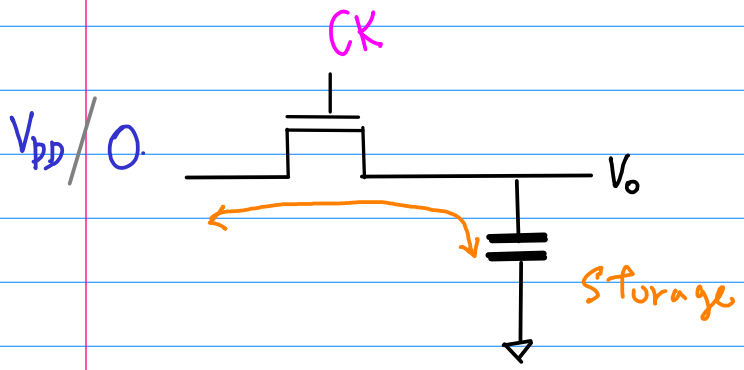




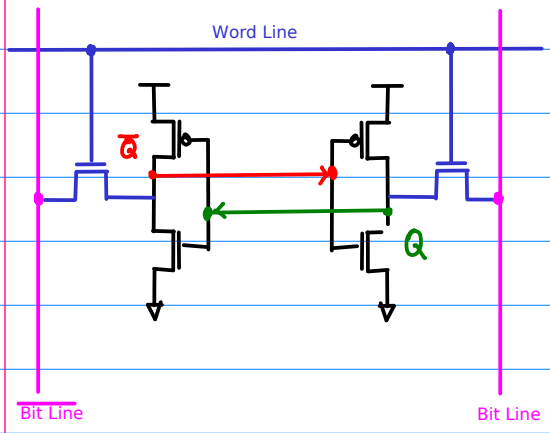
Discharge



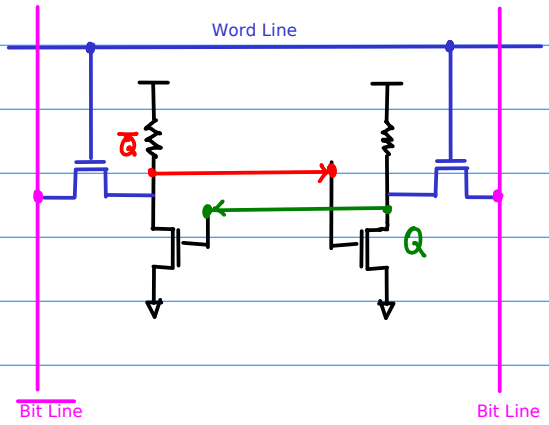




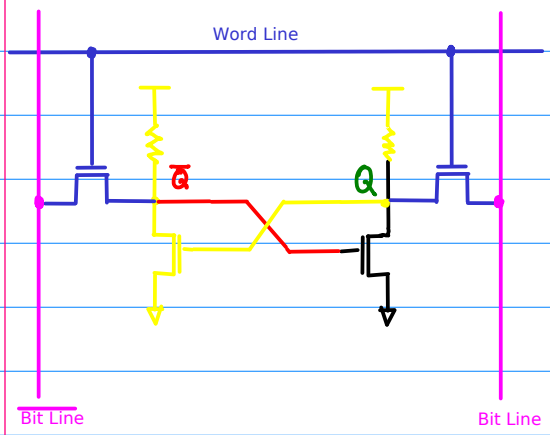
6TR SRAM

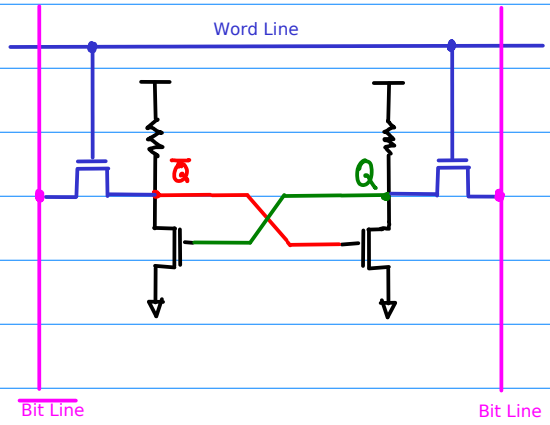


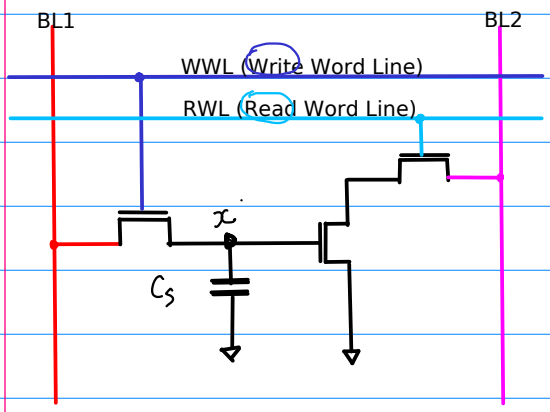
Resistive-load SRAM cell



resistor & redundant tr removed





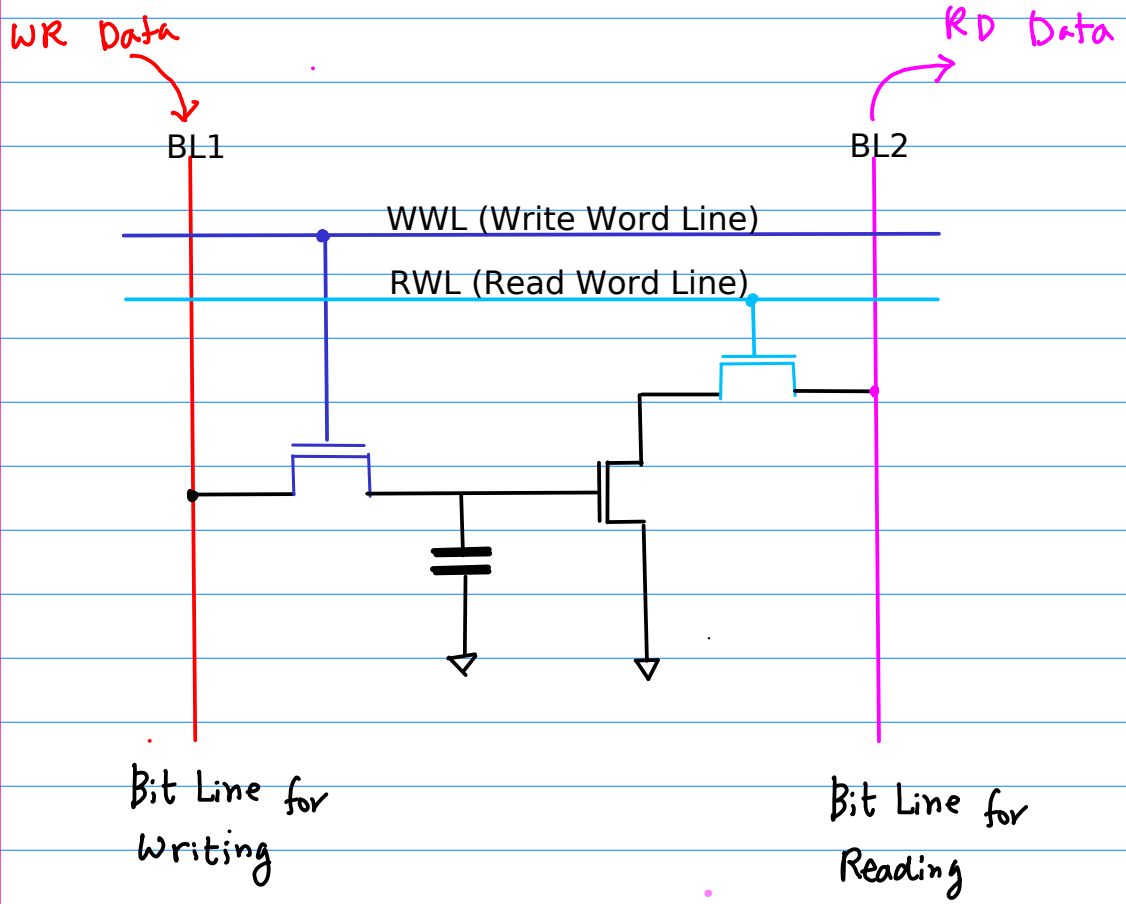


Cs: Storage Capacitance

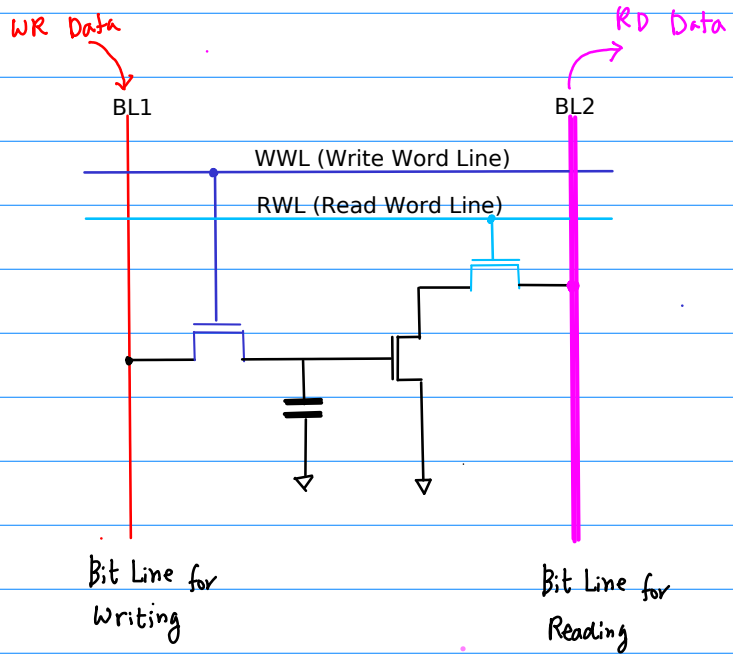
Cs :

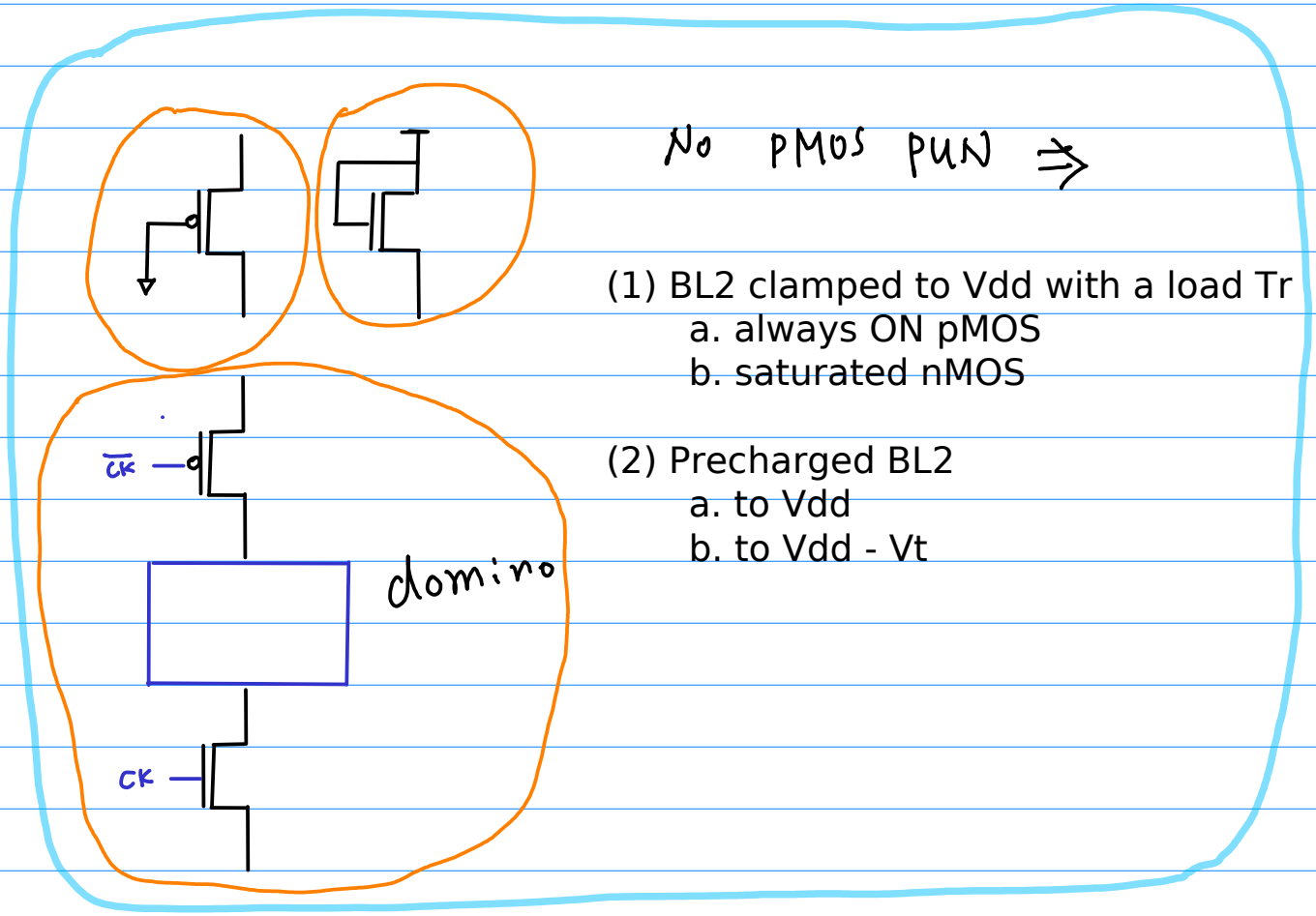
no explicit capacitor
just a gate capacitance

3 Tr DRAM Cell

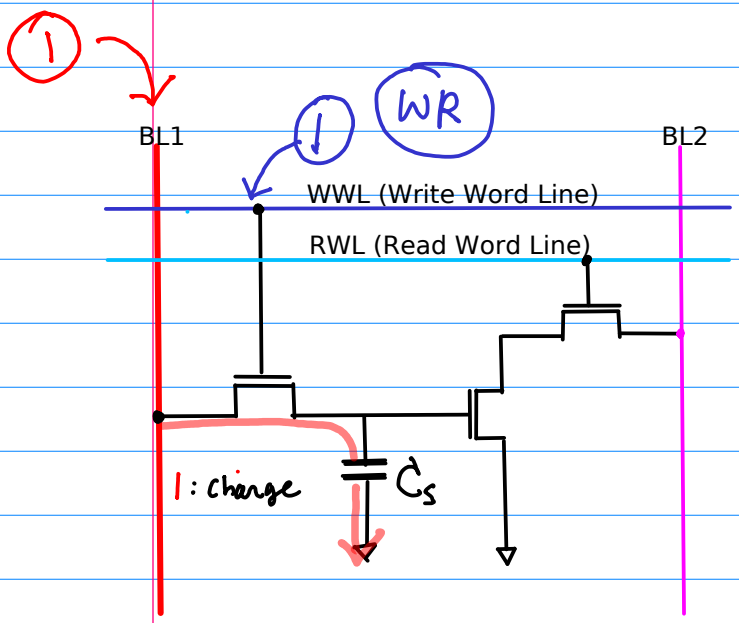


Conditionally Discharged Output

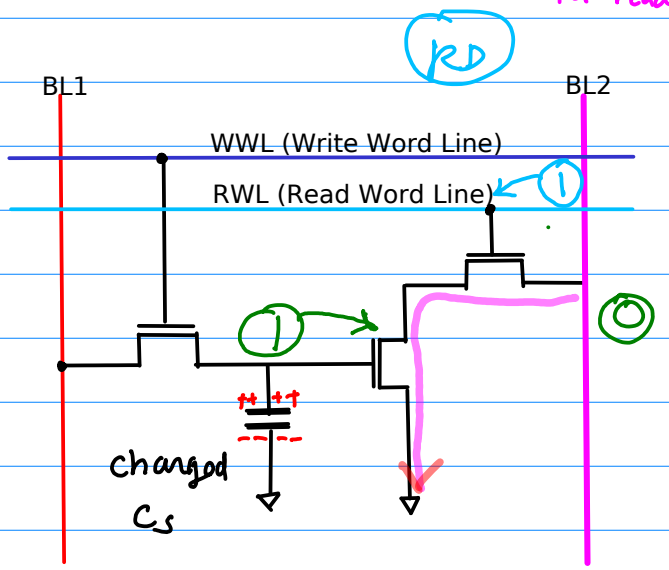




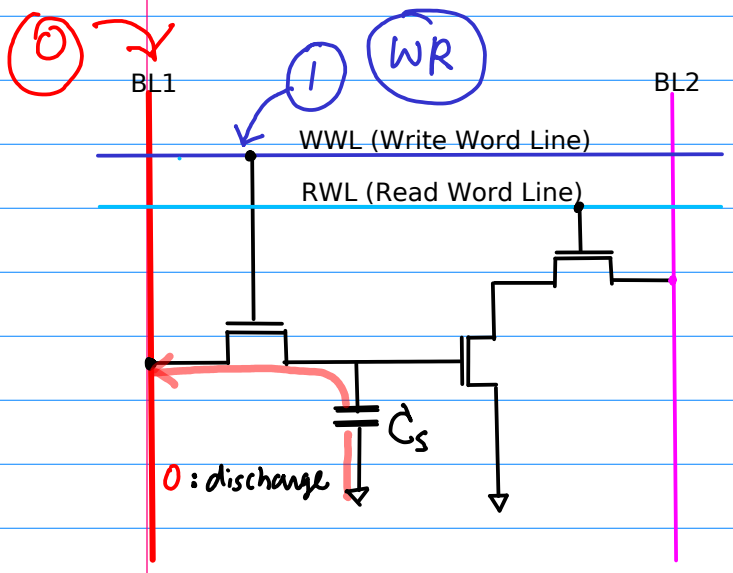
Read / Write Overview



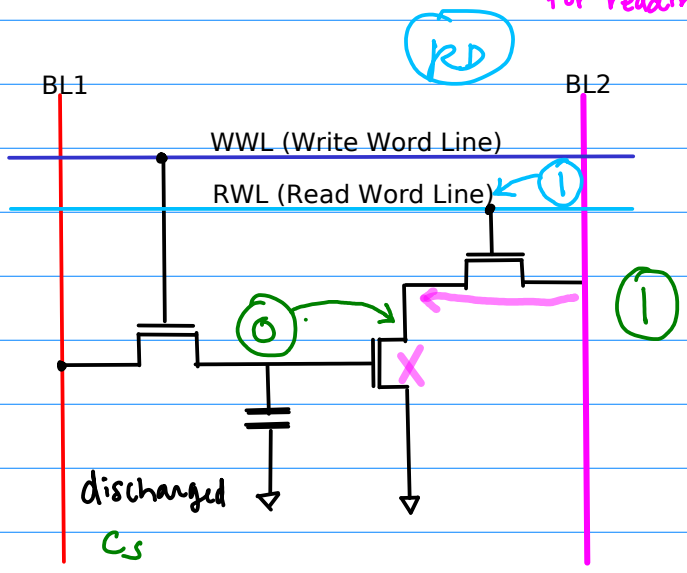
precharged for reading



1 → 0 inverted output



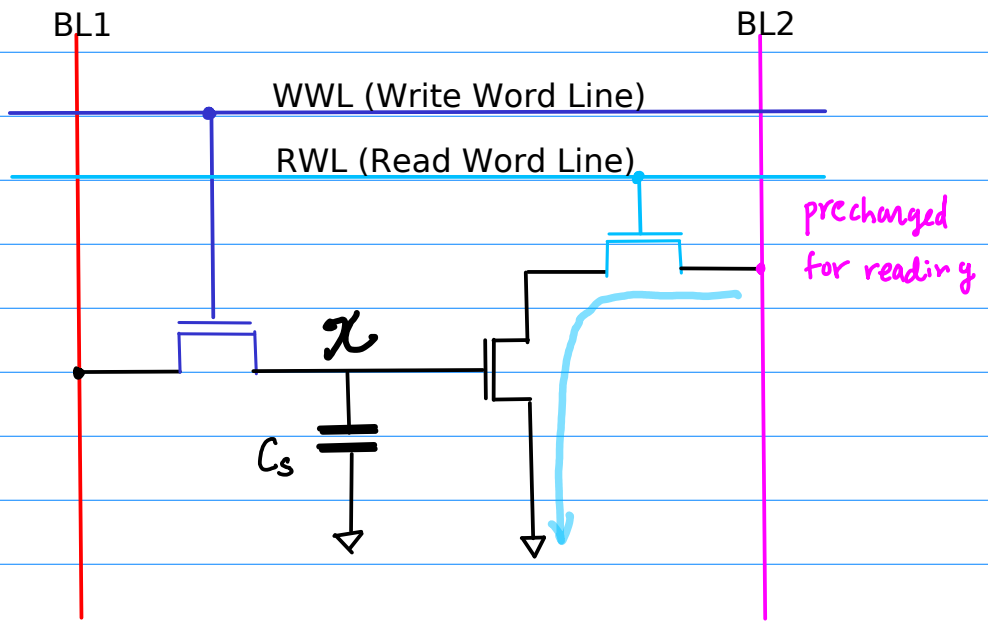
precharged for reading

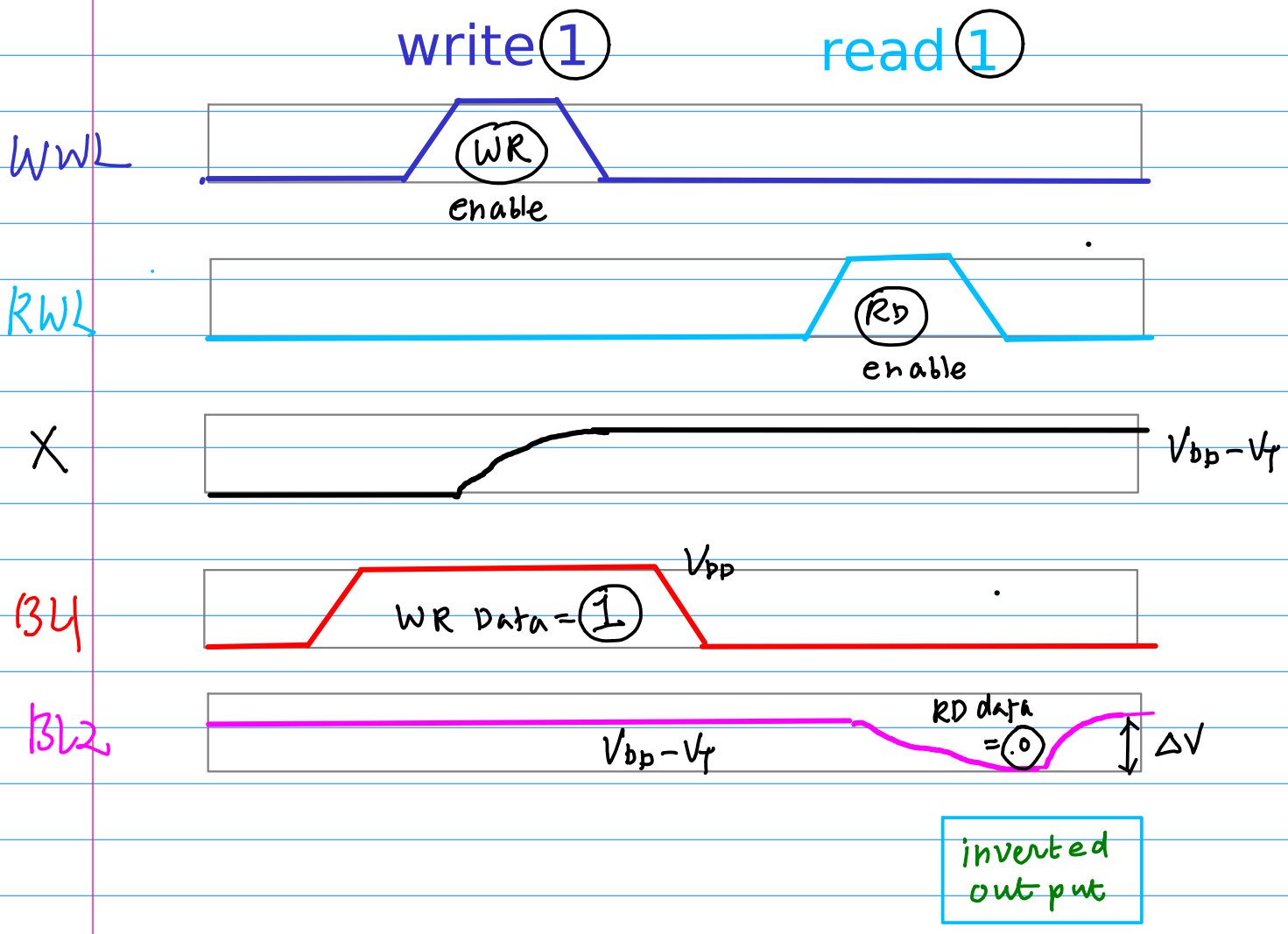


0 → 1 inverted output

non-destructive read

Access Timing Overview



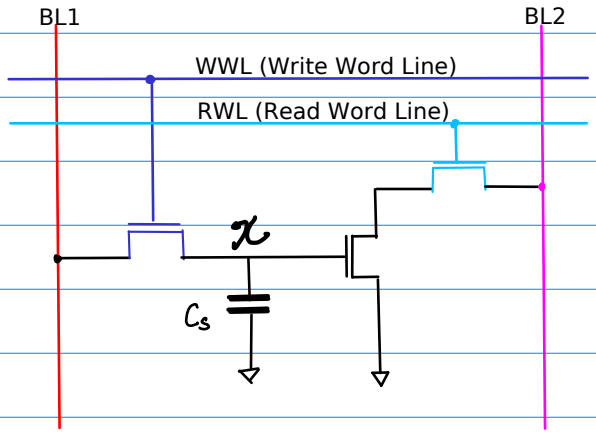


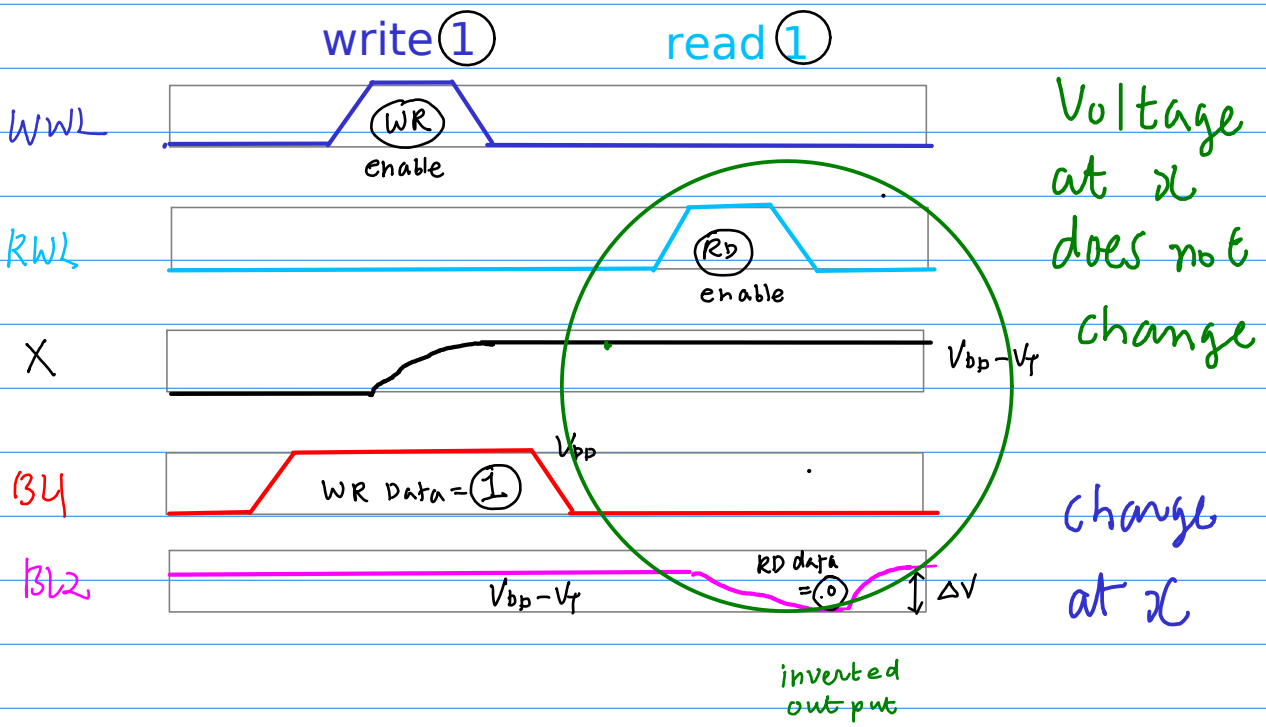
Chracteristics of 3 Tr DRAM Cell

√ No constraints exist on the device ratios

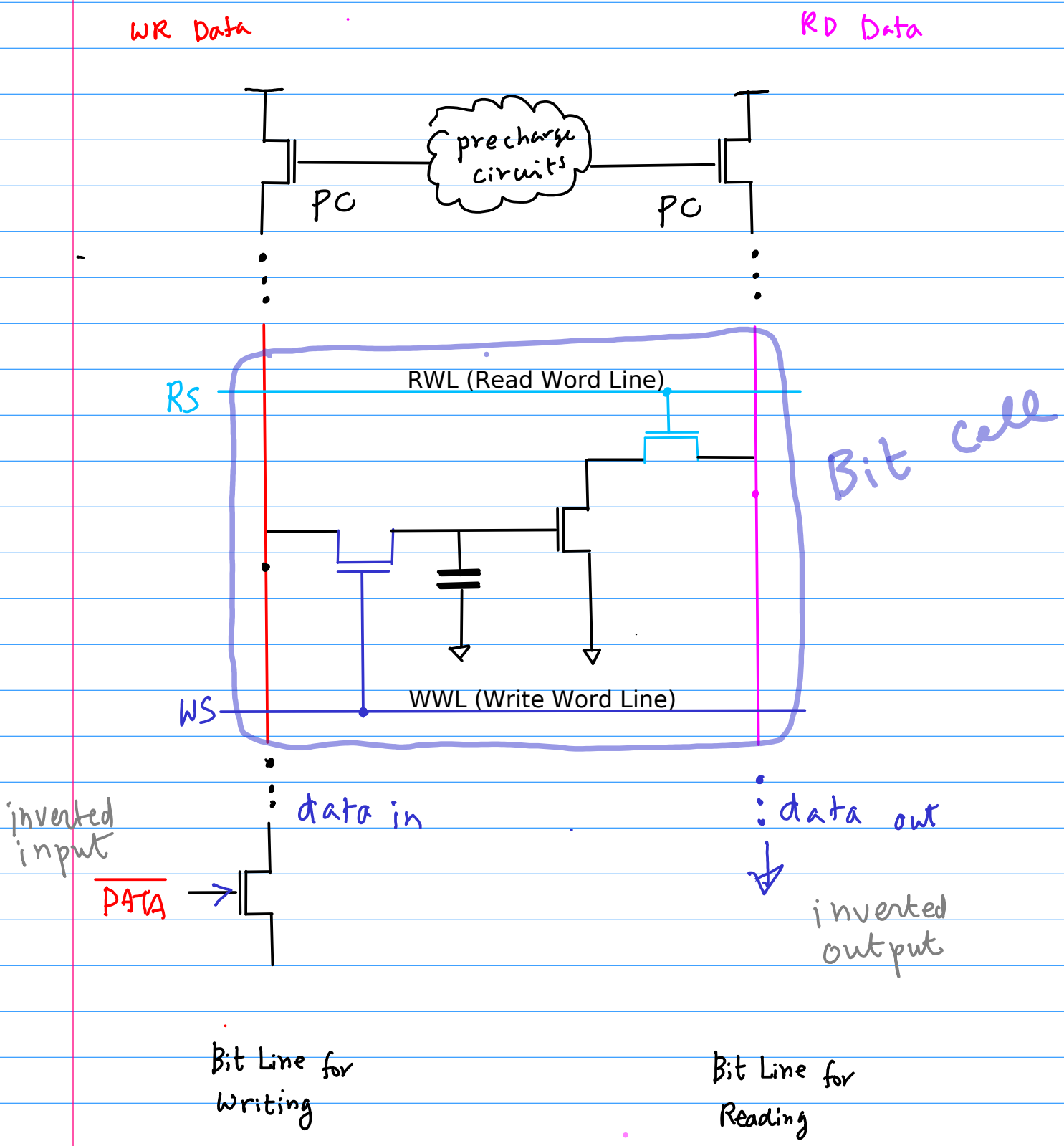
Nondestructive read operation

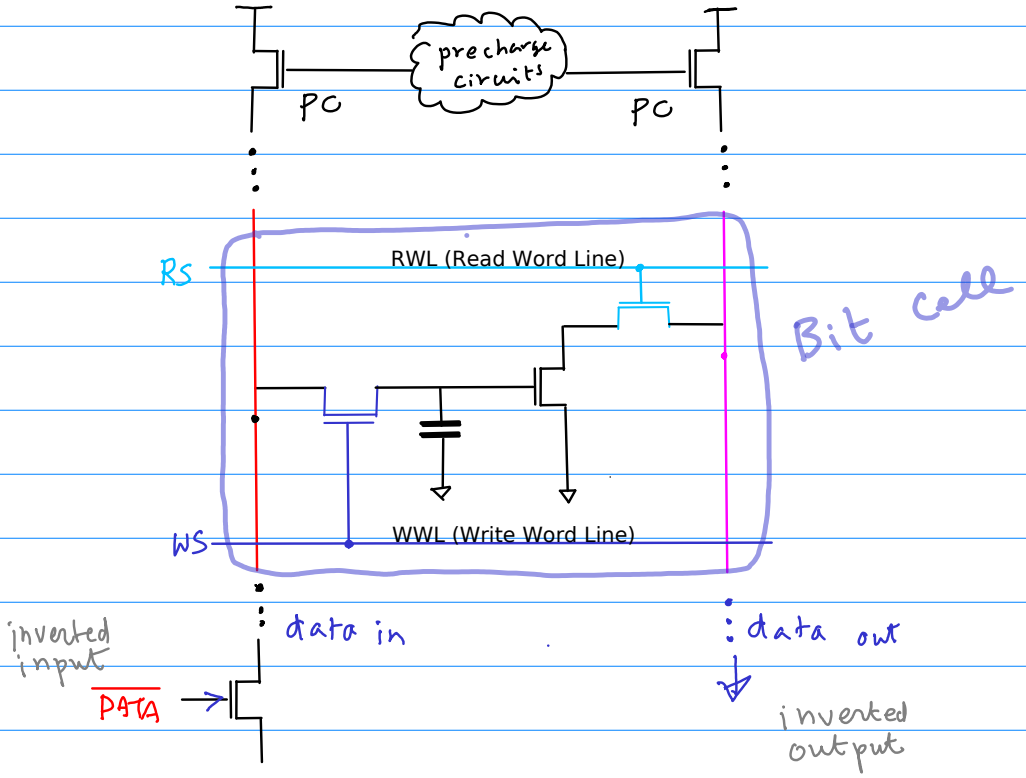
Threshold voltage loss



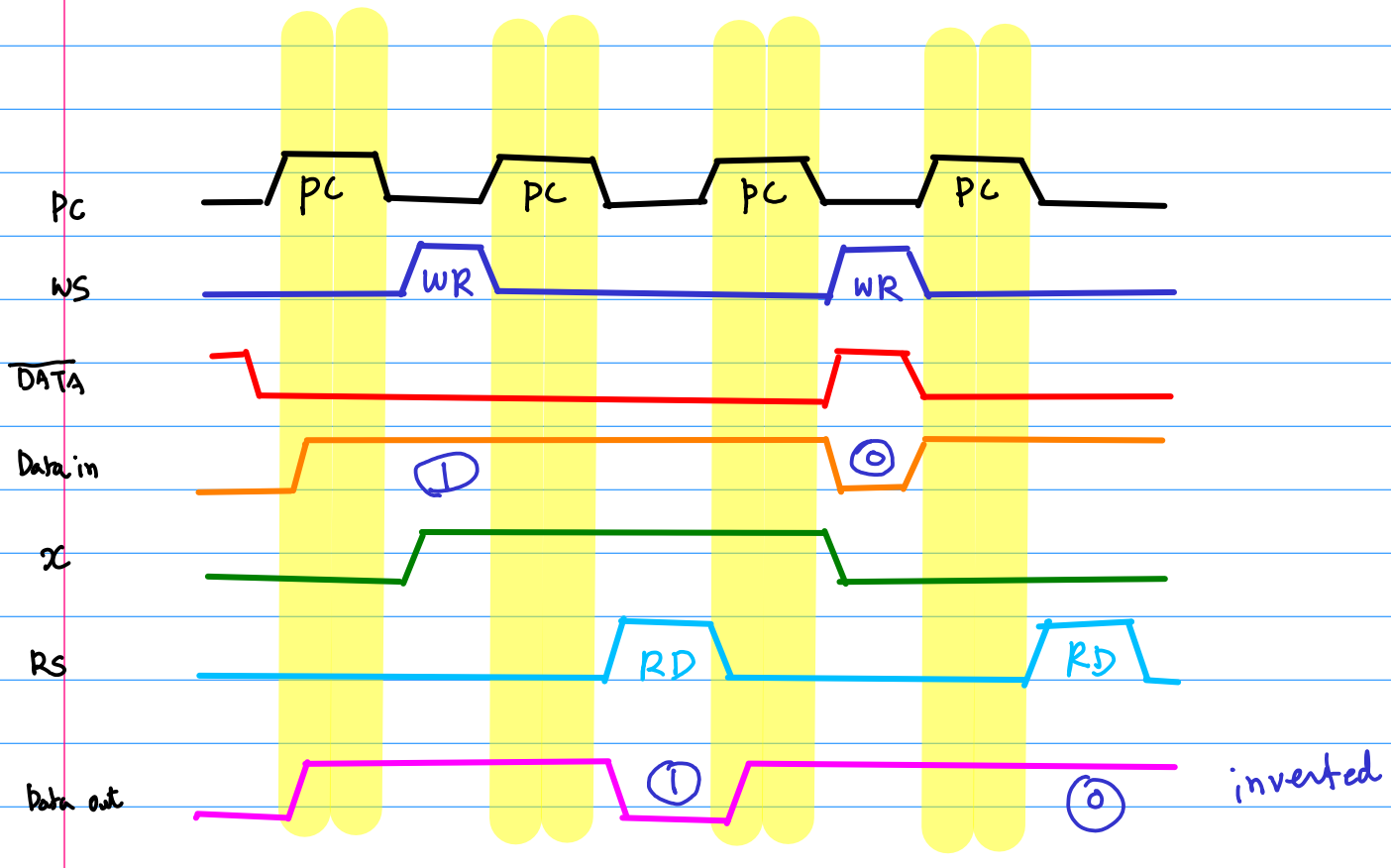


3 Tr DRAM Cell with PU and RW Circuits

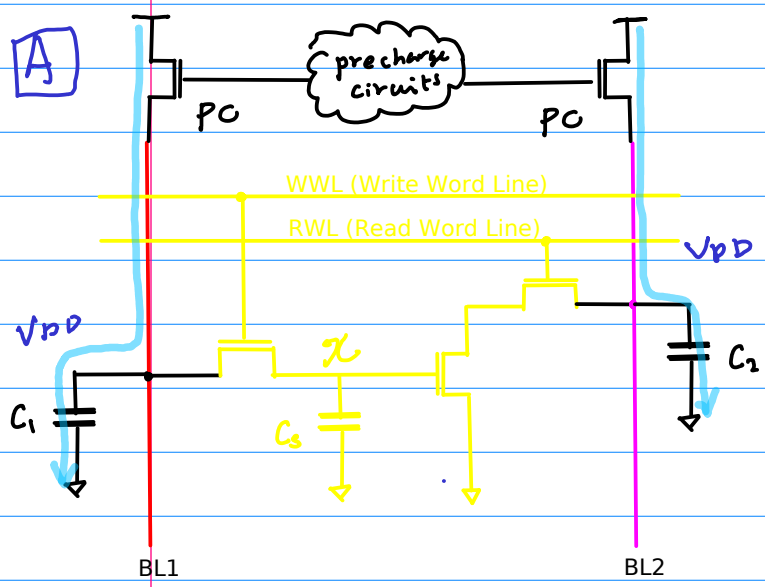


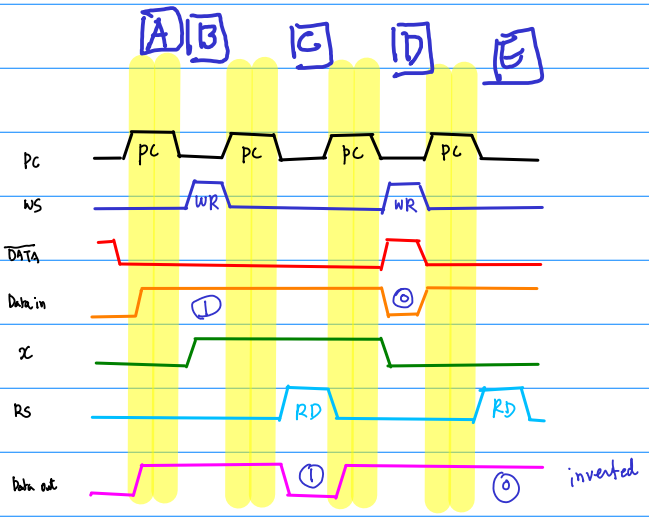


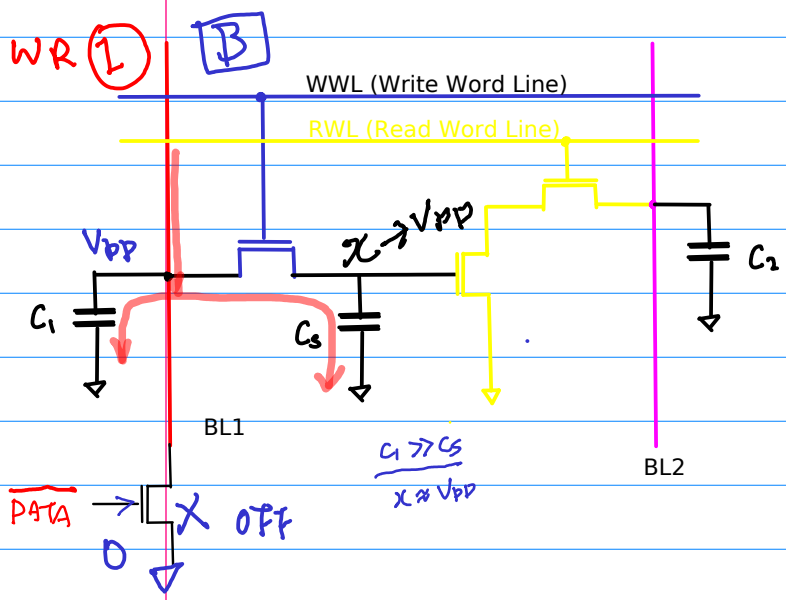
Kang, CMOS Digital Integrated Circuits

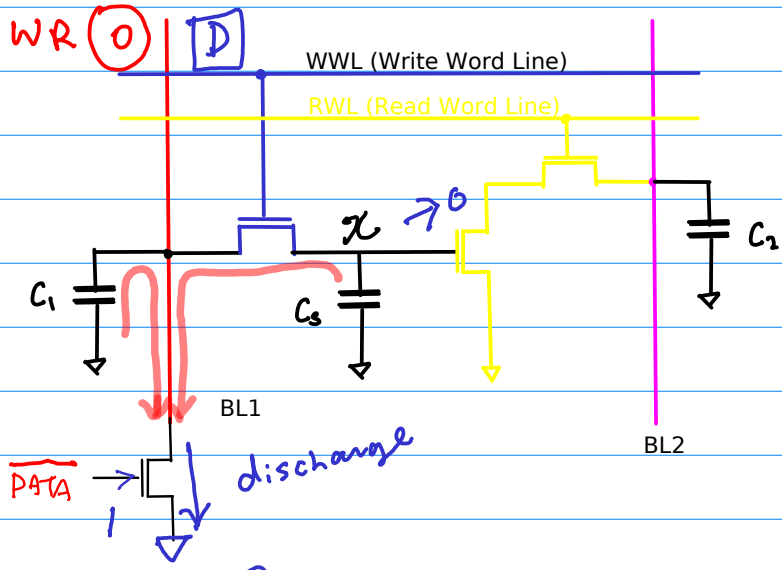


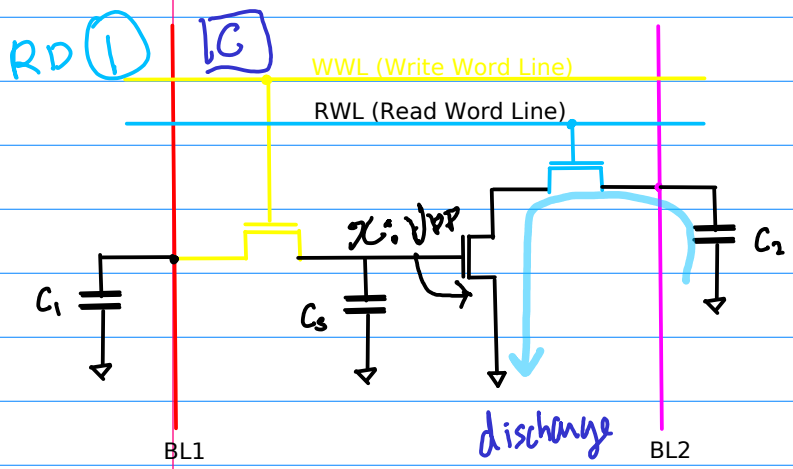
precharge

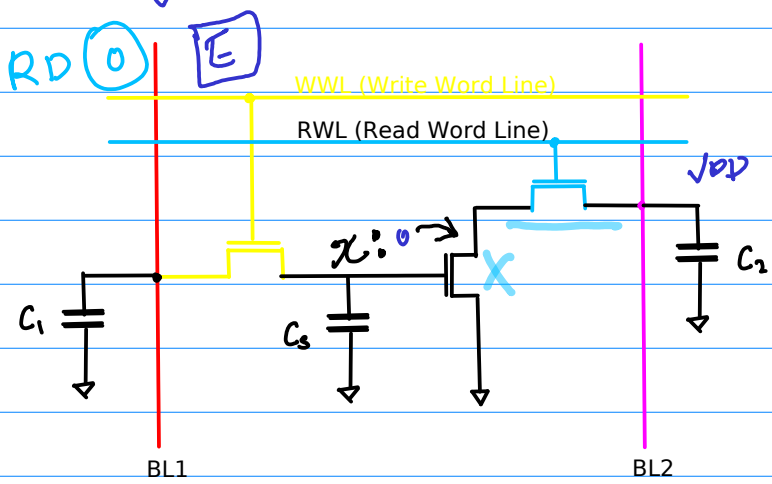

A
precharge circuits
PC
PC
WWL (Write Word Line)
RWL (Read Word Line)
VDD
VDD
C1
Cs
C2
BL1
BL2


A
B
C
D
E
Pc
WS
DATA
Data in
X
RS
Data out
WR
RD
inverted

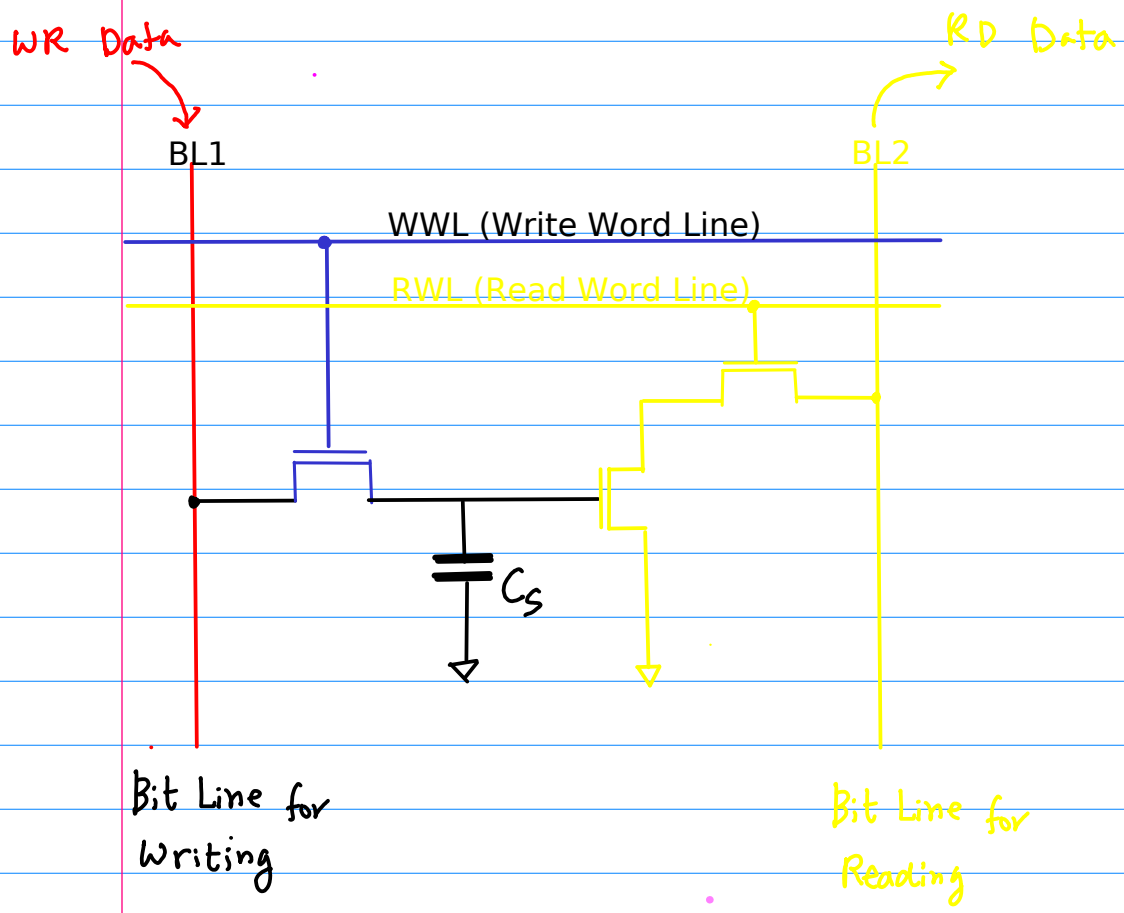

WR 1
B
WWL (Write Word Line)
RWL (Read Word Line)
VDD
X → VDD
C1
Cs
C2
BL1
BL2
C1 >> Cs
X ≈ VDD
DATA
0
X OFF

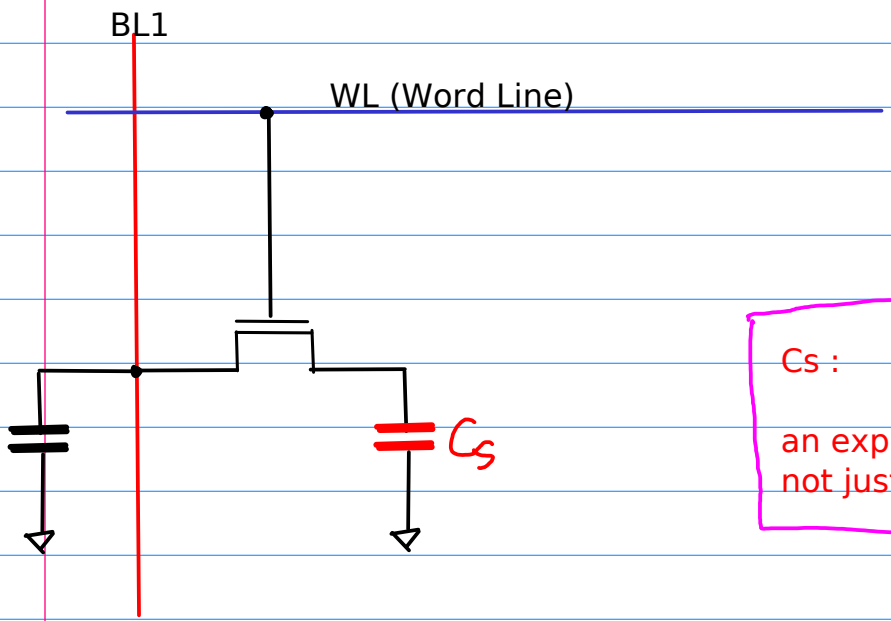

WR 0
D
WWL (Write Word Line)
RWL (Read Word Line)
X → 0
C1
Cs
C2
BL1
BL2
DATA
1
discharge


RD 1
C
WWL (Write Word Line)
RWL (Read Word Line)
X: VDD
C1
Cs
C2
BL1
BL2
discharge


RD 0
E
WWL (Write Word Line)
RWL (Read Word Line)
VDD
X: 0
X
C1
Cs
C2
BL1
BL2

1 Tr DRAM Cell

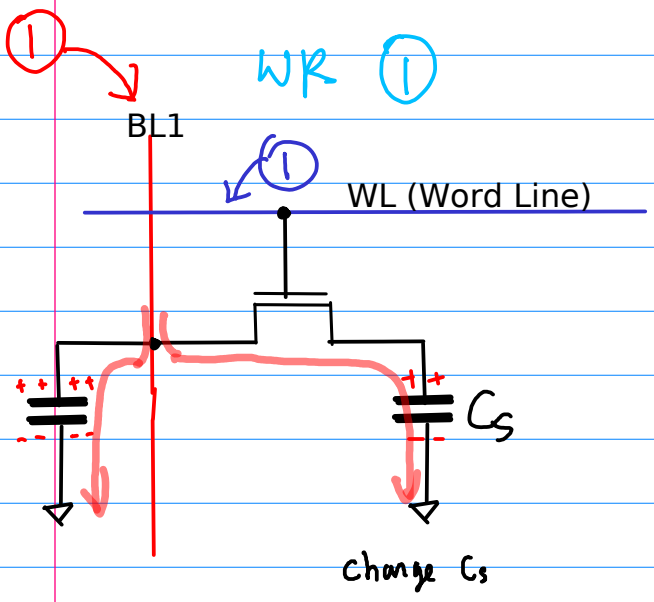


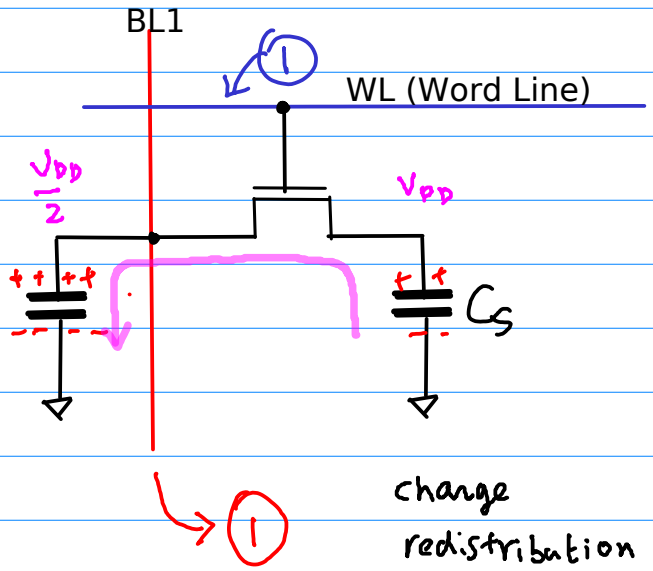


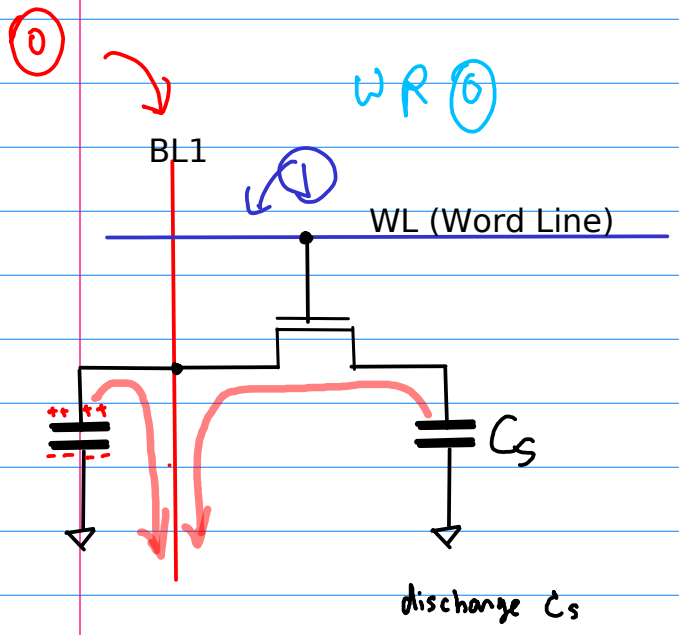
Cs :

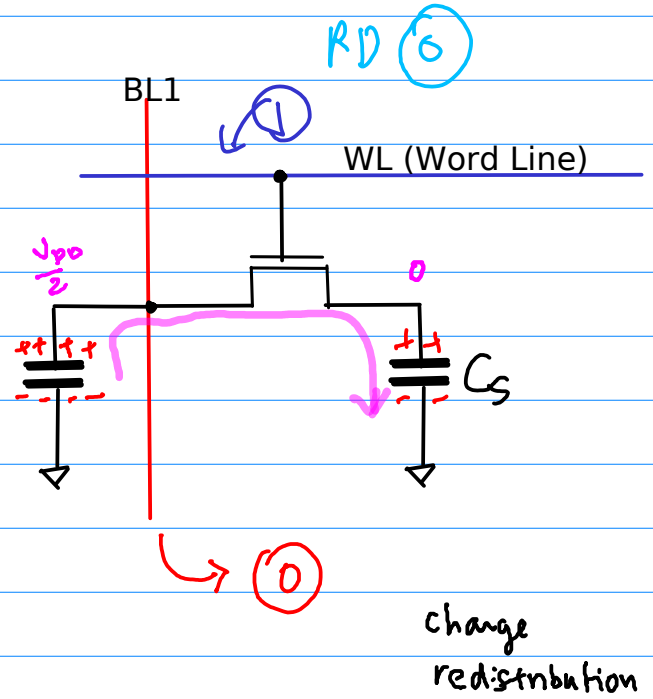
an explicit capacitor
not just a gate capacitance

precharge Bit Line before RD operation $\frac{V_{DD}}{2}$

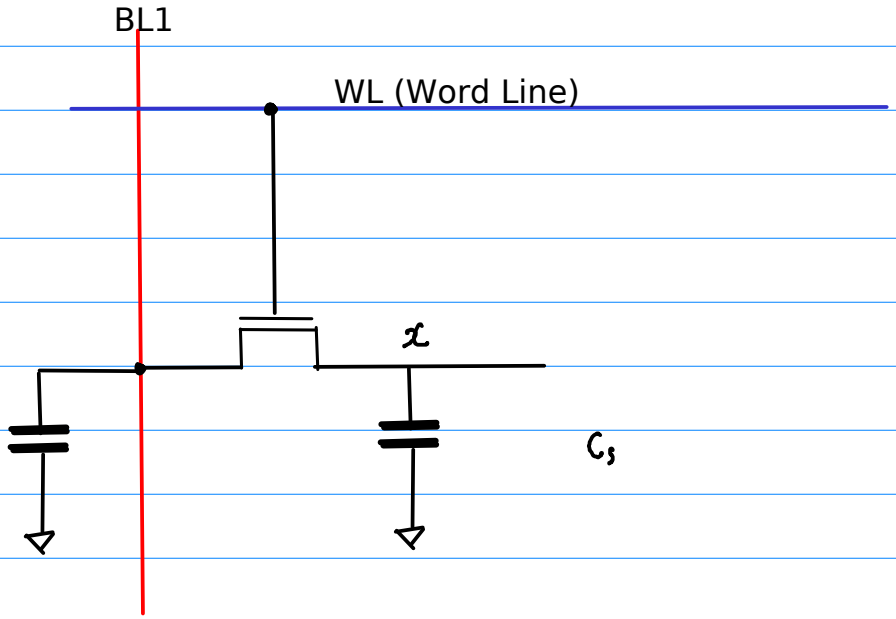


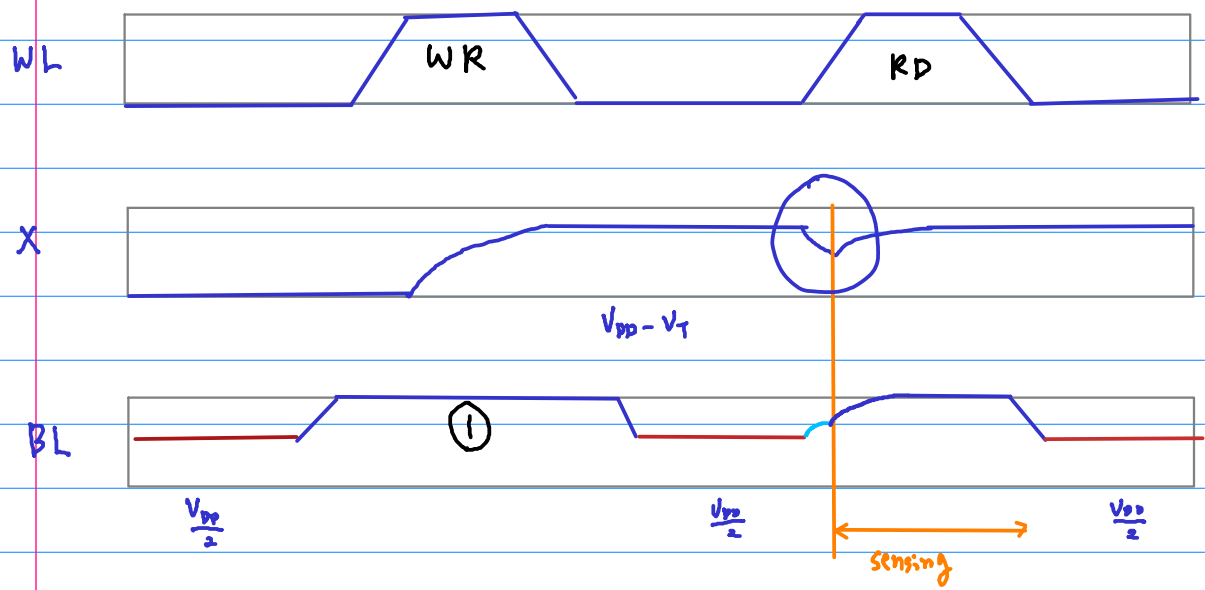






✡ Change Redistribution ⇒ Destructive Reading





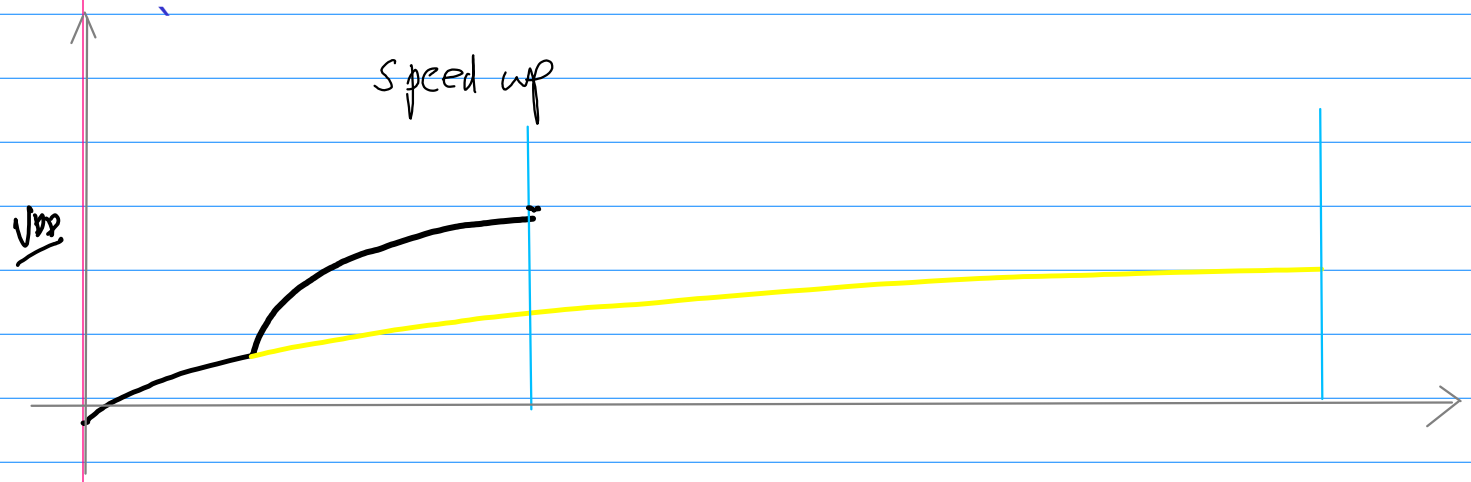
charge redistribution

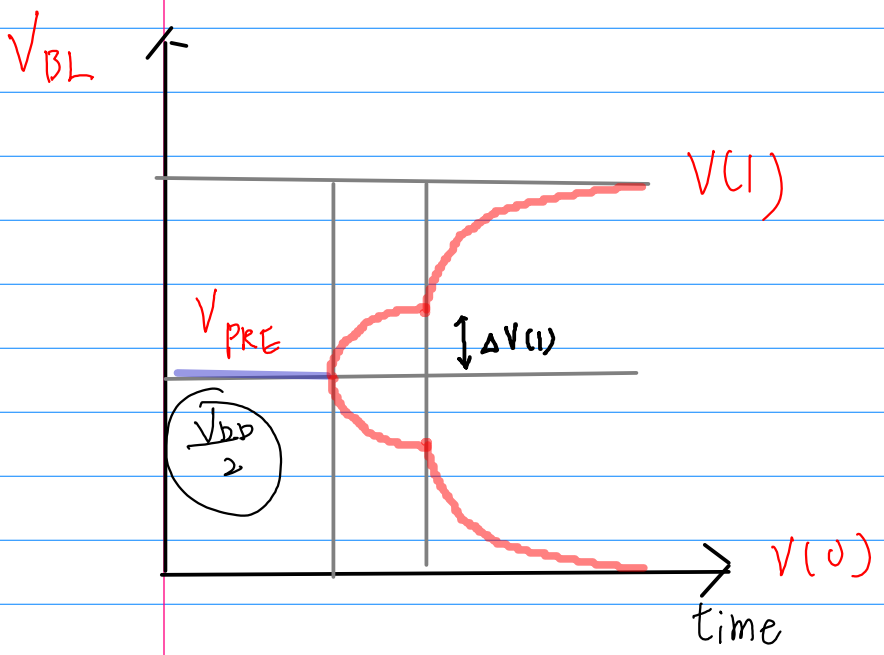
⇒ destructive

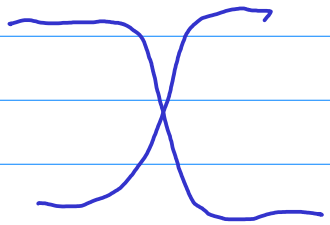
1T DRAM needs a sense amplifier
: the charge redistribution based read operation

A sense amplifier to speed up the read operation
not for functionality considerations

all read operation rely on current sinking





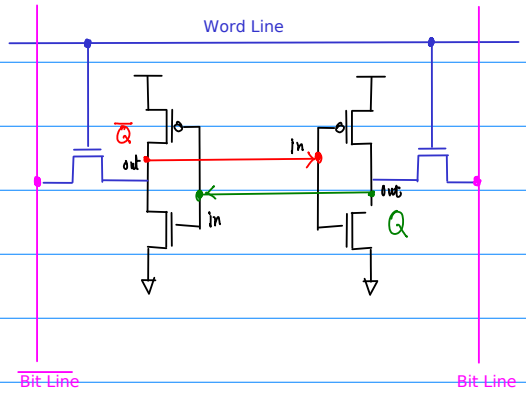


Single-end : DRAM

No complimentary data required

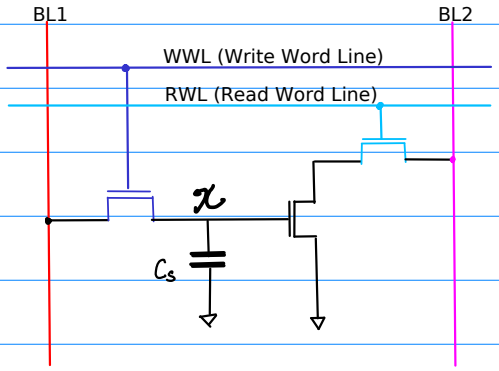
X (Q, $\bar{Q}$)

6-Tr CMOS SRAM Bit Cell



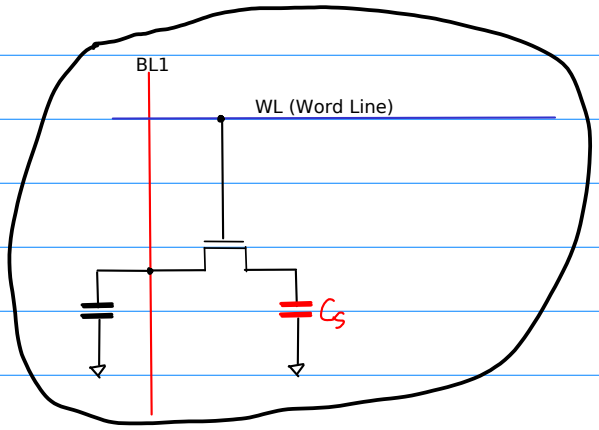
complementary

3-Tr CMOS DRAM Bit Cell



for WR

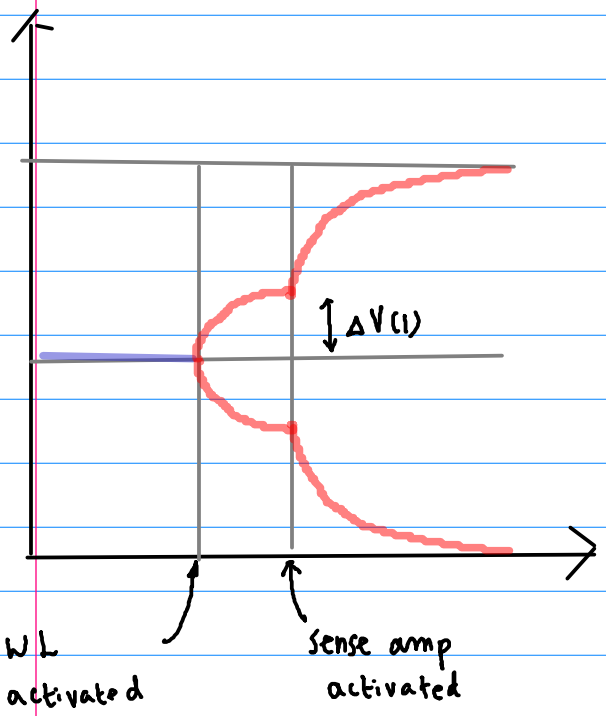
for RD



complicated
sense amp

simple
sense amp

charge sharing / redistribution



$$\Delta V = V_{BL} - V_{PRE}$$
$$= (V_{BIT} - V_{PRE}) \frac{C_S}{C_S + C_{BL}}$$

V_{BL} = the Bit Line potential after charge redistribution

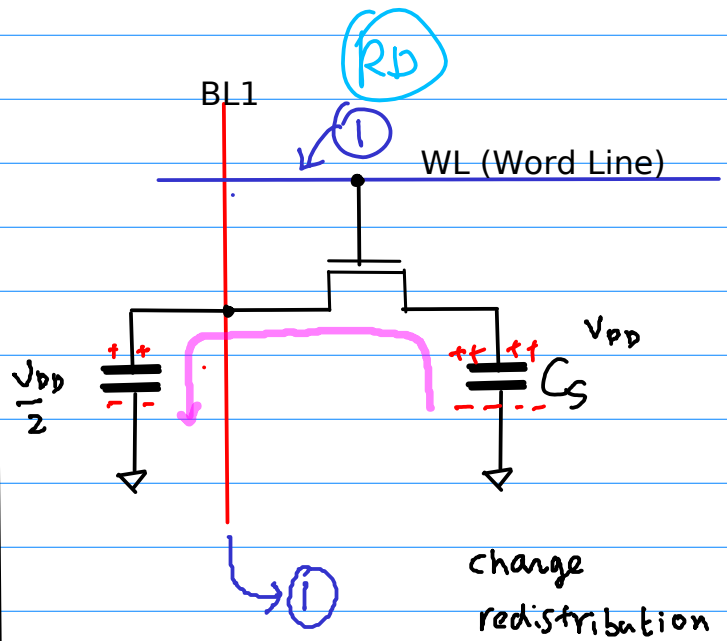
V_{BIT} = the initial potential of C_S

$C_S \ll C_{BL}$

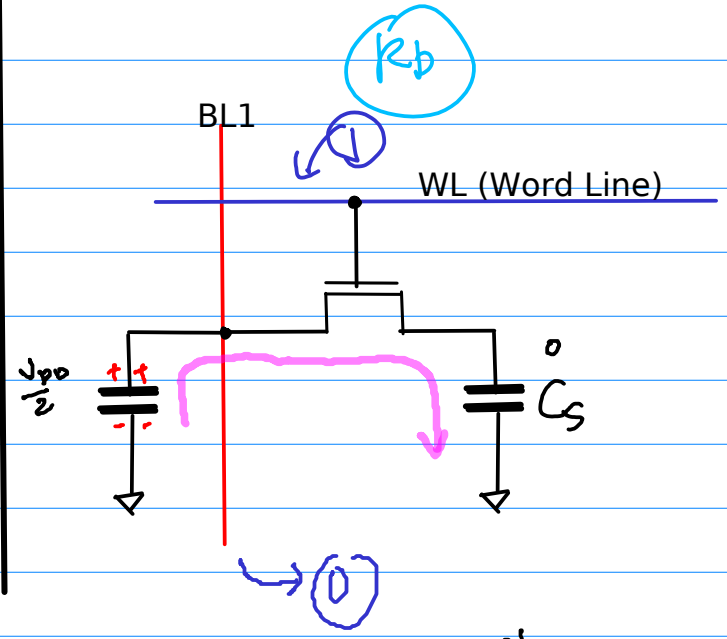
$\frac{C_S}{C_S + C_{BL}} \approx 1 \sim 10\%$

charge transfer ratio

precharge Bit Line before RD operation

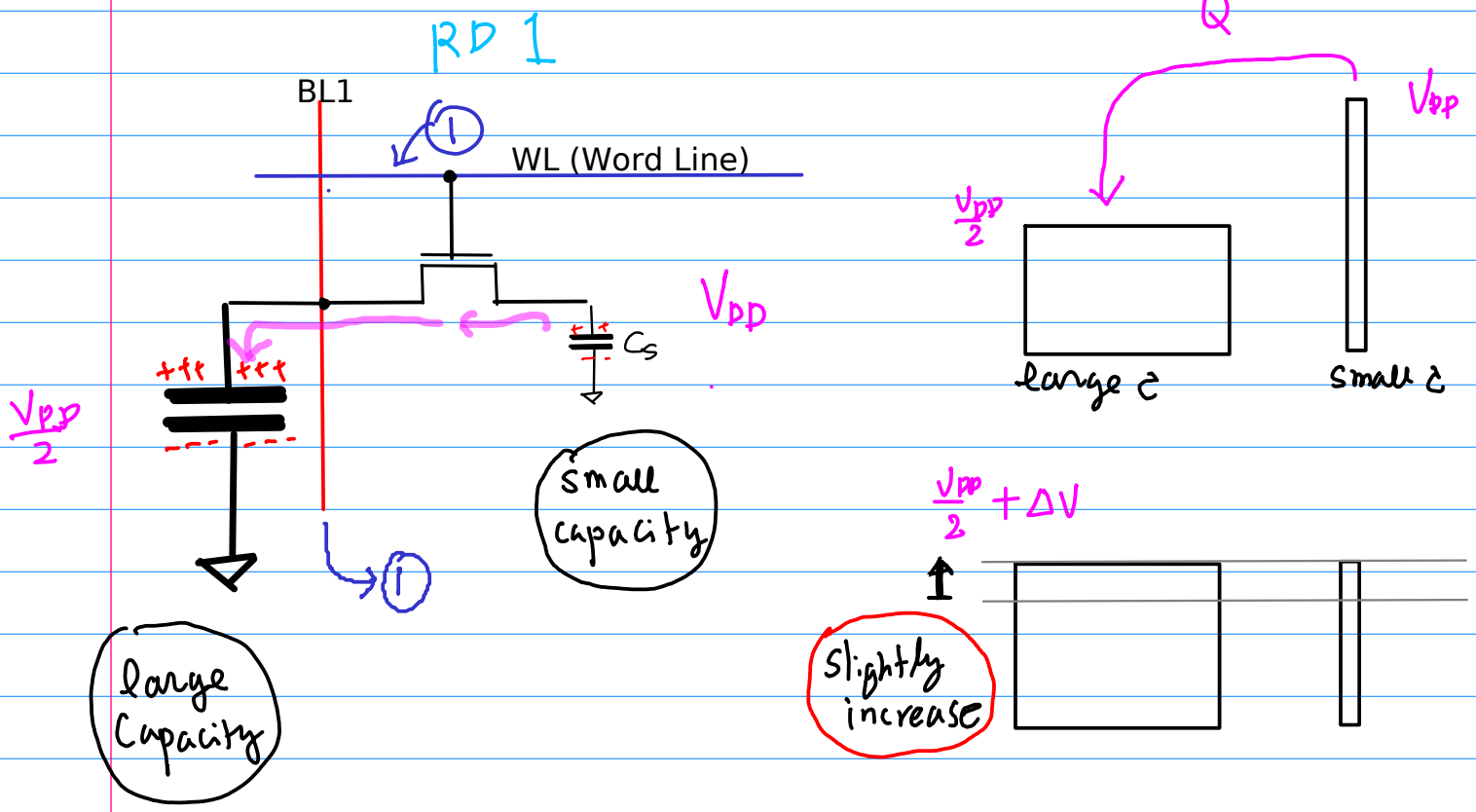


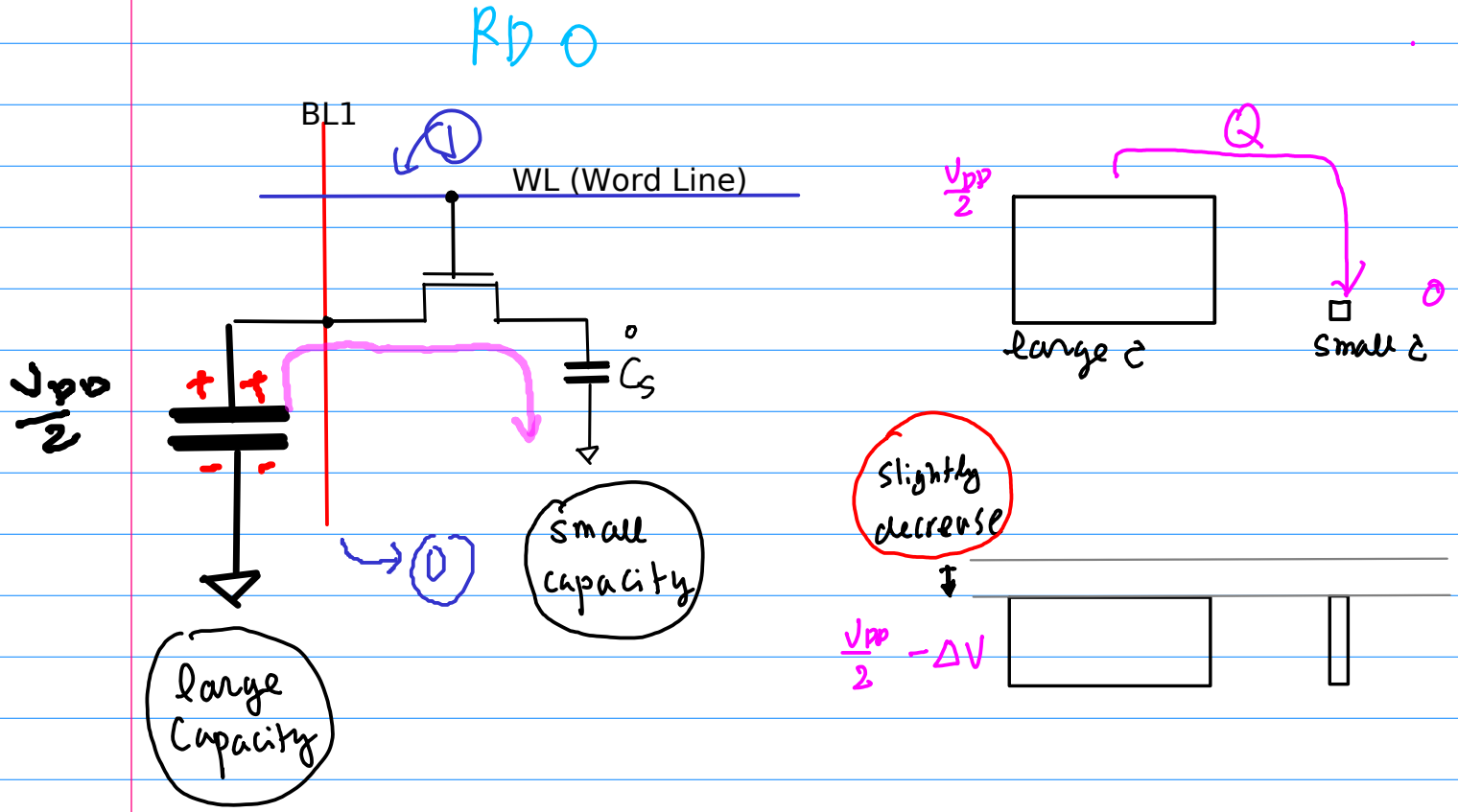
charge redistribution



charge redistribution

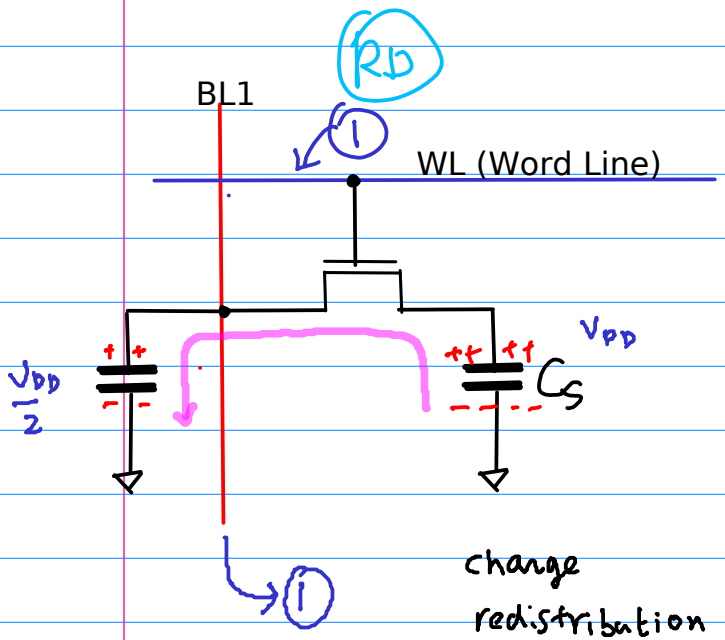
Charge Movement

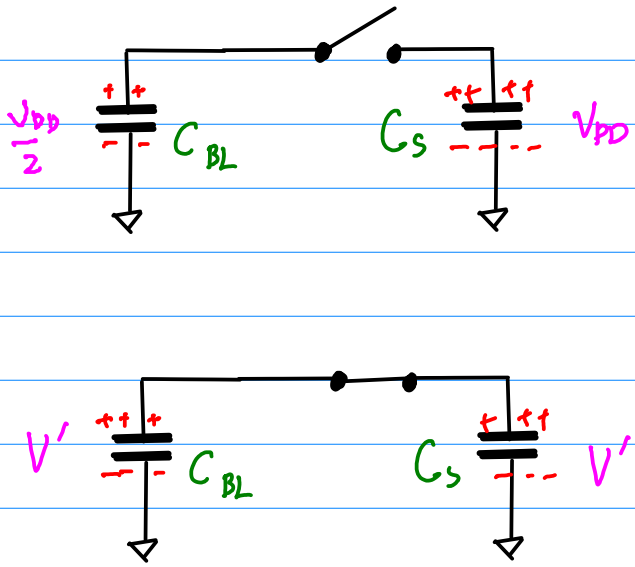




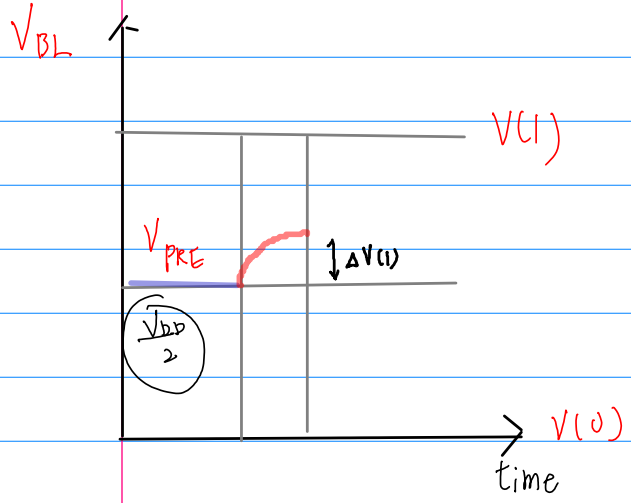
charge sharing / redistribution

precharge Bit Line
before RD operation





$$\frac{V_{DD}}{2} \cdot C_{BL} + V_{DD} C_S = (C_{BL} + C_S) V'$$



$$\frac{V_{DD}}{C_{BL} + C_S} \left(\frac{C_{BL}}{2} + C_S \right) = V'$$

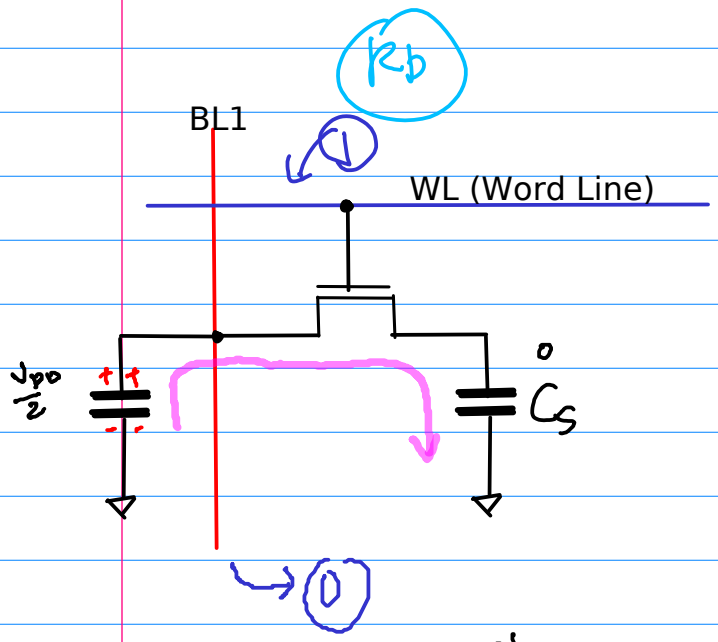
$$\frac{V_{DD}}{2} \frac{C_{BL} + 2C_S}{C_{BL} + C_S} = V'$$

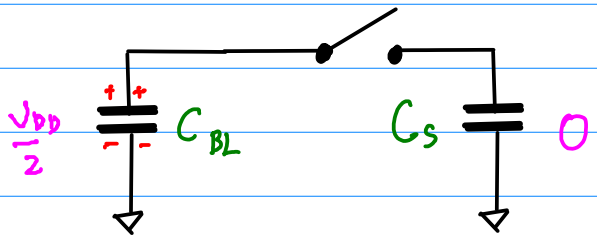
$$\frac{V_{DD}}{2} \left(\frac{C_{BL} + 2C_S}{C_{BL} + C_S} - 1 \right) = V' - \frac{V_{DD}}{2}$$

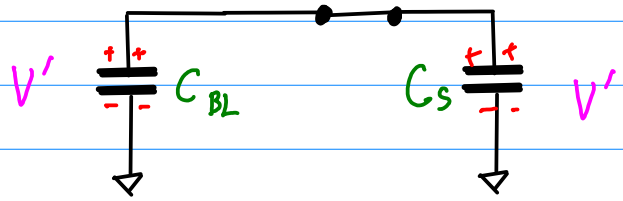
$$+ \frac{V_{DD}}{2} \left(\frac{C_S}{C_{BL} + C_S} \right) = \Delta V$$

charge sharing / redistribution

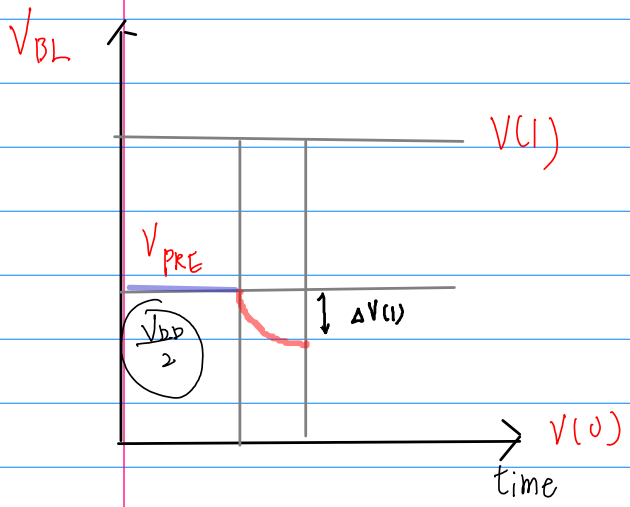
precharge Bit Line
before RD operation







charge
redistribution



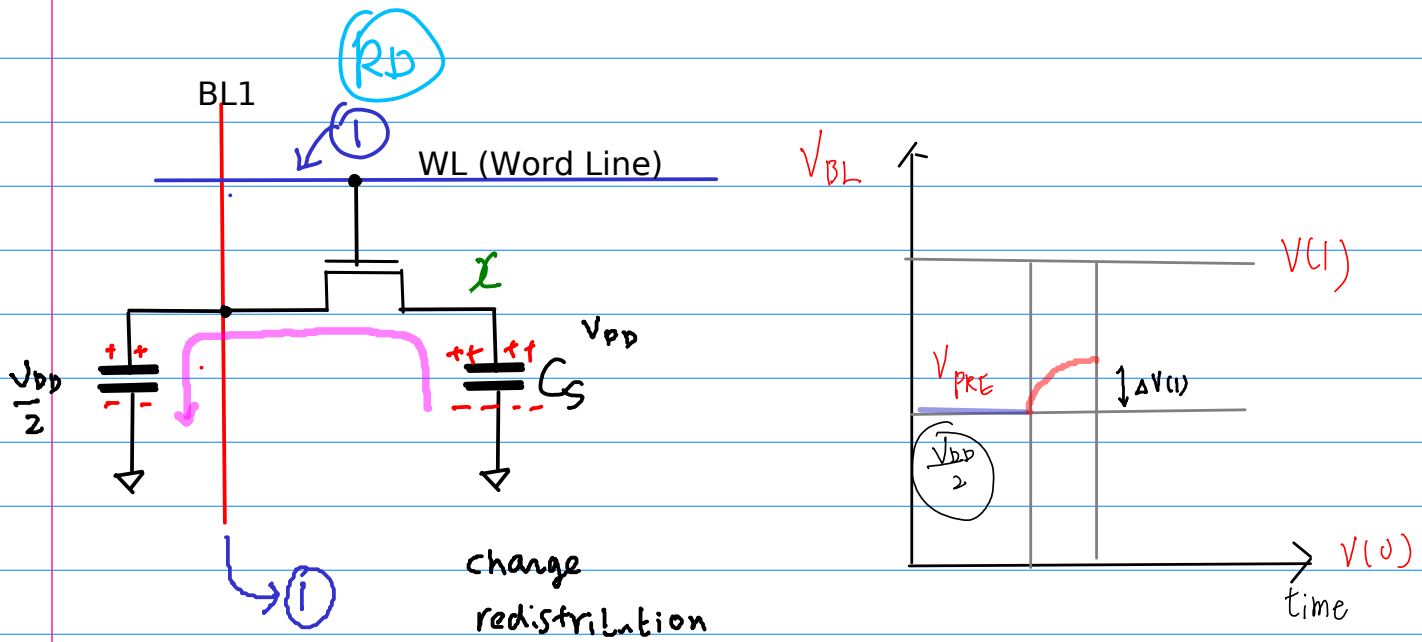
$$\frac{V_{DD}}{2} \cdot C_{BL} + 0\, C_S = (C_{BL} + C_S)\, V'$$

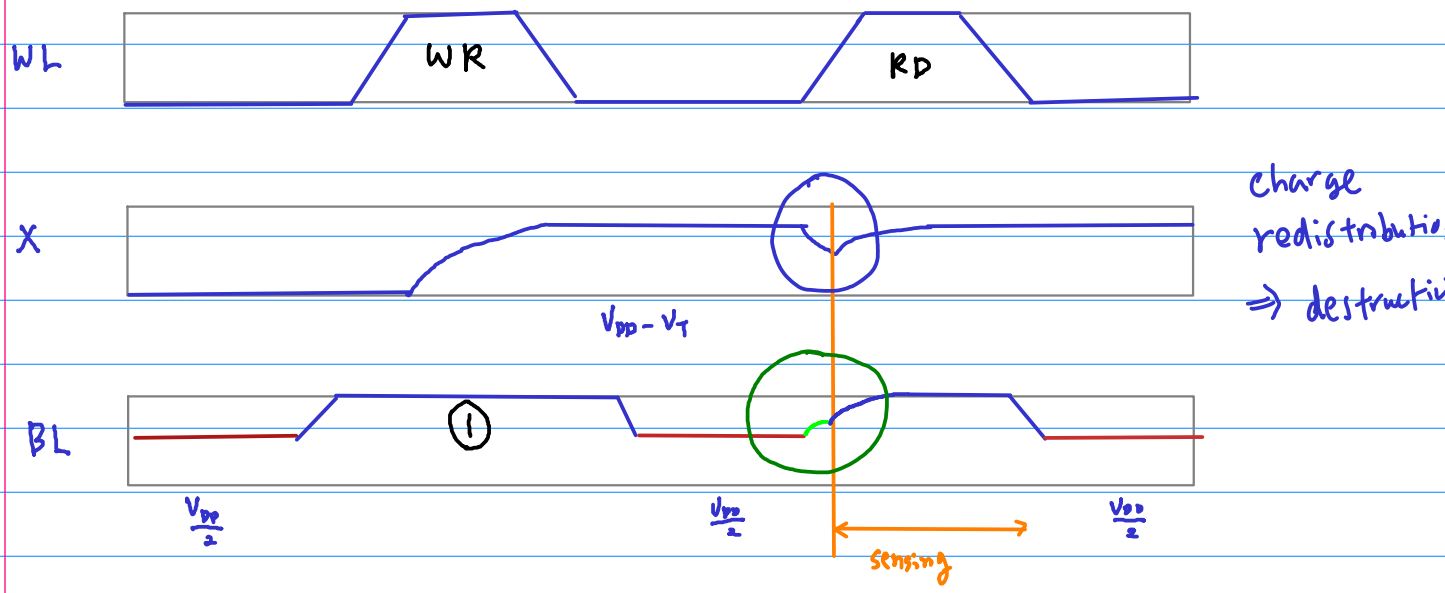
$$\frac{V_{DD}}{C_{BL} + C_S}\left(\frac{C_{BL}}{2}\right) = V'$$

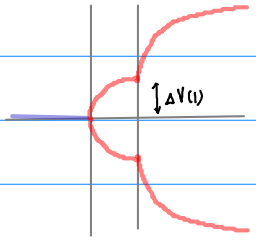
$$\frac{V_{DD}}{2}\,\frac{C_{BL}}{C_{BL} + C_S} = V'$$

$$\frac{V_{DD}}{2}\left(\frac{C_{BL}}{C_{BL} + C_S} - 1\right) = V' - \frac{V_{DD}}{2}$$

$$-\frac{V_{DD}}{2}\left(\frac{C_S}{C_{BL} + C_S}\right) = \Delta V$$


RD
BL1
1
WL (Word Line)
X
V_{DD}
$\frac{V_{DD}}{2}$
C_S
1
charge
redistribution
V_{BL}
V(1)
V_{PRE}
$\Delta V(1)$
$\frac{V_{DD}}{2}$
V(0)
time


WL
WR
RD
X
$V_{DD} - V_T$
charge
redistributio
⇒ destructi
BL
1
$\frac{V_{DD}}{2}$
$\frac{V_{DD}}{2}$
sensing
$\frac{V_{DD}}{2}$



$\frac{V_{DD}}{2} \rightarrow \frac{V_{DD}}{2} + \Delta V \xrightarrow{\text{sense amp}} V_{DD}$

$\frac{V_{DD}}{2} \rightarrow \frac{V_{DD}}{2} - \Delta V \xrightarrow{\text{sense amp}} 0$

destructive read, must be restored

~~inverted~~ output

Destructive Reading

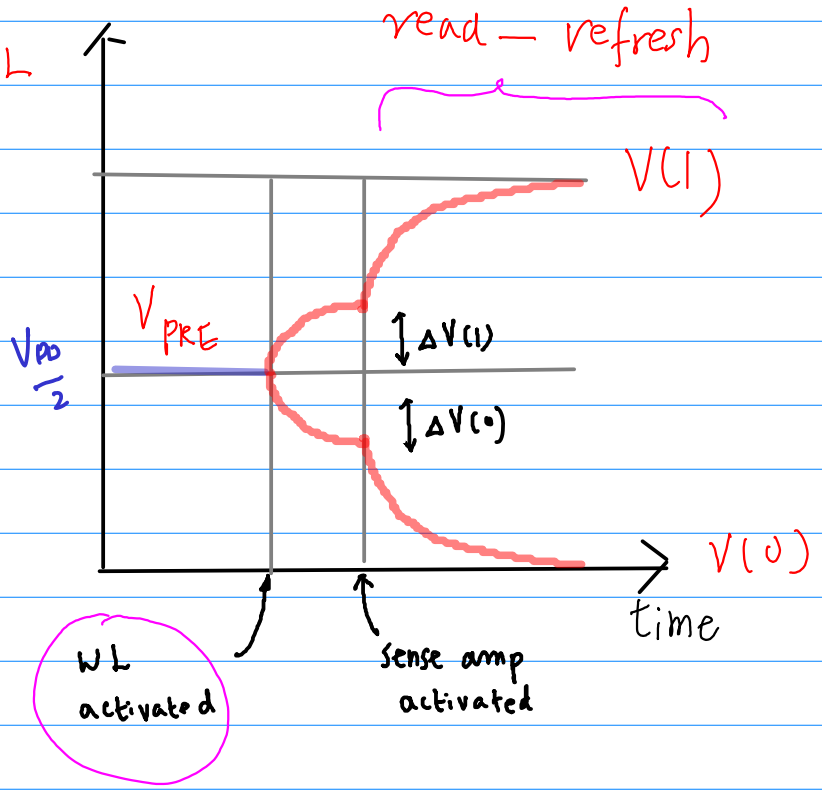
Read operations modifies the charge stored

the original value must be restore : Refreshing

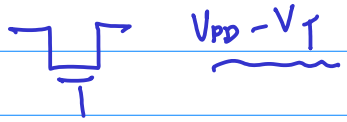
the sensor amp's output connected to the bit line

during WorLine = H, the cell charge is restored

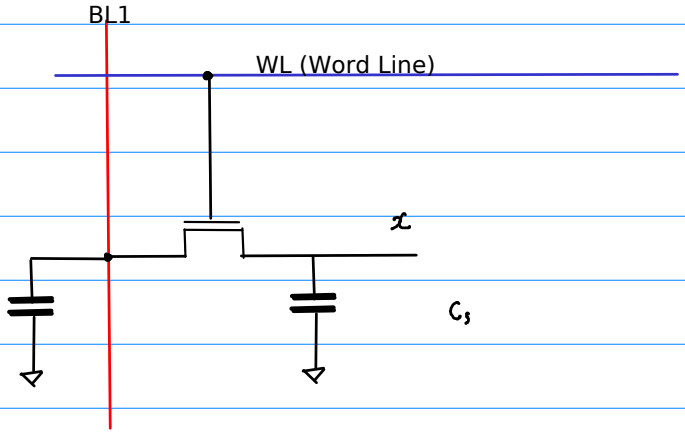
typical bit-line voltage waveform during read-out

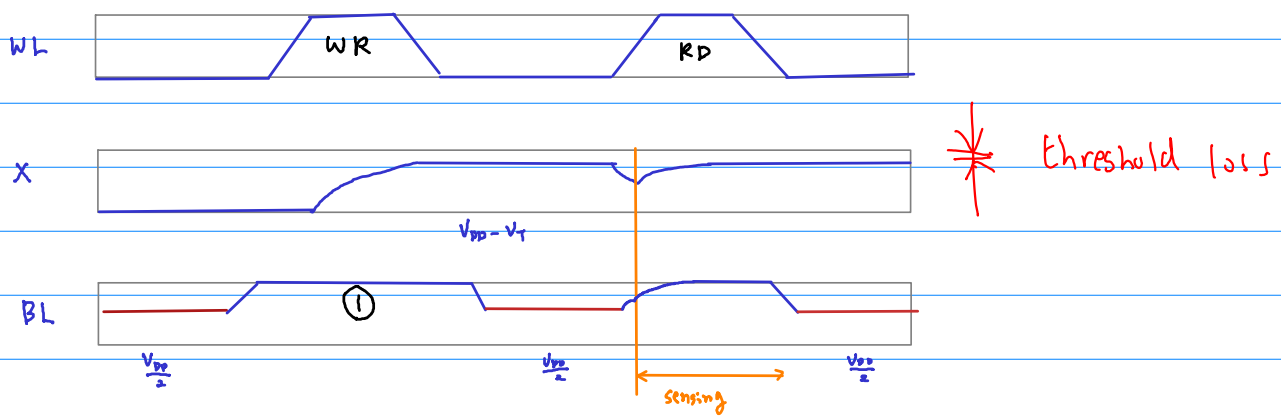


Threshold Voltage Loss
: reduces the availabe charge

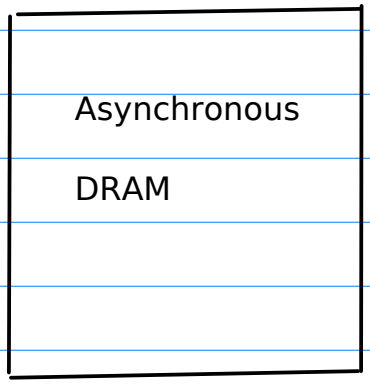


Bootstrapping
: apply a higher voltage to the word line





Asynchronous DRAM



Synchronous DRAM