Finite Sate Machine (A3)

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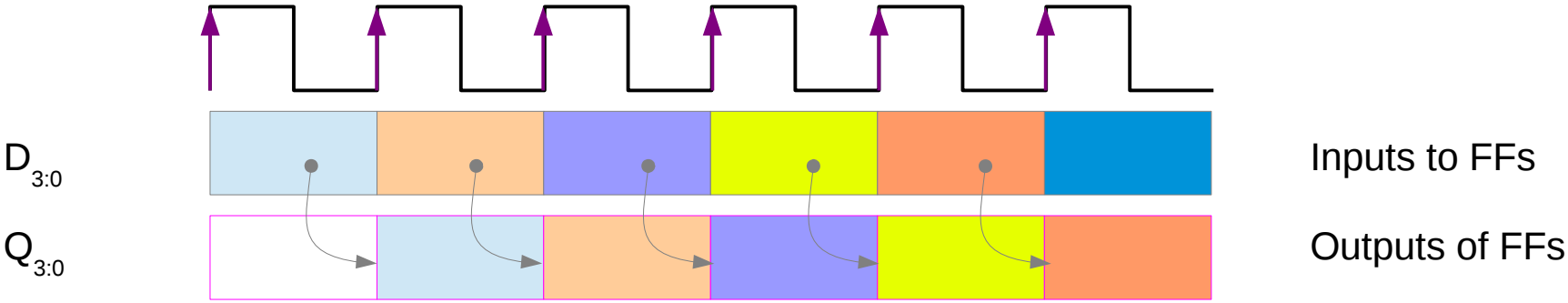
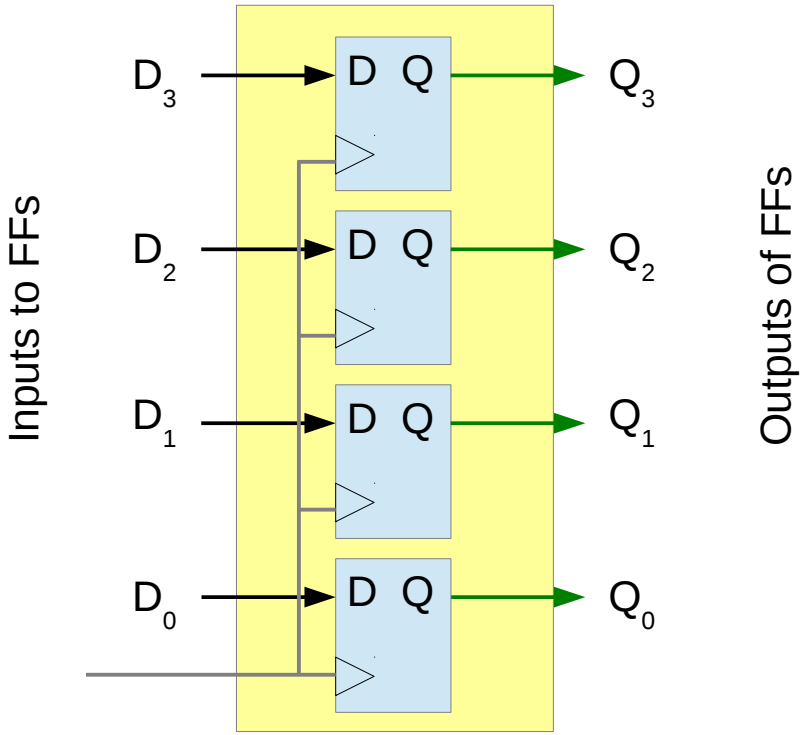
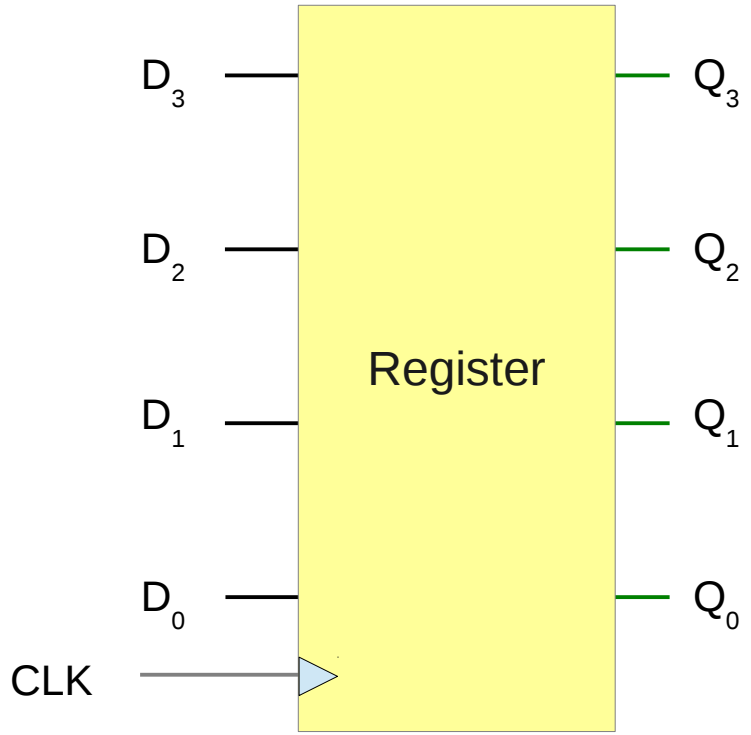
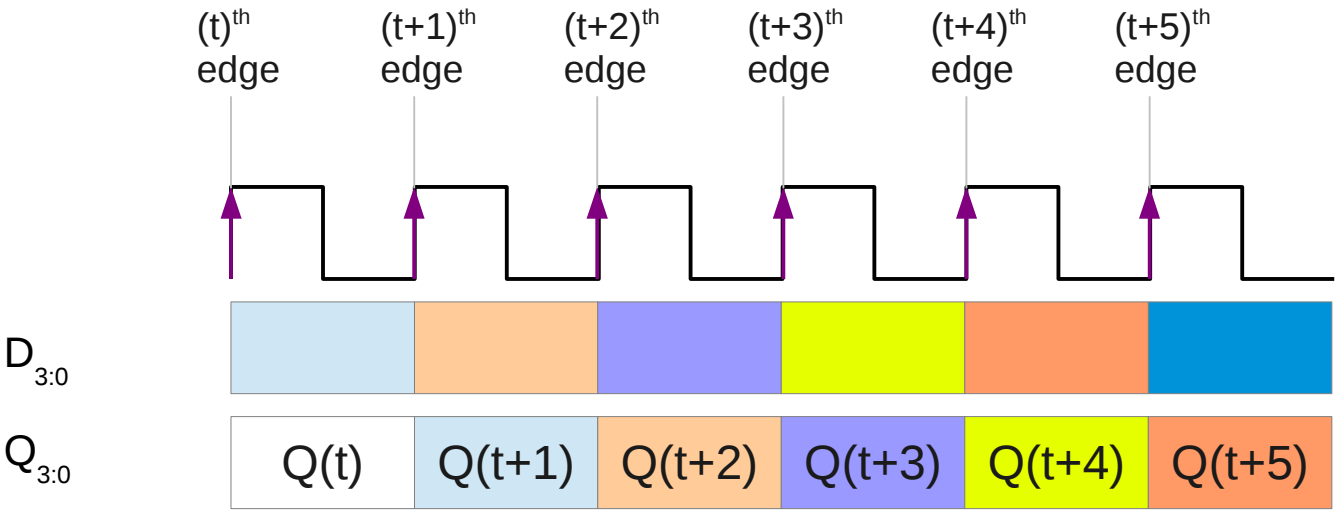
FF Timing (Ideal)





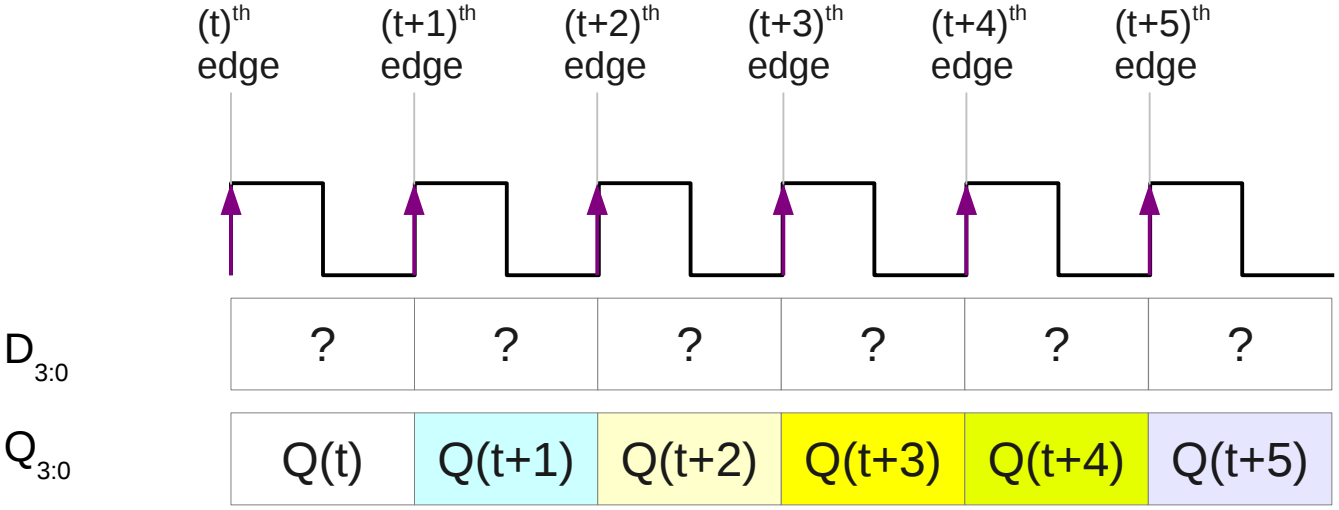


Sequence of States



Inputs to FFs

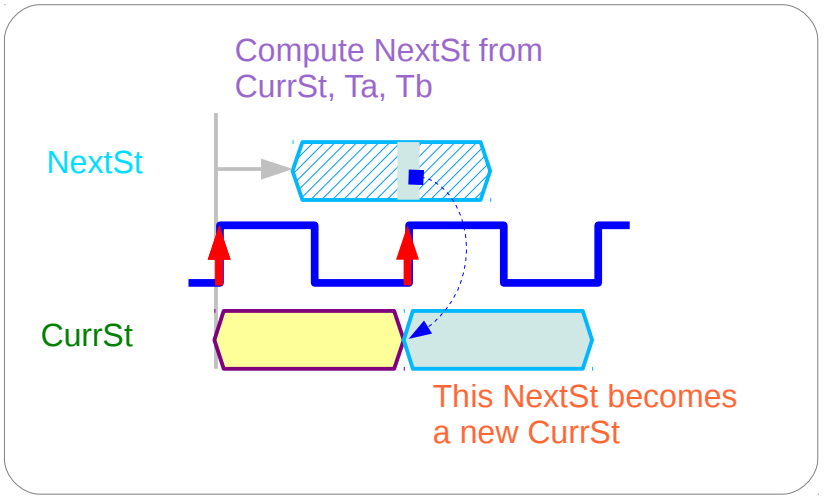
Outputs of FFs

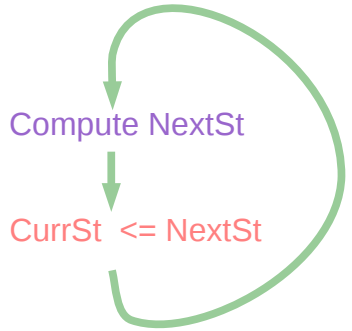


Find inputs to FFs

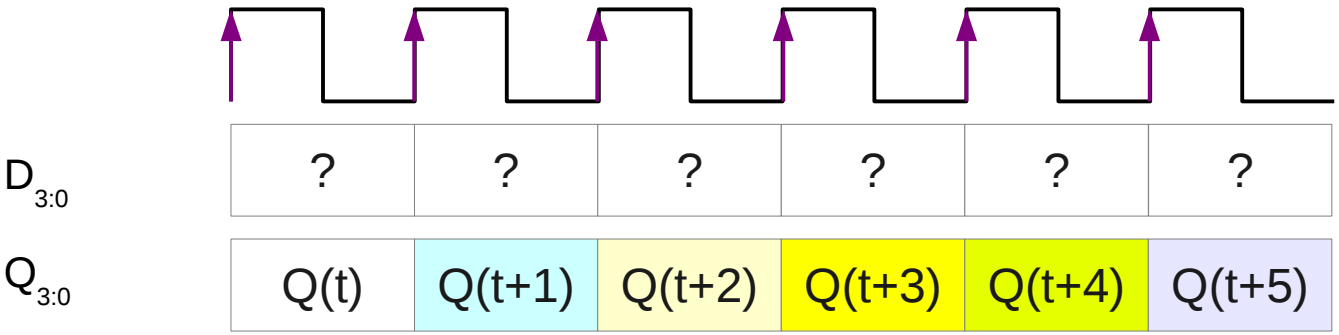
which will make outputs in this sequence

When NextSt becomes CurrSt



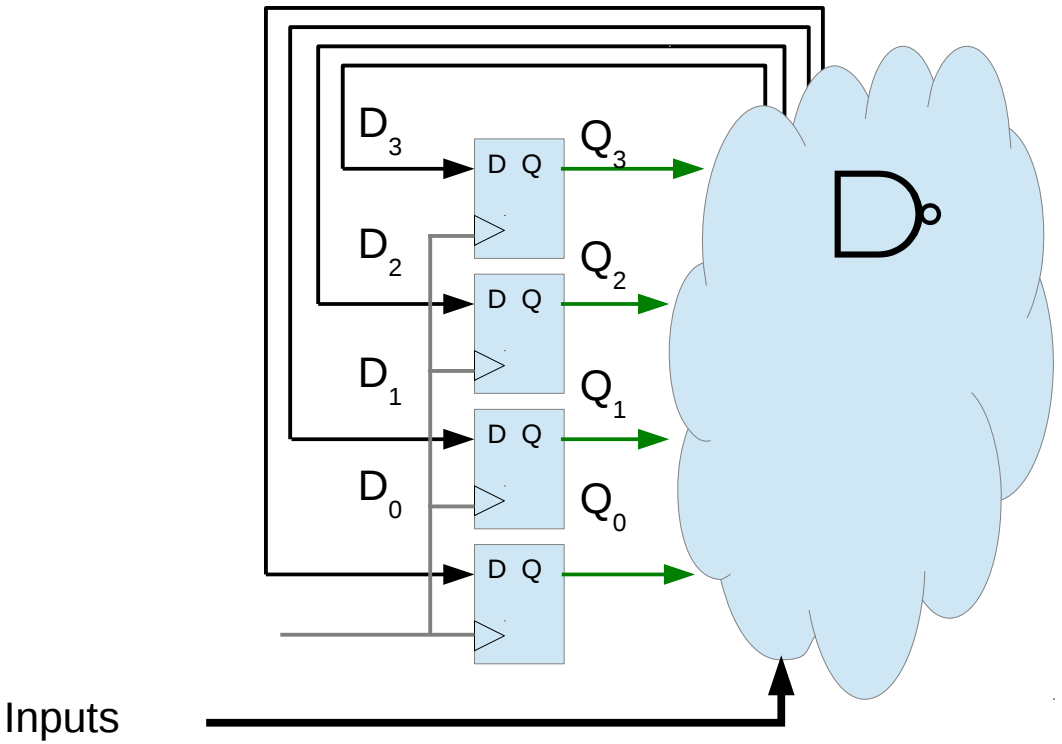


Finding FF Inputs



Inputs to FFs

Outputs of FFs



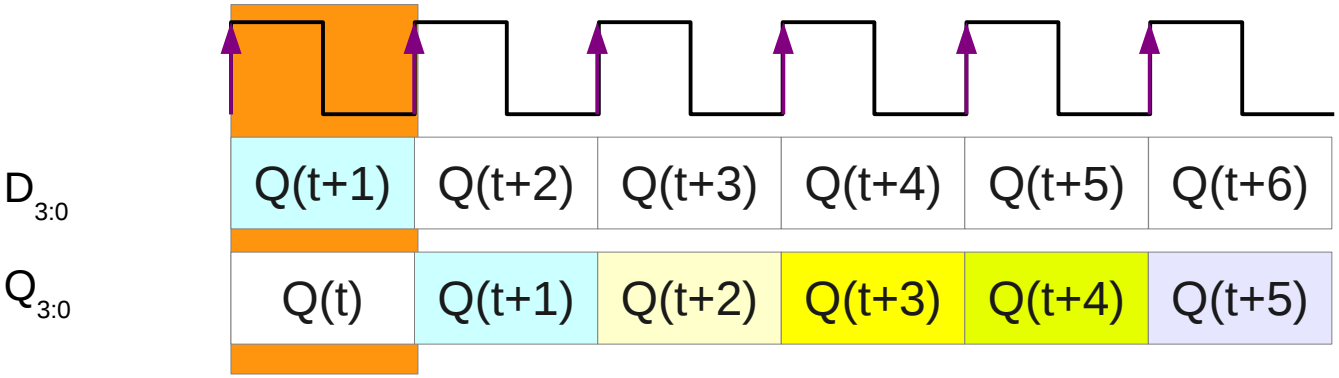
During the t^{th} clock edge period,

Compute the next state Q(t+1) using the current state Q(t) and other external inputs

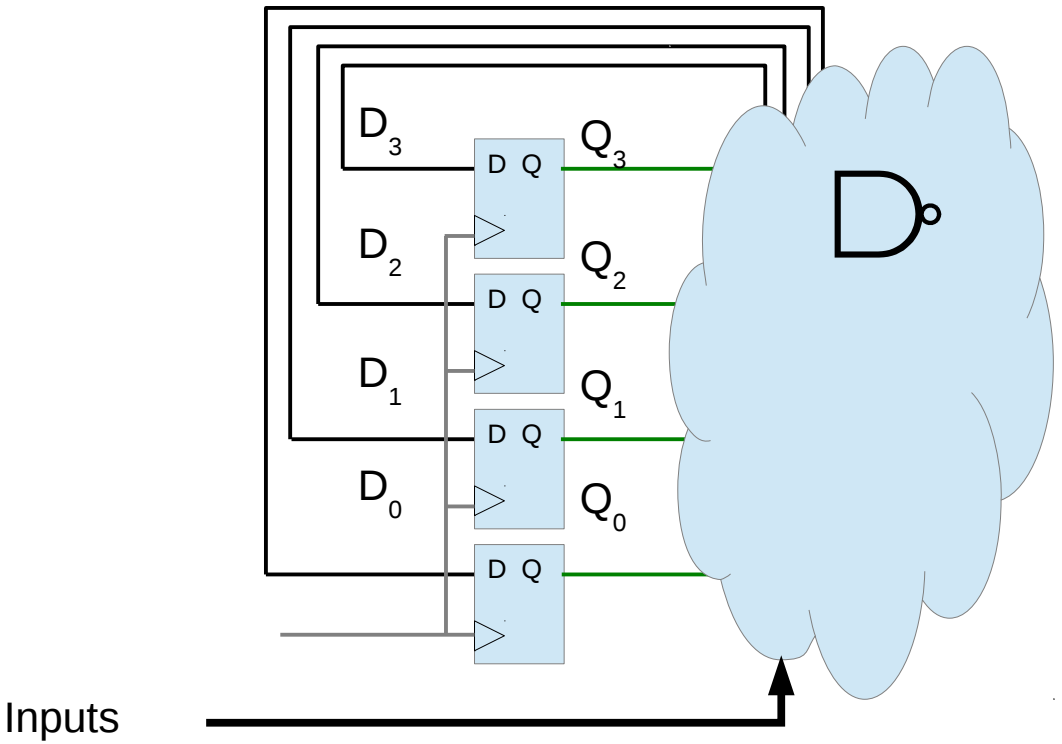
Place it to FF inputs

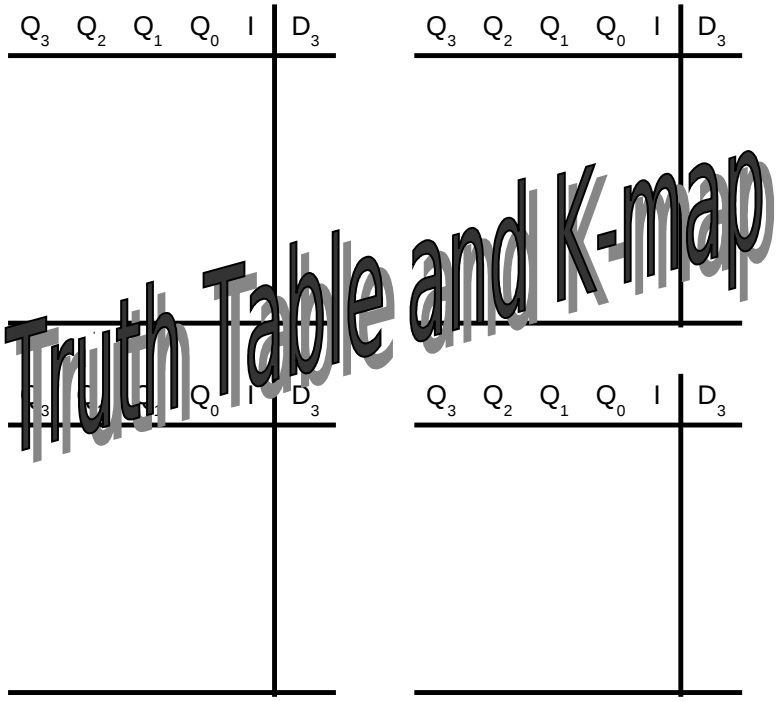
After the next clock edge, $(t+1)^{th}$, the computed next state Q(t+1) becomes the current state

Method of Finding FF Inputs

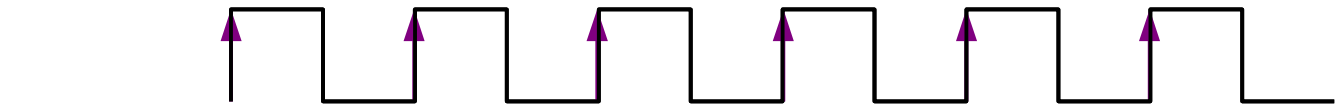


Find the boolean functions
D3, D2, D1, D0
in terms of Q3, Q2, Q1, Q0,
and external inputs
for all possible cases.



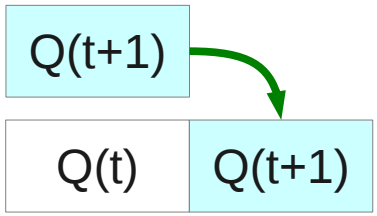


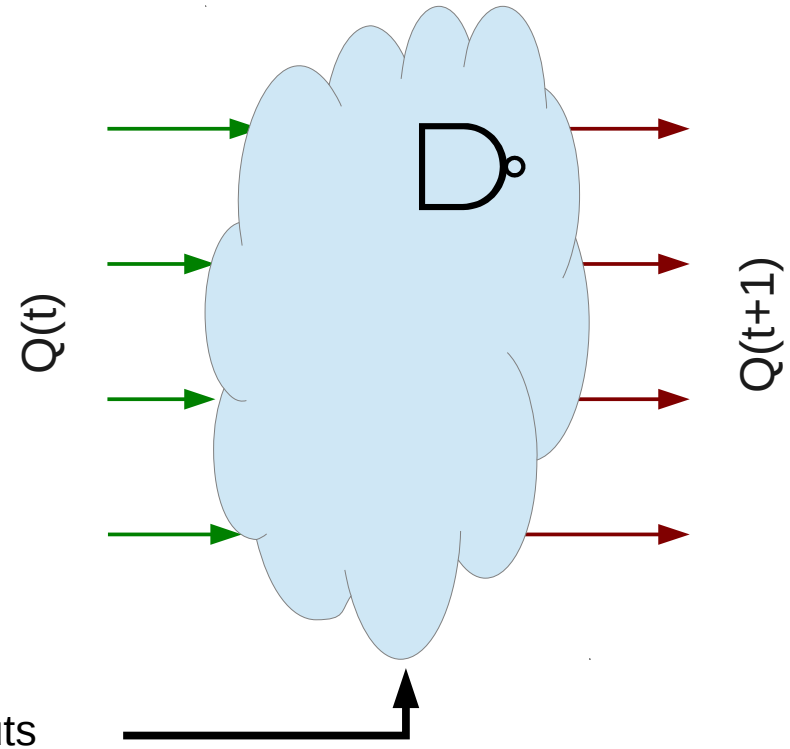
State Transition



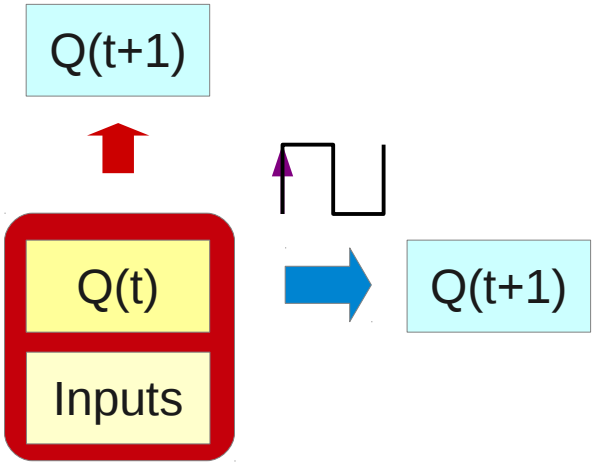
$D_{3:0}$

$Q_{3:0}$



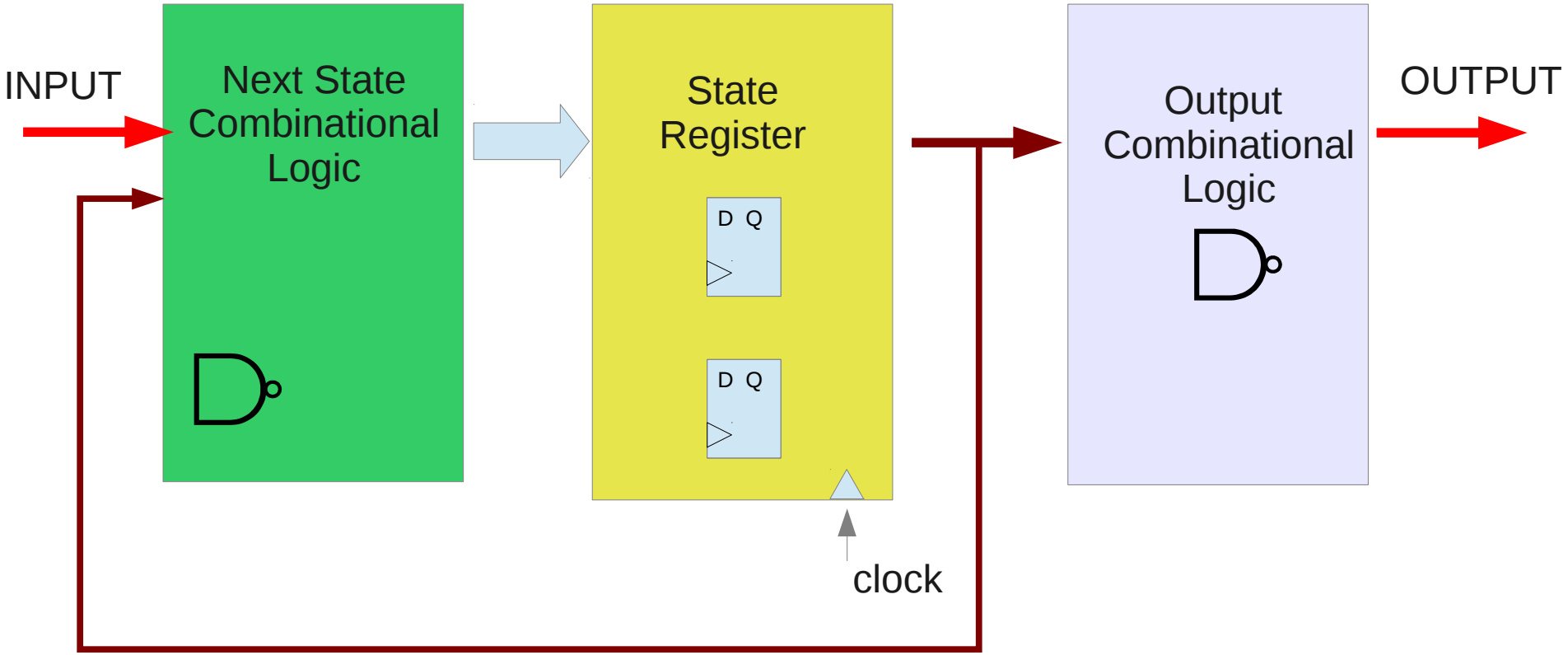


Compute the next state
using the current state
and external inputs
in the current clock cycle

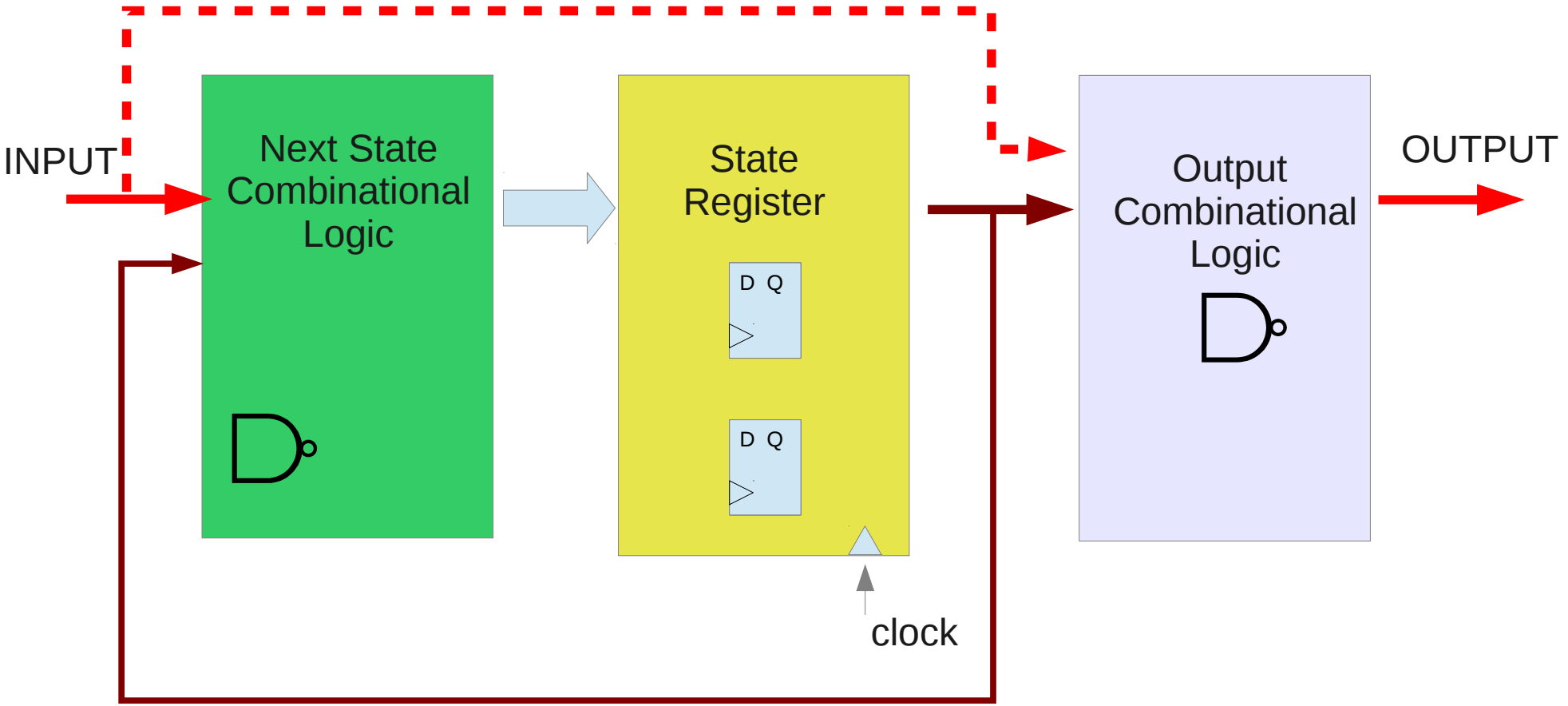


After the next clock edge,
the computed next state (FF Inputs)
becomes the current state (FF Outputs)

Moore FSM

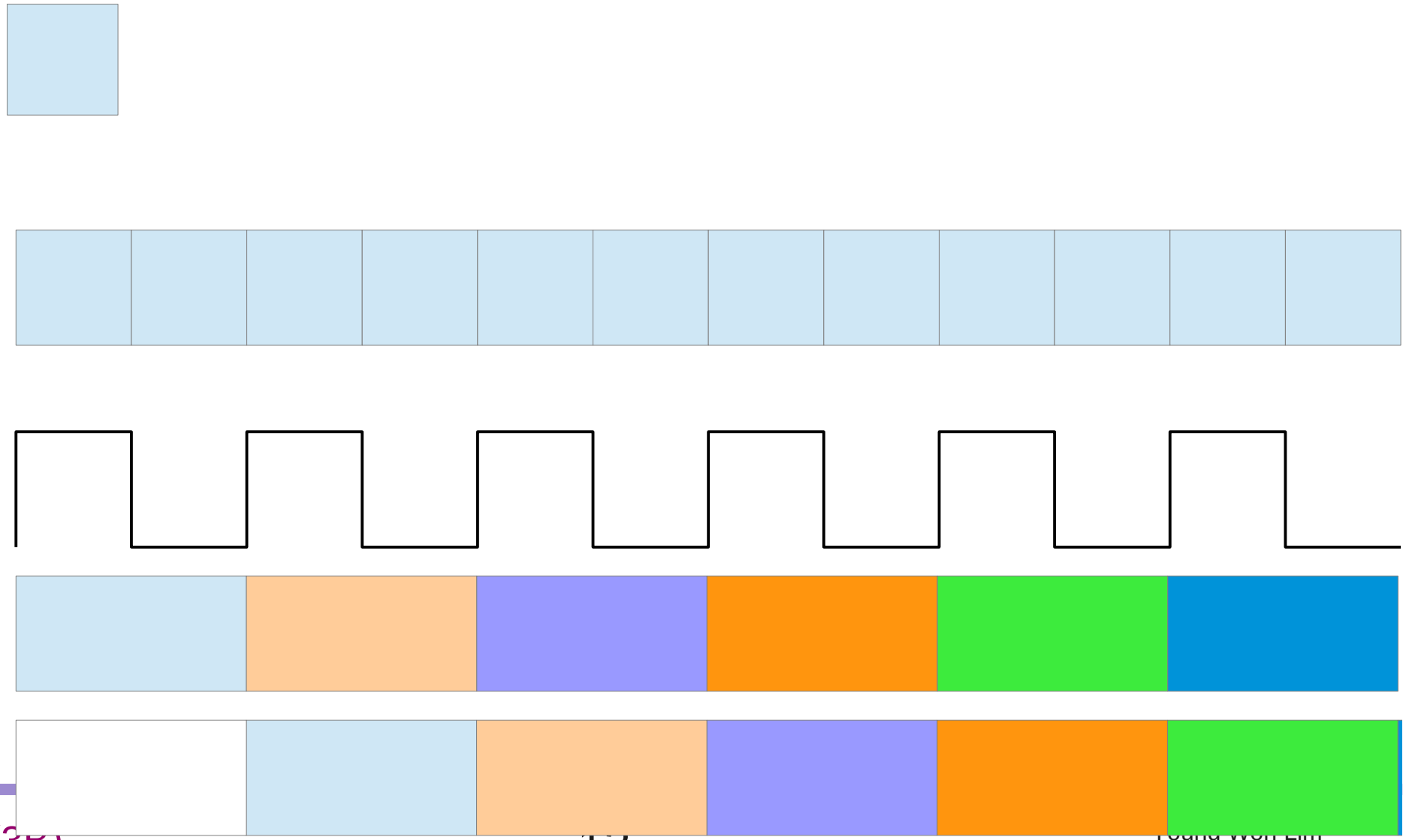

INPUT
Next State
Combinational
Logic
State
Register
D Q
D Q
Output
Combinational
Logic
OUTPUT
clock

Mealy Machine



Register Timing

NOR-based SR Latch



References

[1] http://en.wikipedia.org/
[2] M. M. Mano, C. R. Kime, “Logic and Computer Design Fundamentals”, 4th ed.
[3] D.M. Harris, S. L. Harris, “Digital Design and Computer Architecture”