Multiplexer (A)

Please send corrections (or suggestions) to youngwlim@hotmail.com.

This document was produced by using OpenOffice and Octave.

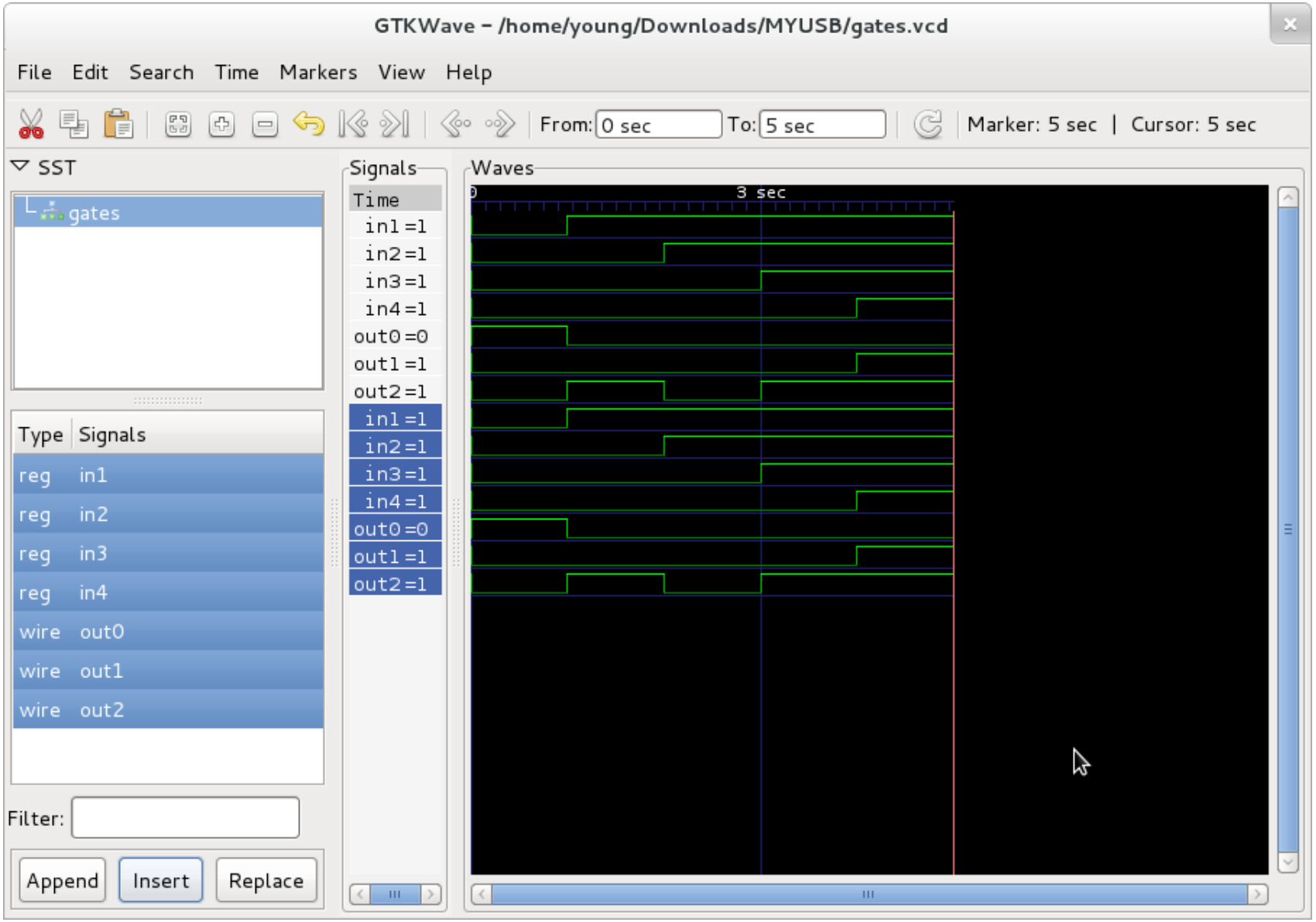
Simple Gates

```
module gates();

  wire out0;
  wire out1;
  wire out2;

  reg  in1, in2, in3, in4;

  not U1 (out0, in1);

  and U2 (out1, in1, in2, in3, in4);

  xor U3 (out2, in1, in2, in3);
```

```
initial begin
  $dumpfile("gates.vcd");
  $dumpvars(0, gates);

  $monitor(
  "in1=%b in2=%b in3=%b in4=%b out0=%b out1=%b out2=%b",
   in1,in2,in3,in4, out0,out1,out2);

  in1 = 0;
  in2 = 0;
  in3 = 0;
  in4 = 0;

 #1 in1 = 1;
 #1 in2 = 1;
 #1 in3 = 1;
 #1 in4 = 1;
 #1

  $finish;
 end

endmodule
```

from www.asic-world.com

Simple Gates



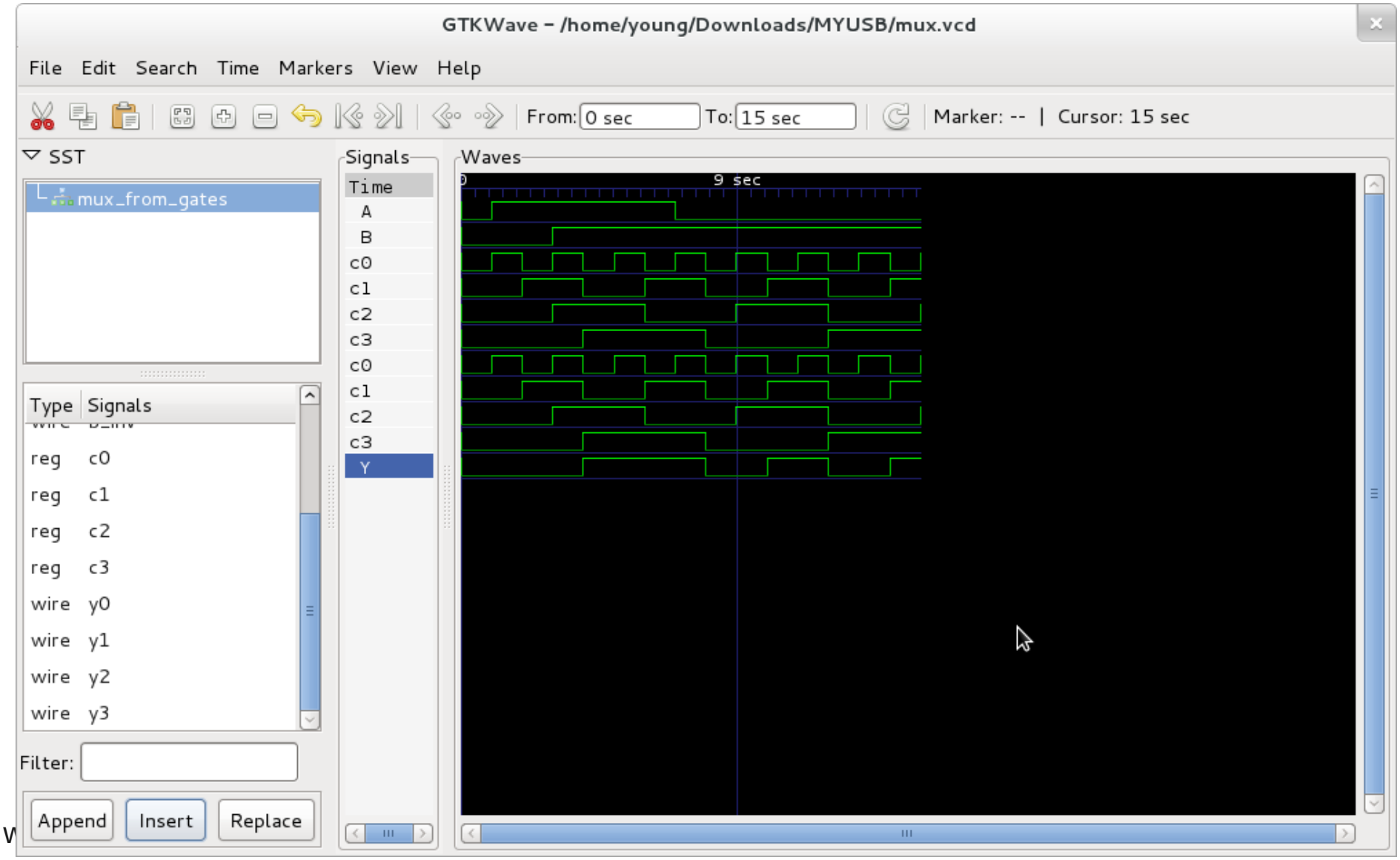
Multiplexer

```
module mux_from_gates ();
  reg c0,c1,c2,c3, A,B;
  wire Y;

  //Invert the sel signals
  not (a_inv, A);
  not (b_inv, B);


  // 3-input AND gate
  and (y0, c0, a_inv, b_inv);  // 00
  and (y1, c1, a_inv, B);      // 01
  and (y2, c2, A,     b_inv);  // 10
  and (y3, c3, A,     B);      // 11


  // 4-input OR gate
  or (Y, y0, y1, y2, y3);
```

from www.asic-world.com

```
initial begin
  $dumpfile("mux.vcd");
  $dumpvars(0,mux_from_gates);

  $monitor (
   "c0 = %b c1 = %b c2 = %b c3 = %b A = %b B = %b Y = %b",
   c0, c1, c2, c3, A, B, Y);

  c0 = 0;
  c1 = 0;
  c2 = 0;
  c3 = 0;
  A = 0;
  B = 0;

  #1 A  = 1;
  #2 B  = 1;
  #4 A  = 0;
  #8 $finish;
end

always #1 c0 = ~c0;
always #2 c1 = ~c1;
always #3 c2 = ~c2;
always #4 c3 = ~c3;
endmodule
```

Multiplexer



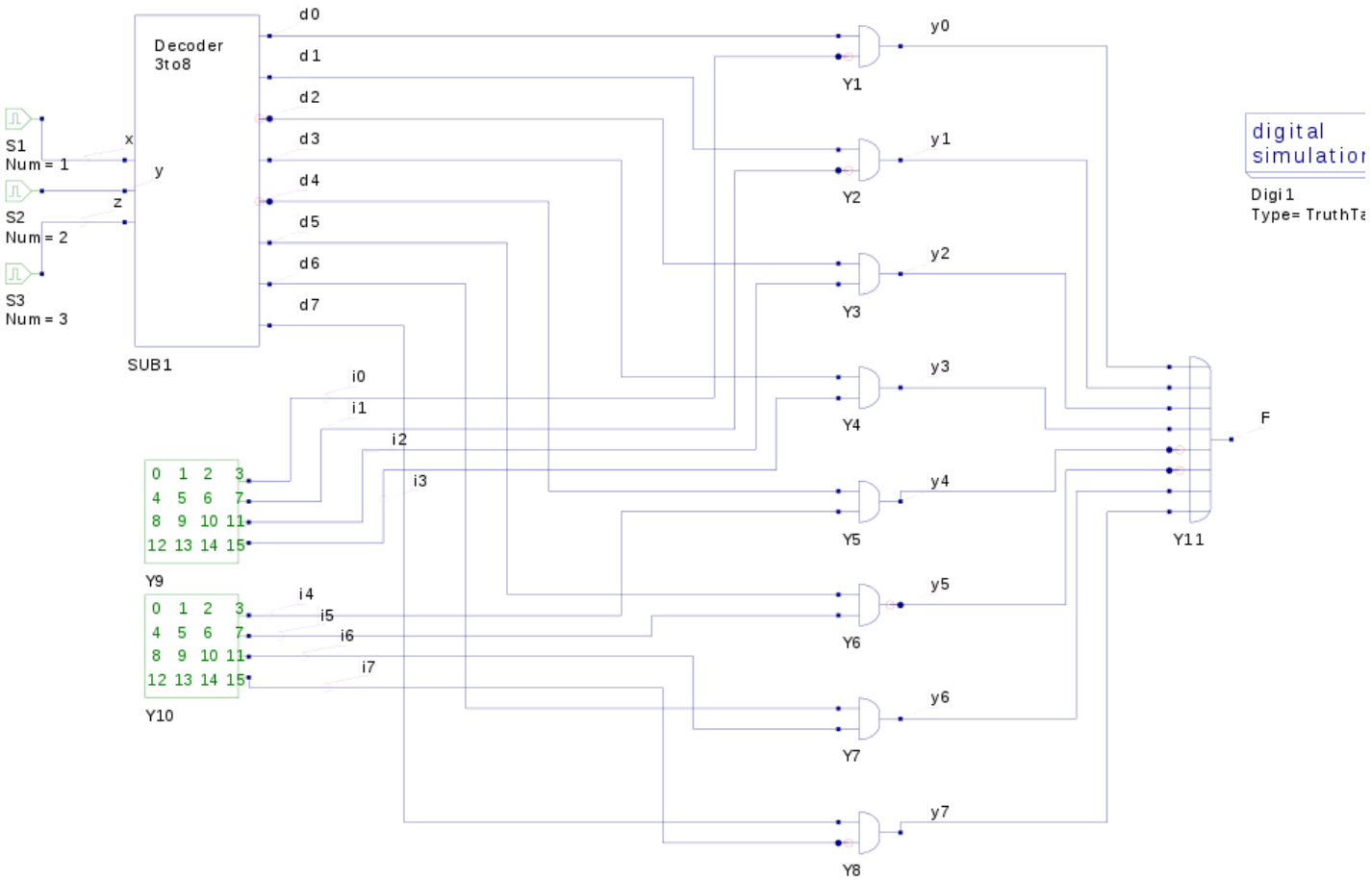
from w

Multiplexer

```
module mux(sel, D0, D1, D2, D3, Y)
  input [1:0] sel;
  input D0, D1, D2, D3;
  output Y;
  reg Y;

  always @(sel or D0 or D1 or D2 or D3)
     case (sel)
         2'b00 : Y = D0;
         2'b01 : Y = D1;
         2'b10 : Y = D2;
         2'b11 : Y = D3;
        default: Y = D0;
     endcase

endmodule
```

from www.asic-world.com

Multiplexer Schematic



Multiplexer Schematic

References

[1] http://en.wikipedia.org/
[2] www.asic-world.com