CMOS Combi-2 (H.2)

20151111

References

Some Figures from the following sites

[1] http://pages.hmc.edu/harris/cmosvlsi/4e/index.html
Weste & Harris Book Site

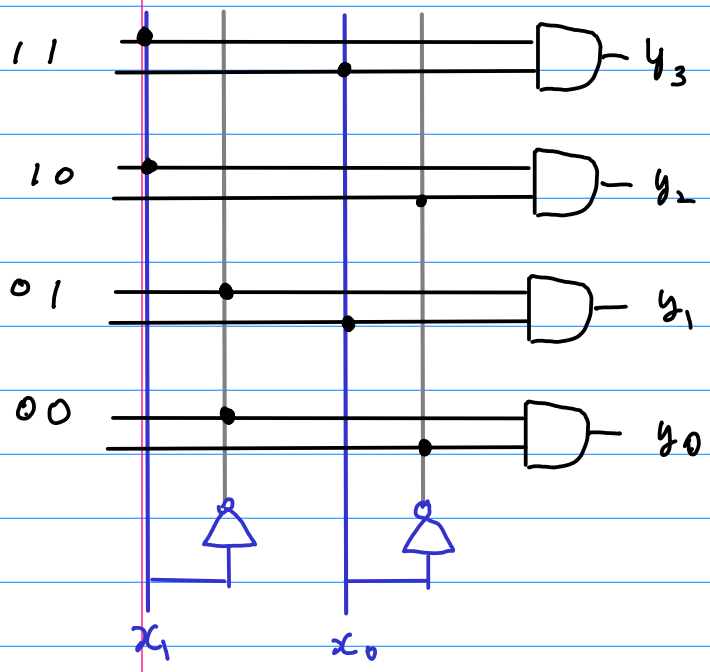
[2] en.wikipedia.org

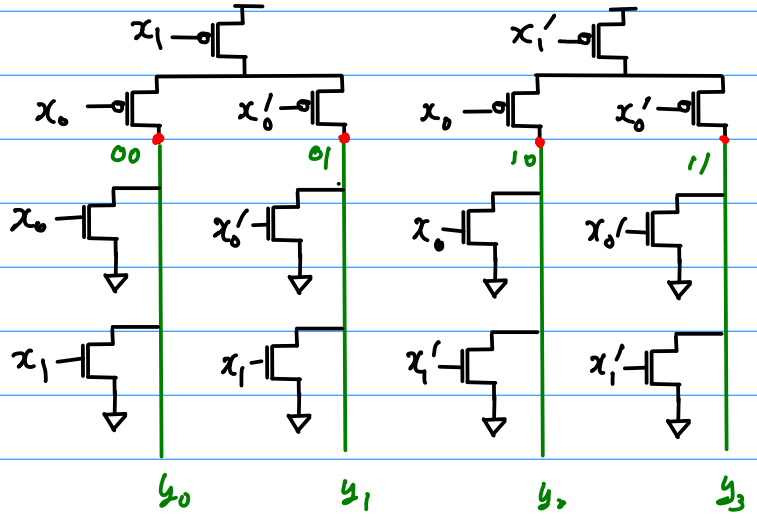
[3] Digital Integrated Circuits : A Design Perspective,
Jan M. Rabaey,
(http://bwrcs.eecs.berkeley.edu/Classes/IcBook/)

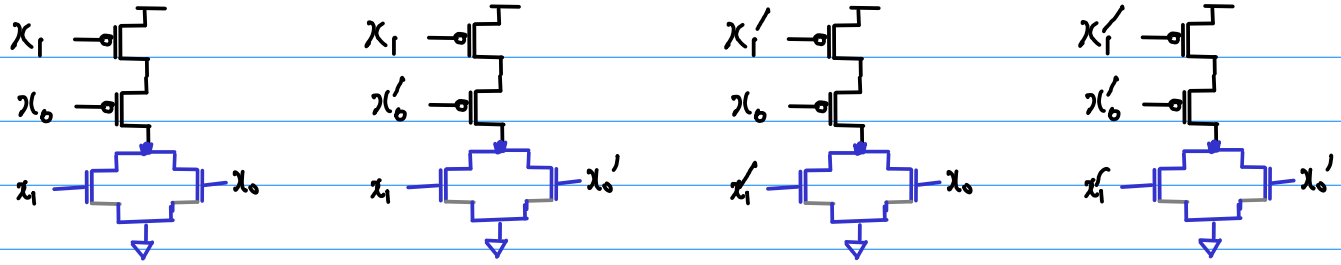
[4] Digital Electronics and Design with VHDL
Pedroni

Decoder

x_1	x_0	y_3	y_2	y_1	y_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0







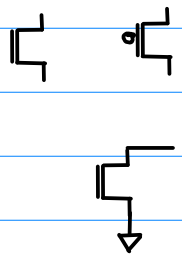
x_1x_0 00 — all nMOS OFF → $y_0 \to 1$

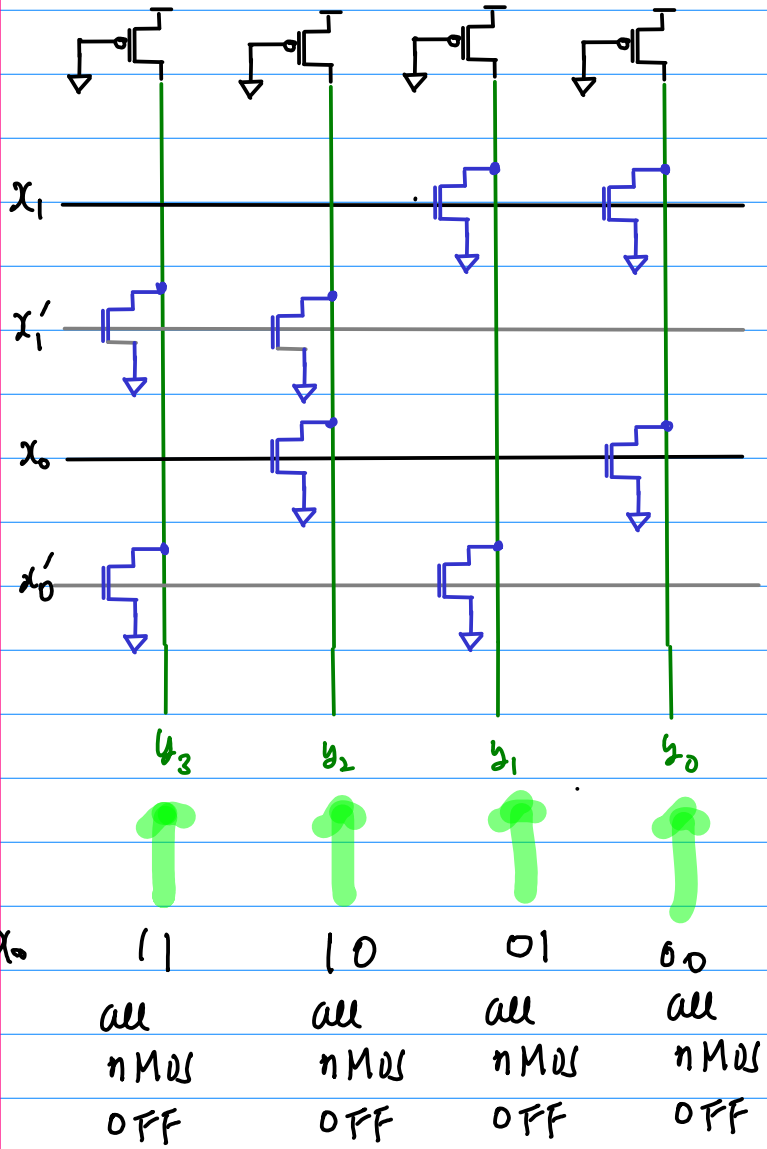
01 — all nMOS OFF → $y_1 \to 1$

10 — all nMOS OFF → $y_2 \to 1$

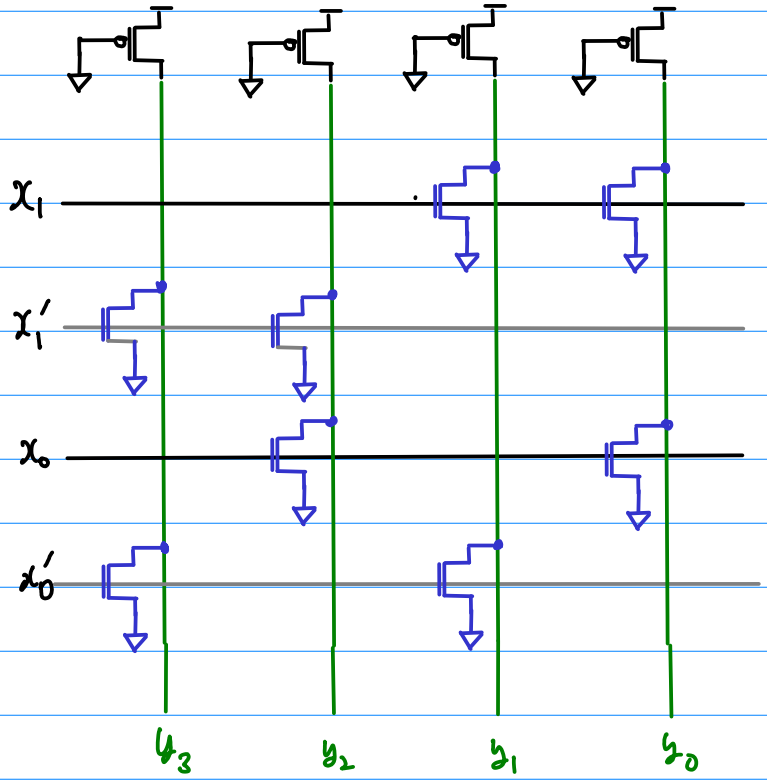
11 — all nMOS OFF → $y_3 \to 1$

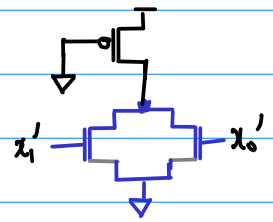
x_1	x_0	y_3	y_2	y_1	y_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0





x_1x_0	11	10	01	00
	all nMOS OFF	all nMOS OFF	all nMOS OFF	all nMOS OFF

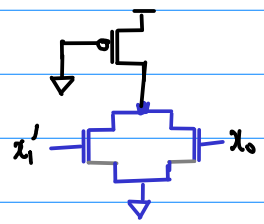




$(x_1 = 0) \vee (x_0 = 0)$

$y_3 \Rightarrow 0$

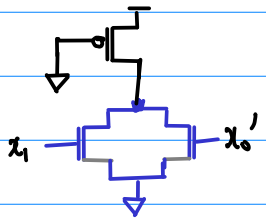
$x_1 x_0 = 11$



$(x_1 = 0) \vee (x_0 = 1)$

$y_3 \Rightarrow 0$

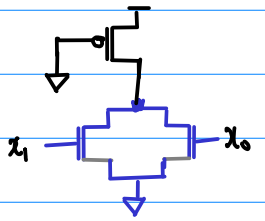
$x_1 x_0 = 10$



$(x_1 = 1) \vee (x_0 = 0)$

$y_3 \Rightarrow 0$

$x_1 x_0 = 01$

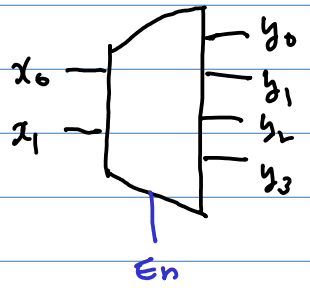


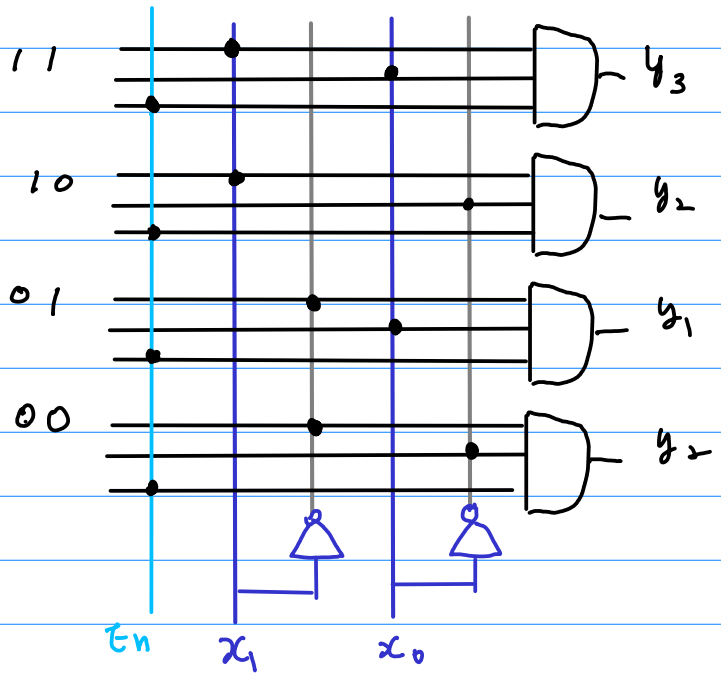
$(x_1 = 1) \vee (x_0 = 1)$

$y_3 \Rightarrow 0$

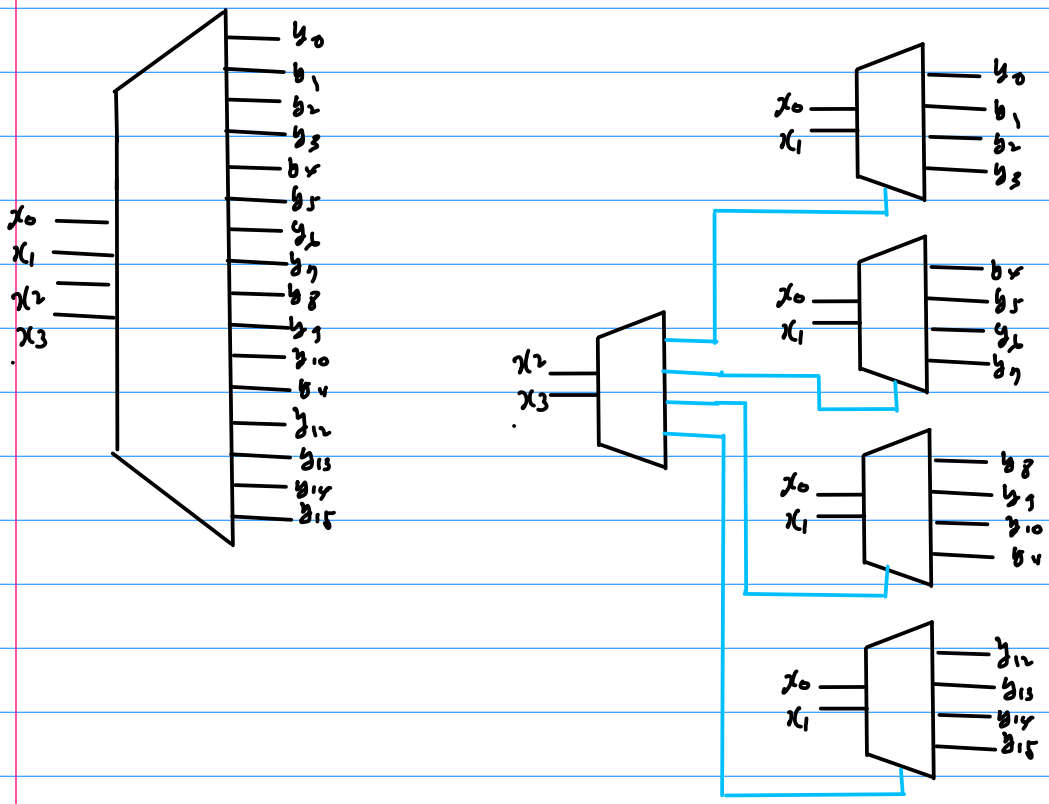
$x_1 x_0 = 00$

Decoder with Enable



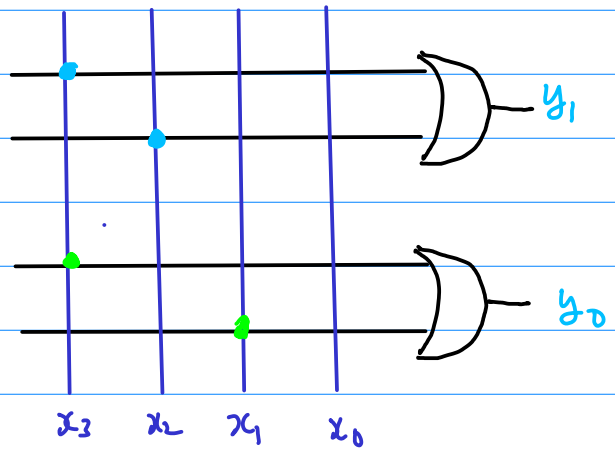


Large Address Decoder

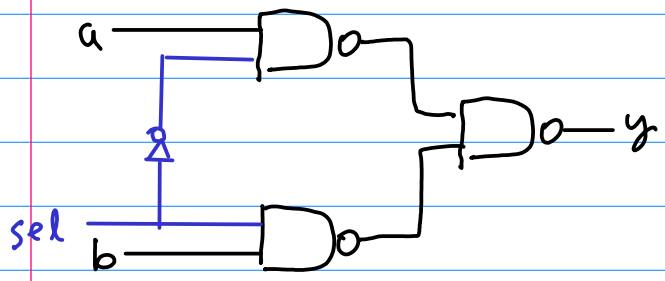


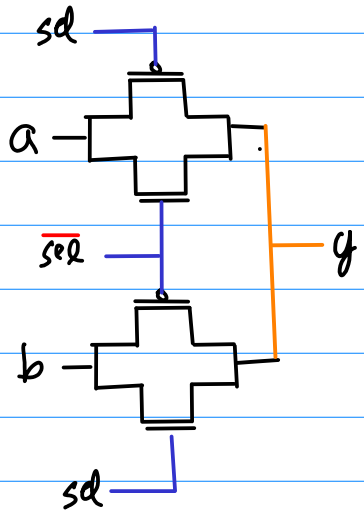
Address Encoder

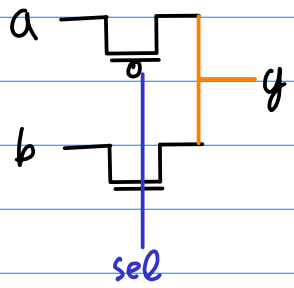
x_3	x_2	x_1	x_0	y_1	y_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1



Multiplexer



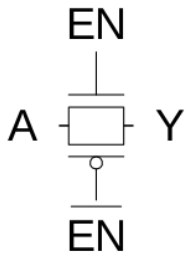


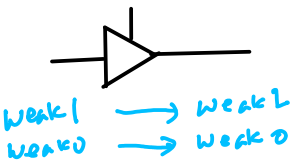


Nonrestoring Tristate

- Transmission gate acts as tristate buffer
  - Only two transistors
  - But *nonrestoring*
    - Noise on A is passed on to Y

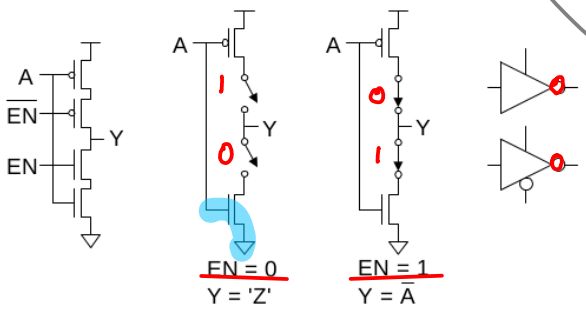
if A is weak 1 or weak 0, then it is propagated to the output Y

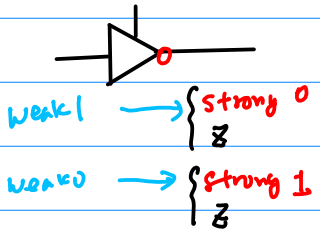




Tristate Inverter

- Tristate inverter produces restored output → can make a signal strong.
  - Violates conduction complement rule
  - Because we want a Z output

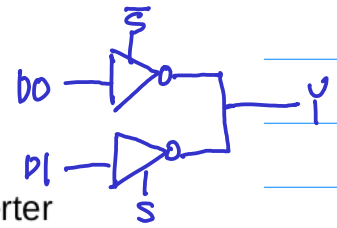


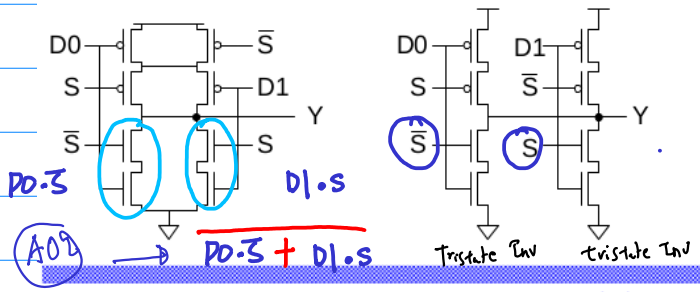


1 → Z
0 → Z

Inverting Mux

- Inverting multiplexer
  - Use compound AOI22
  - Or pair of tristate inverters
  - Essentially the same thing
- Noninverting multiplexer adds an inverter





4:1 Multiplexer

- 4:1 mux chooses one of 4 inputs using two selects
  - Two levels of 2:1 muxes
  - Or four tristates