# Interrupts

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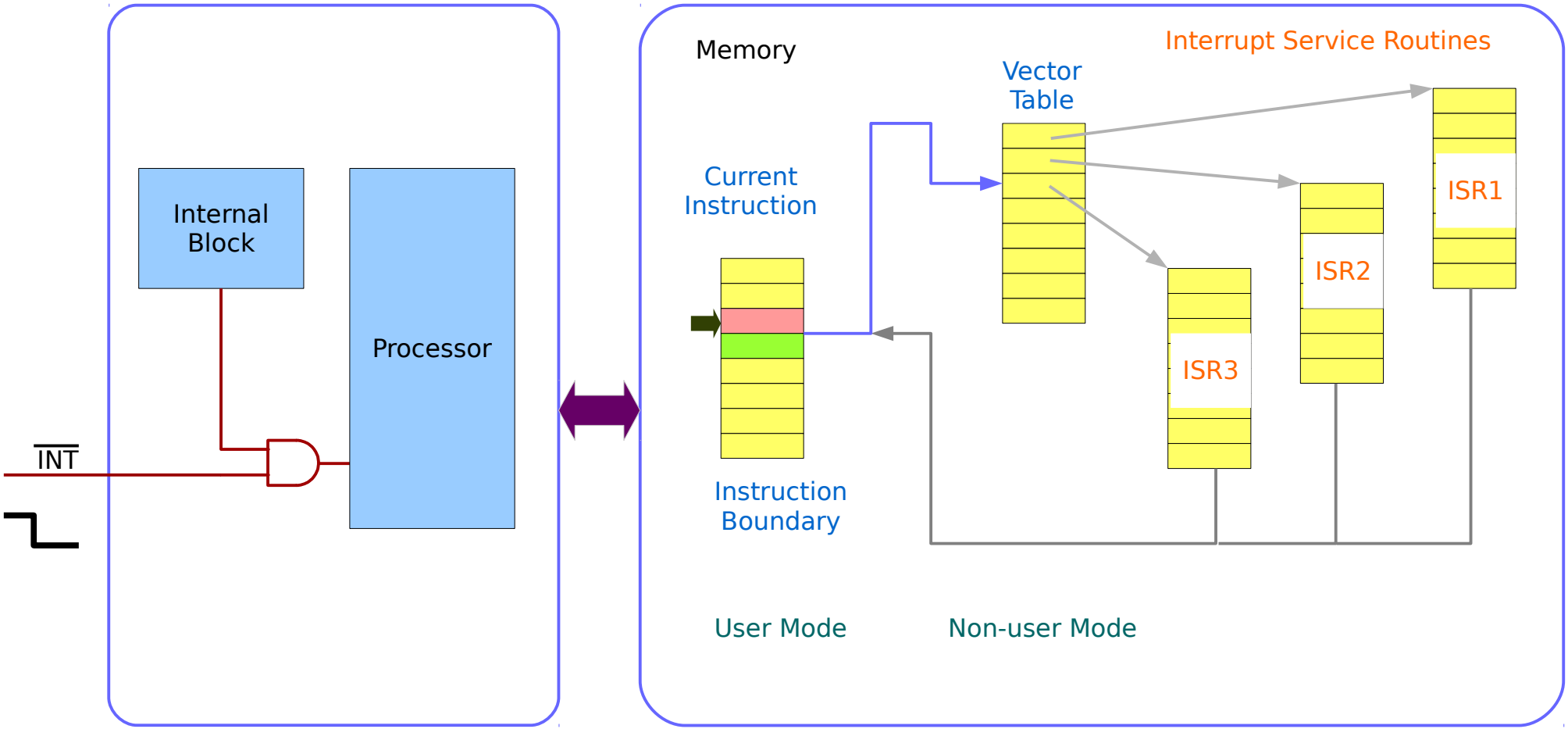
# Interrupt Overview



# Interrupt Overview

An event that requires
the CPU to stop the current program execution and
perform some service related to the event.

**ISR** : Interrupt Service Routine / Interrupt Handler

Coordinates I/O activities and prevent the CPU from
continous checking events

Performs Time critical  applications

# Interrupt Overview

**Interrupt Vector**
the starting address of an interrupt service routine

**Interrupt Vector Table**
Table storing several interrupt vectors
Each entry represents an address of an ISR

**Interrupt Enable Bit**
Processor's bit
Used to selectively enable a device
If the enable bit is 0, processor ignores the interrupt request

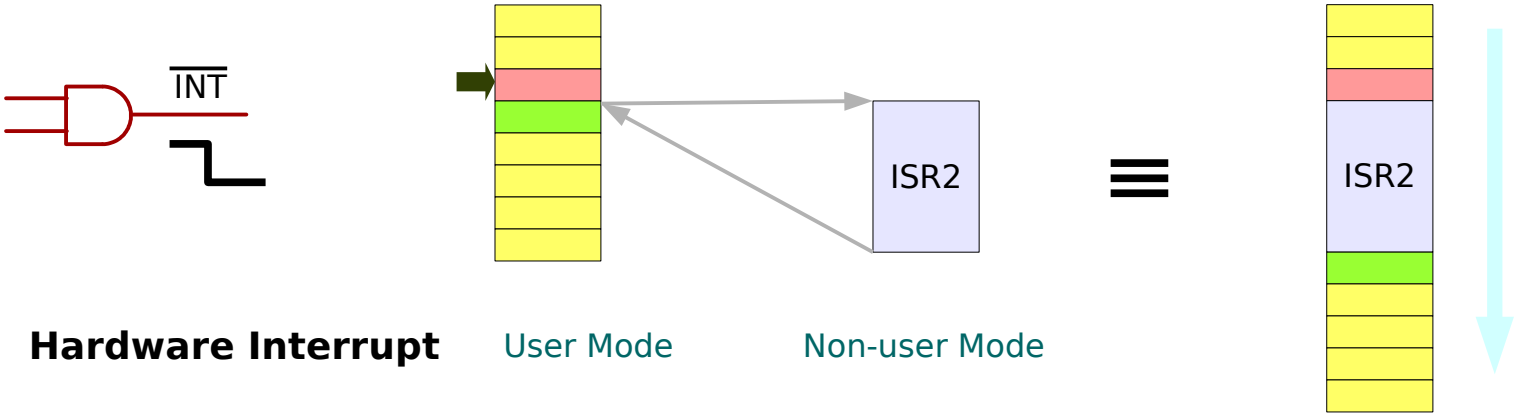
**Interrupt Flag Bit**
Devices' bit
Used to get the processor's attention for it's service

# Interrupt Overview

1. The device sets its flag bit
2. Upon detecting a flag is set,
the microprocessor triggers an interrupt
if the enable bit is also set
3. The processor status is saved
automatically on the stack.
4. The Processor searches
the appropriate interrupt vector
5. The processor jumps to the ISR.
6. At completing ISR, the special return
instruction must be used to restore the saved
processor status

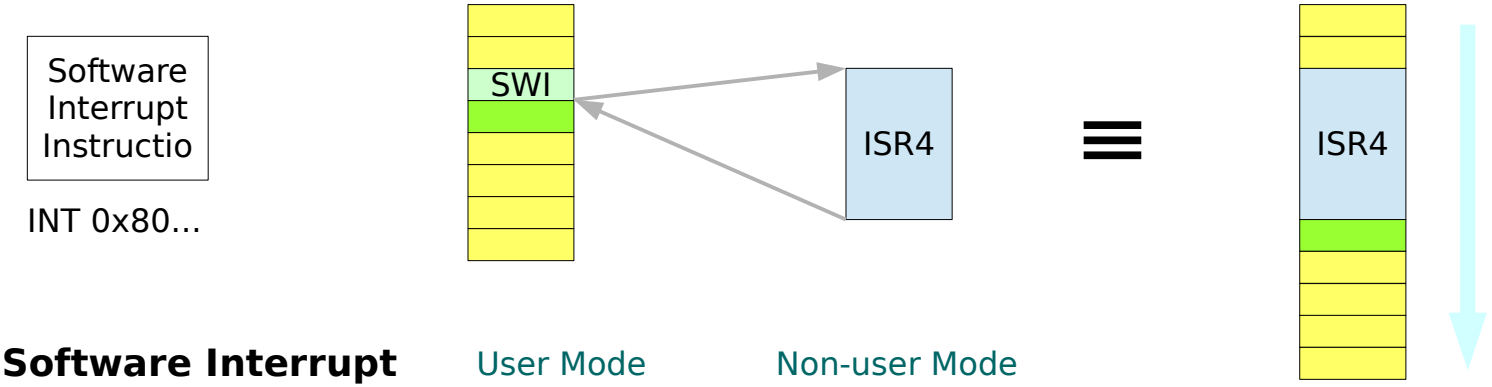
# HW & SW Interrupt

**Asynchronous**



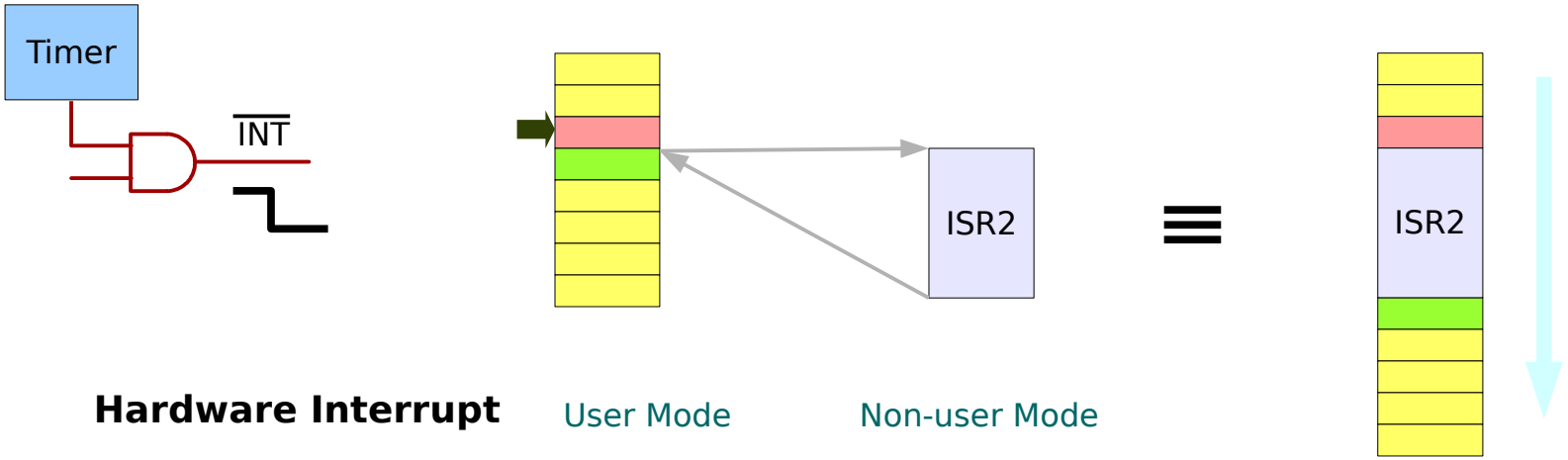

**Hardware Interrupt** User Mode Non-user Mode

**Synchronous**




**Software Interrupt** User Mode Non-user Mode

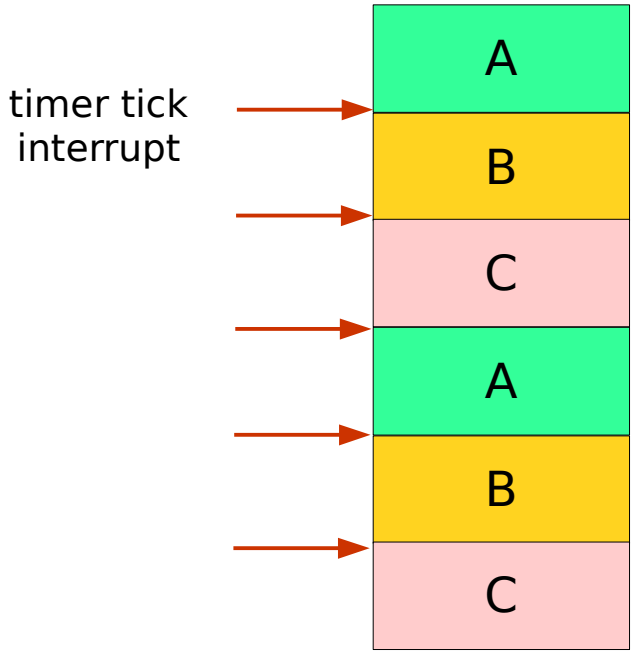
# Timer & Interrupt

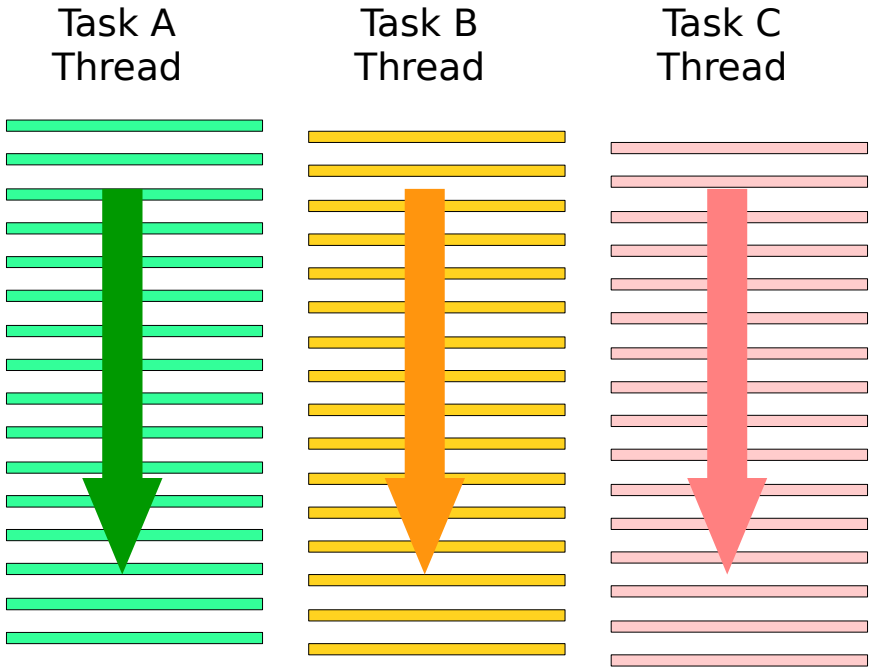



**Hardware Interrupt** User Mode Non-user Mode

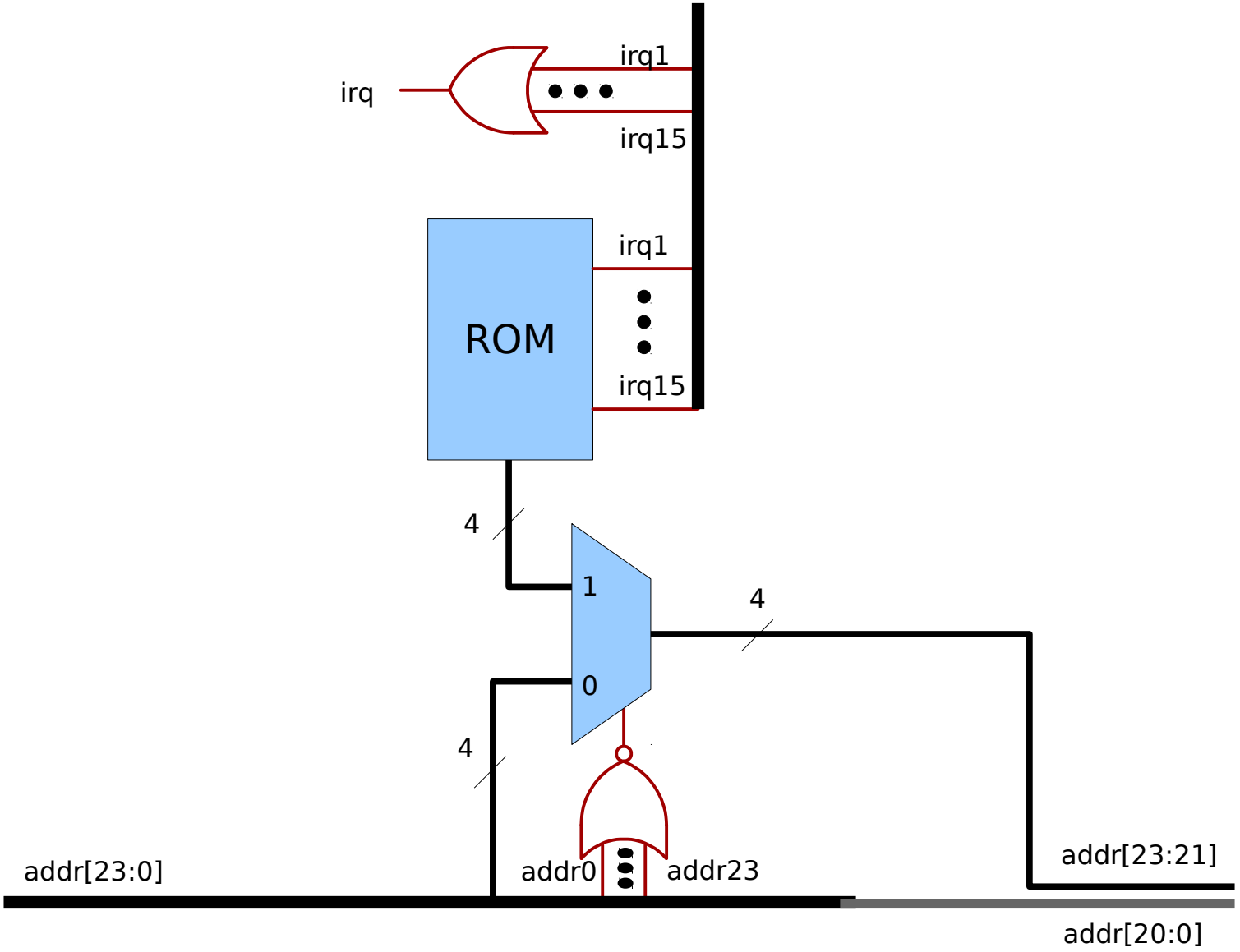
# Time Sharing

- **Time Slice**
- **Round Robin Scheduling**
- **Context Switching**

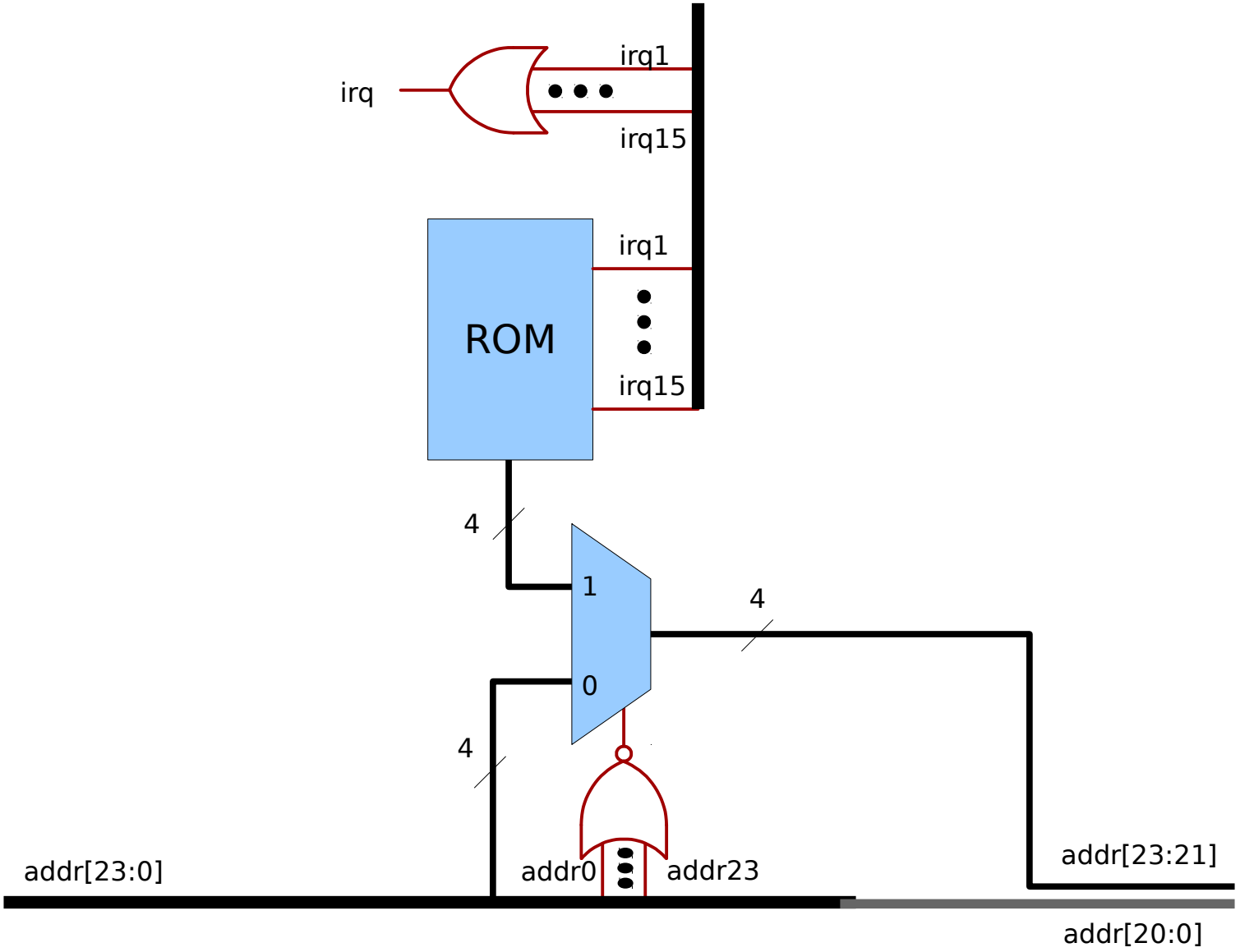


# Interrupt Vector System



# Vectored Interrupt Control Unit



## References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