Memory Mapped IO

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4/25/16

Please send corrections (or suggestions) to youngwlim@hotmail.com.

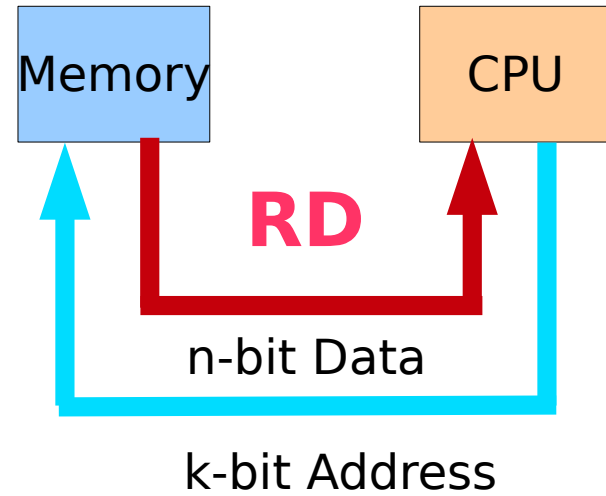This document was produced by using OpenOffice.
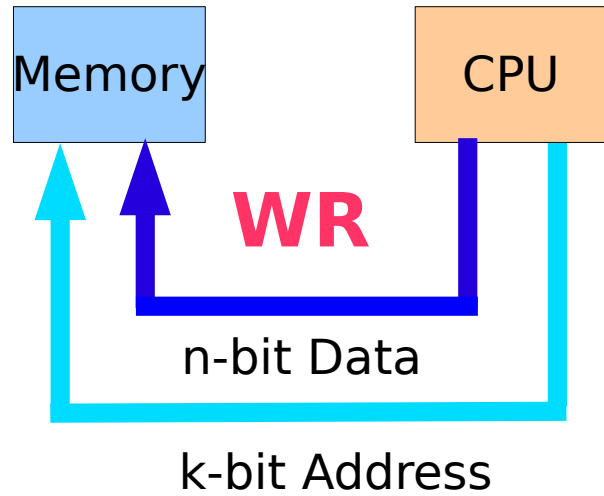
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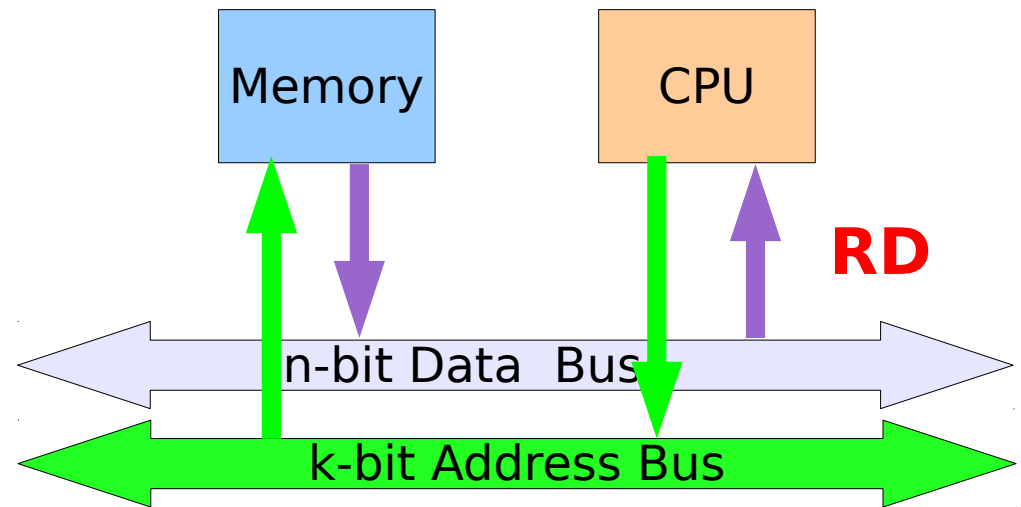
csrGen

Based on

Chuck Benz ASIC and FPGA Design
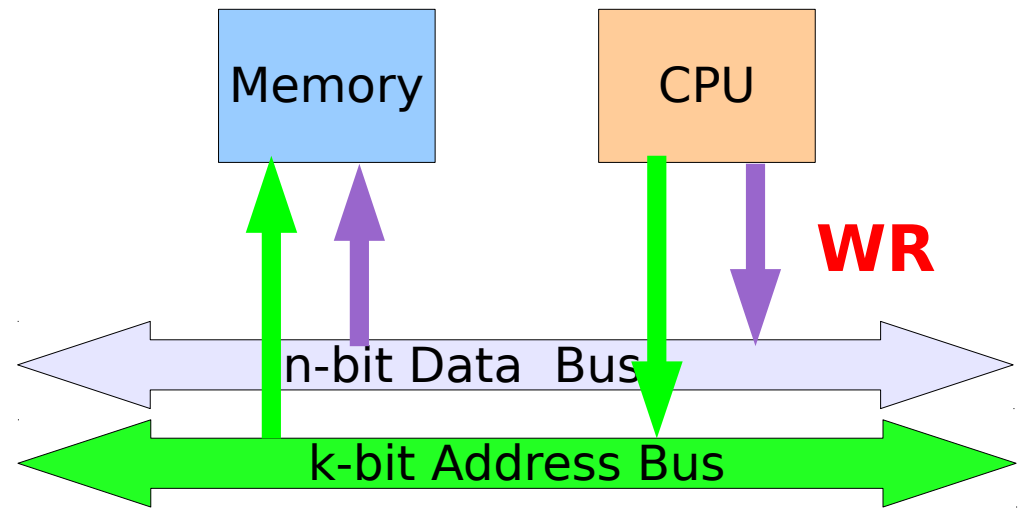
csrGen - generate verilog RTL code
for processor memory maps in ASIC/FPGA designs

http://asics.chuckbenz.com/

Memory Access Operations

Memory RD & WR Operations

Input n-bit word

k-bit address

Memory Unit
2^k words
n-bit per word

Mem_En

RD/WR

Output n-bit word

Memory   CPU

WR

n-bit Data Bus

k-bit Address Bus

Memory   CPU

RD

n-bit Data Bus

k-bit Address Bus
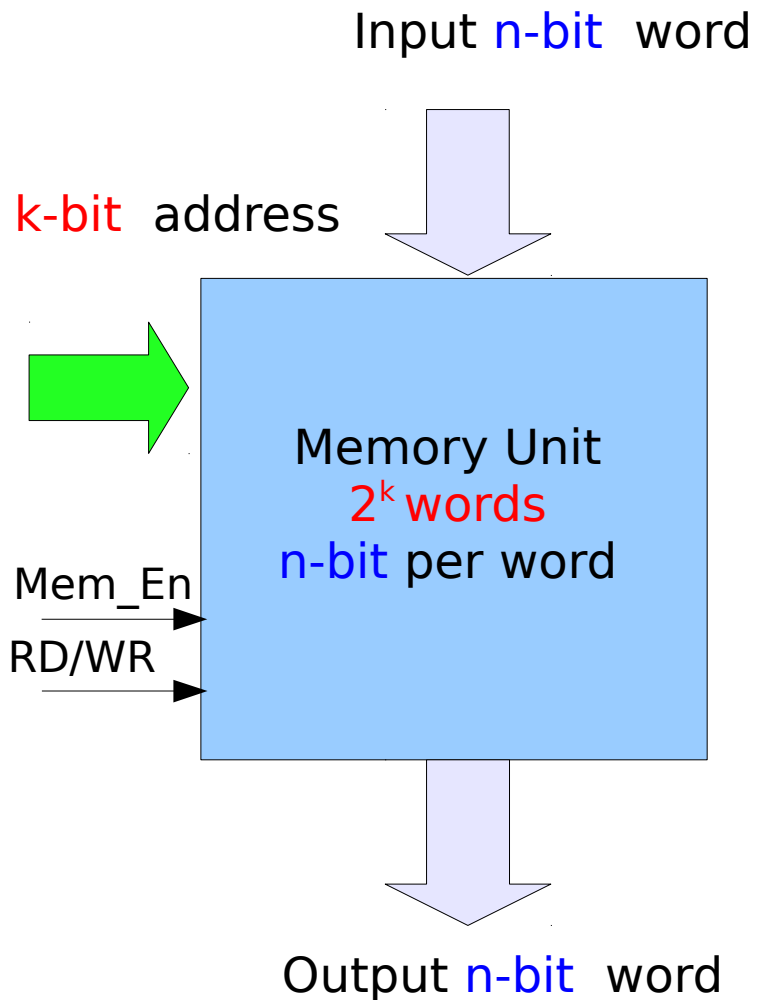
Memory-mapped IO Operations

For normal memory address

For I/O device address

Peri-Device

Memory

CPU

WR

Data Bus

Address Bus

Peri-Device

Memory

CPU

RD

Data Bus

Address Bus
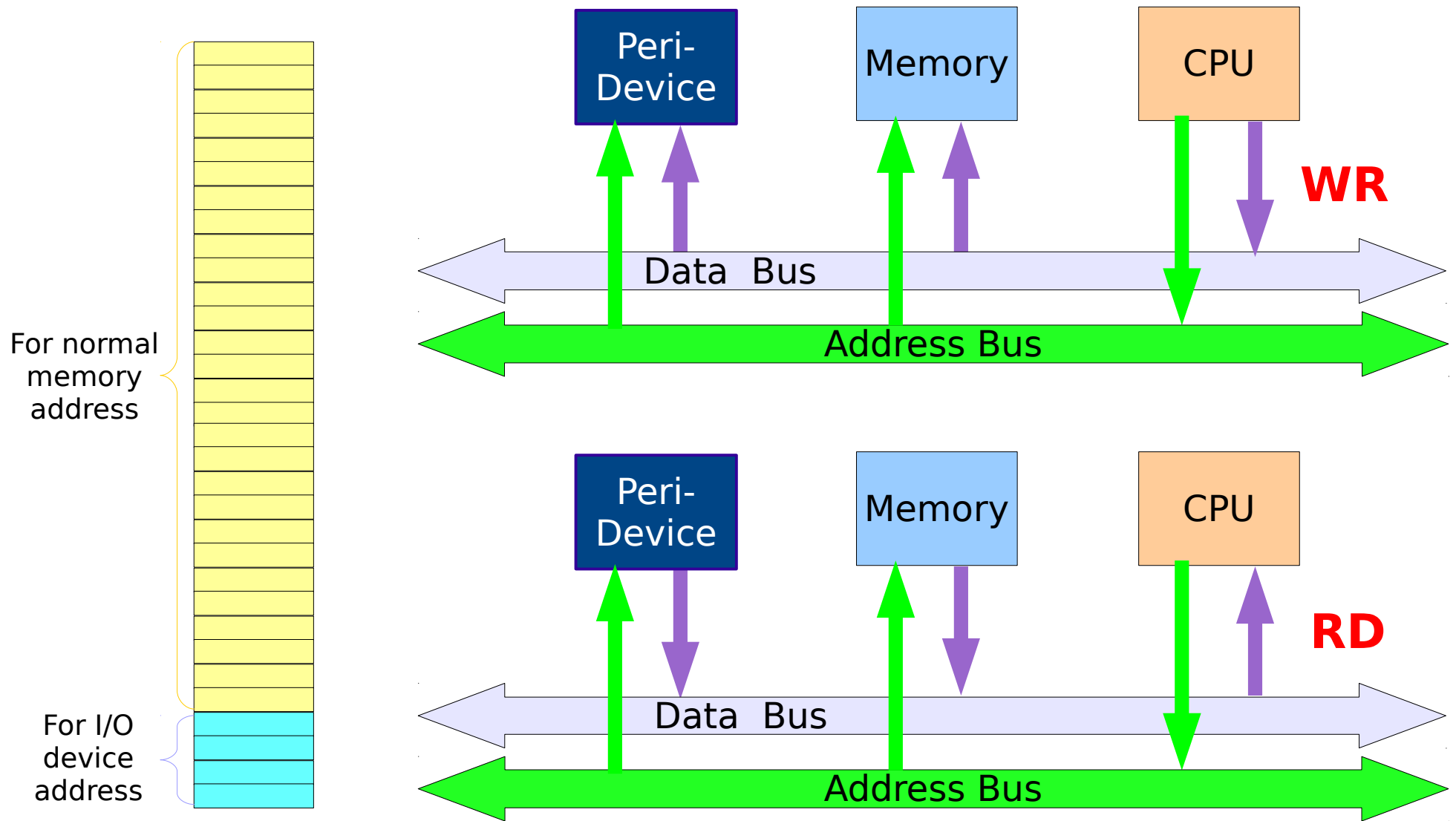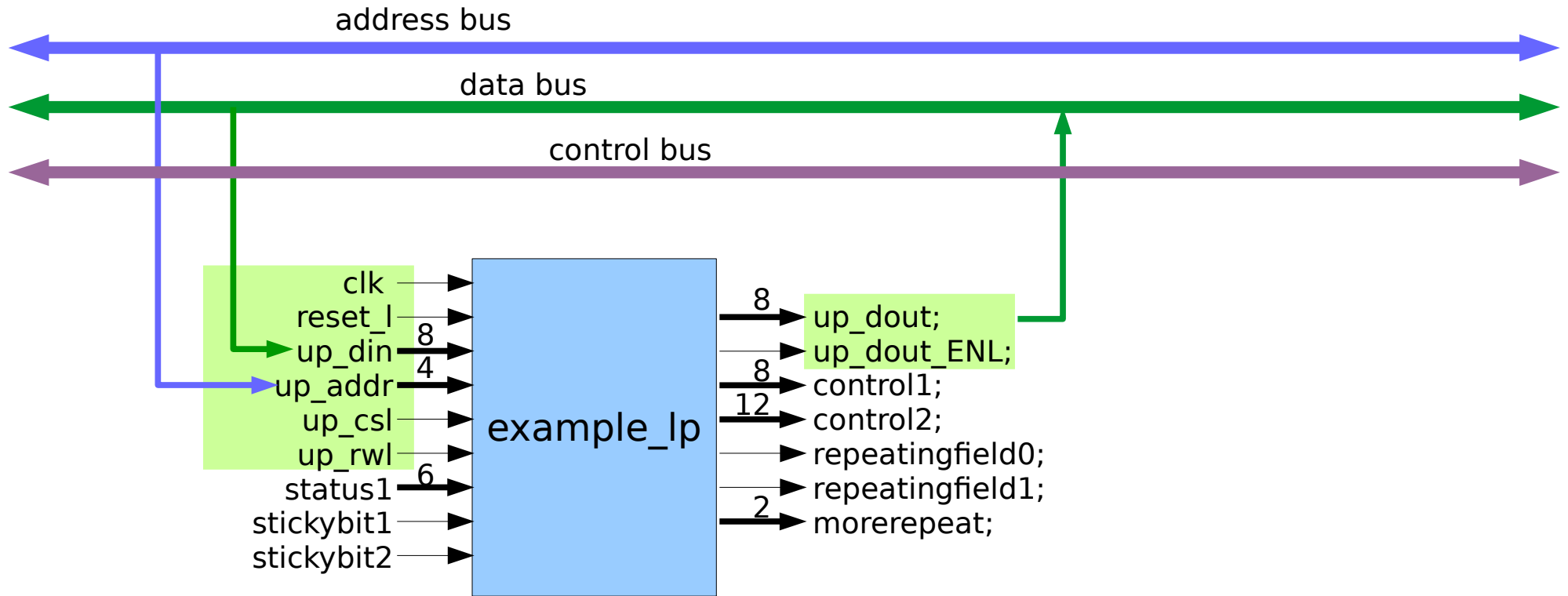
System Bus Interface

Module Interface

address bus

data bus

clk
reset_l
up_din — 8
up_addr — 4
up_csl
up_rwl
status1 — 6
stickybit1
stickybit2

example_lp

8 → up_dout;
→ up_dout_ENL;
8 → control1;
12 → control2;
→ repeatingfield0;
→ repeatingfield1;
2 → morerepeat;

addr rdata wdata

Peripheral Device

Processor

Module Interface

System BUS I/F

example_lp

clk
reset_l
up_din — 8
up_addr — 4
up_csl
up_rwl
status1 — 6
stickybit1
stickybit2

up_dout — 8
up_dout_ENL
control1 — 8
control2 — 12
repeatingfield0
repeatingfield1
morerepeat — 2

Status info from the peri-device

Control signal to the peri-device

References

[1] http://en.wikipedia.org/
[2] https://en.wikiversity.org/wiki/The_necessities_in_SOC_Design
[3] https://en.wikiversity.org/wiki/The_necessities_in_Digital_Design
[4] https://en.wikiversity.org/wiki/The_necessities_in_Computer_Design
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[8] Digital Systems, Hill, Peterson, 1987