GPIO

Please send corrections (or suggestions) to youngwlim@hotmail.com.
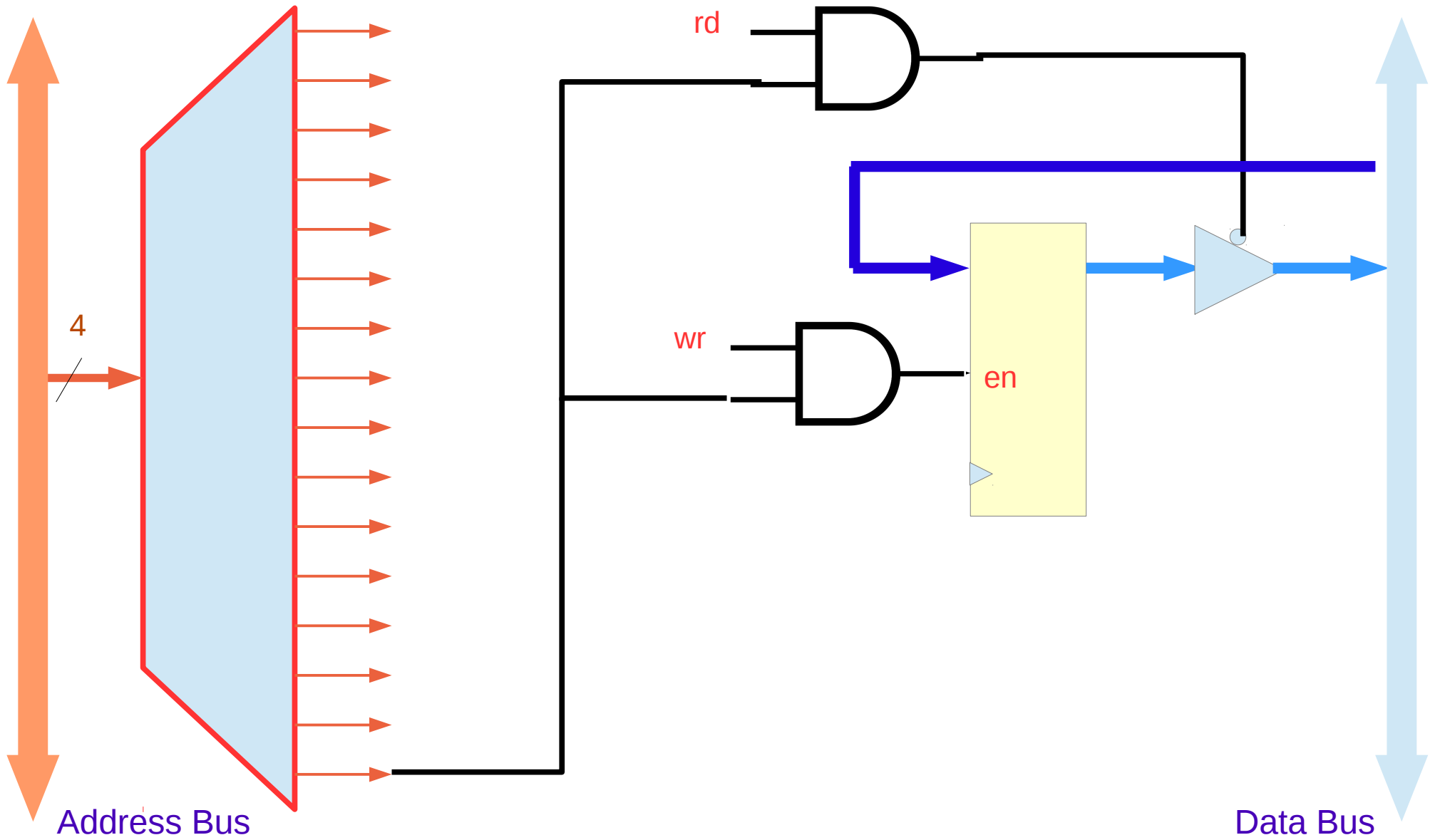
This document was produced by using OpenOffice and Octave.

IO Registers
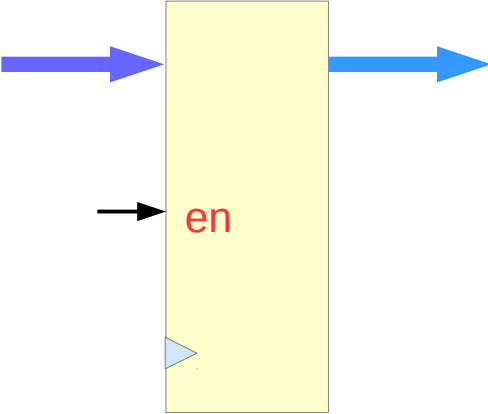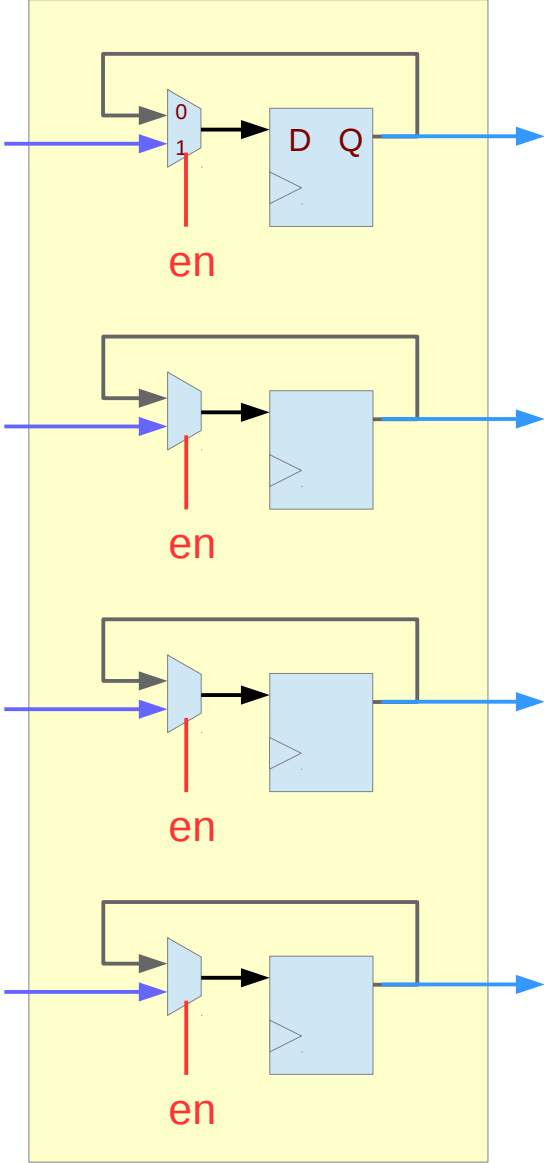
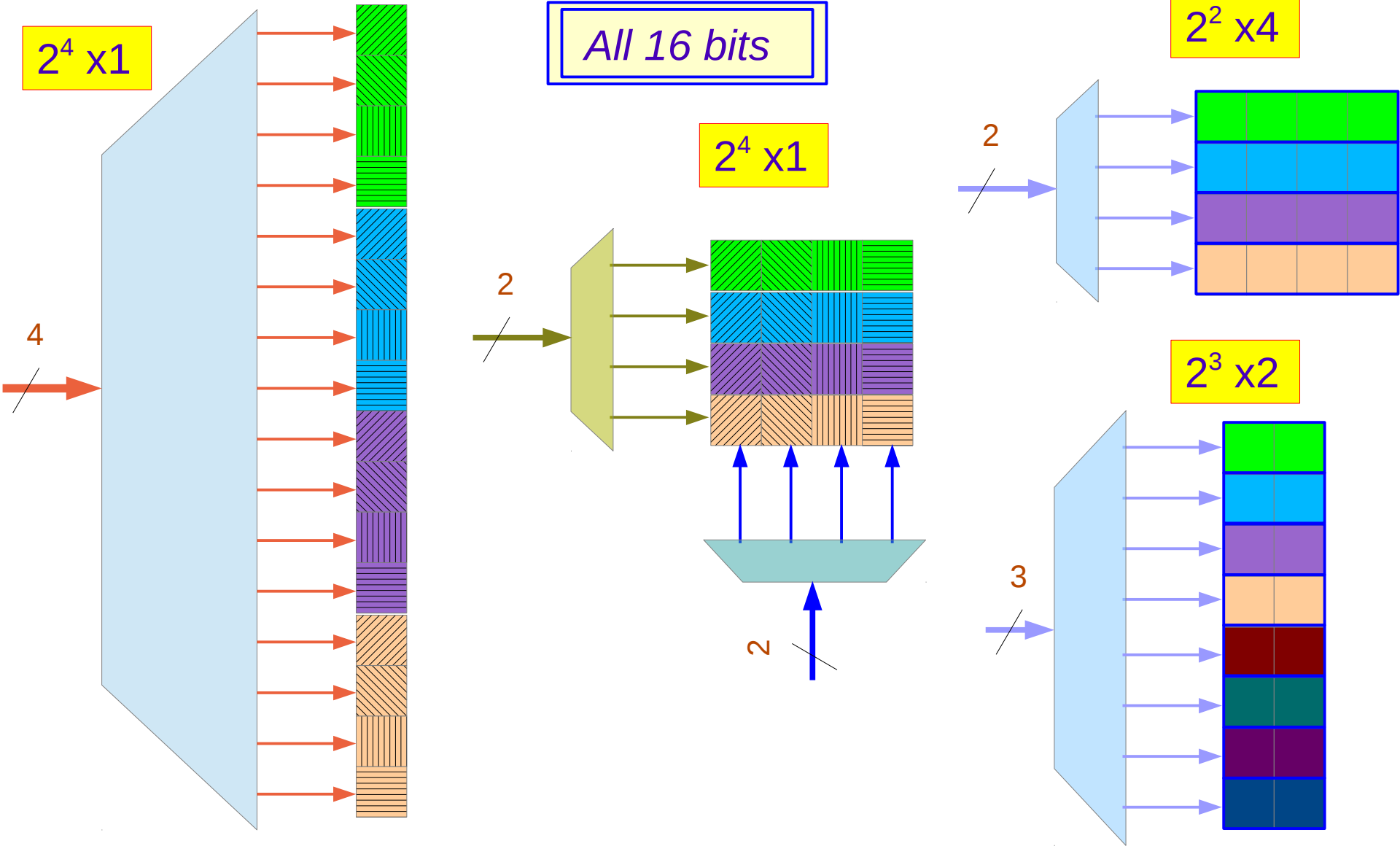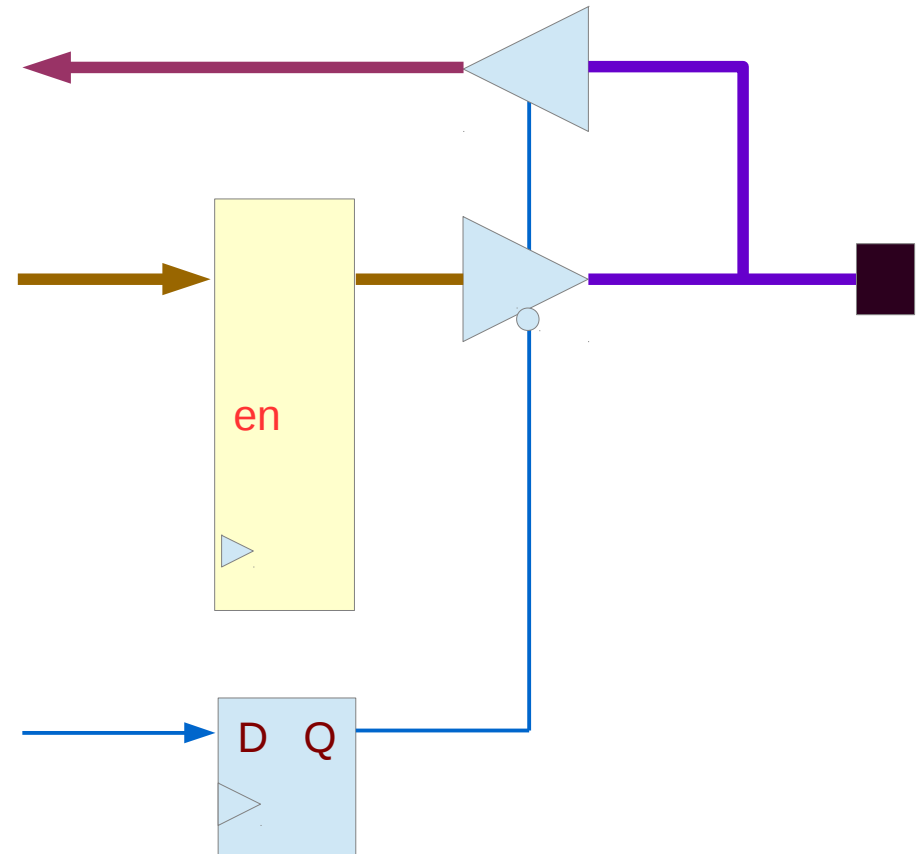# Address Decoding & IO Register

rd

wr

en

4

Address Bus

Data Bus

Young Won Lim
11/8/14

Address Decoding & DRAM

$2^4 \times 1$

All 16 bits

$2^4 \times 1$

$2^2 \times 4$

$2^3 \times 2$

4

2

2

2

3

GPIO

- read from port address

- write to port address

en

- write to port direction register

D   Q

References

[1] http://en.wikipedia.org/
[2] D.M. Harris, S. L. Harris, "Digital Design and Computer Architecture"