DRAM (2A)

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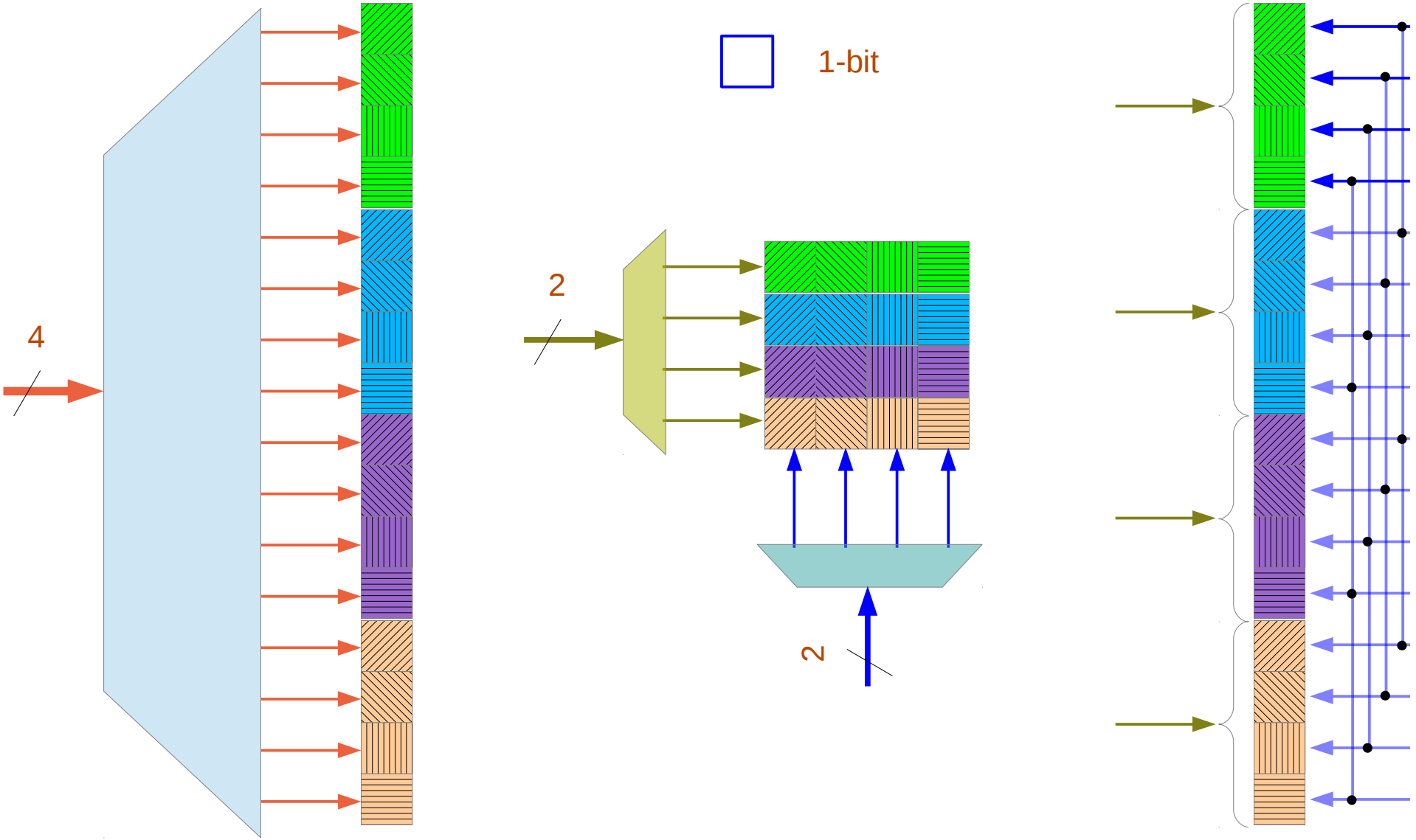
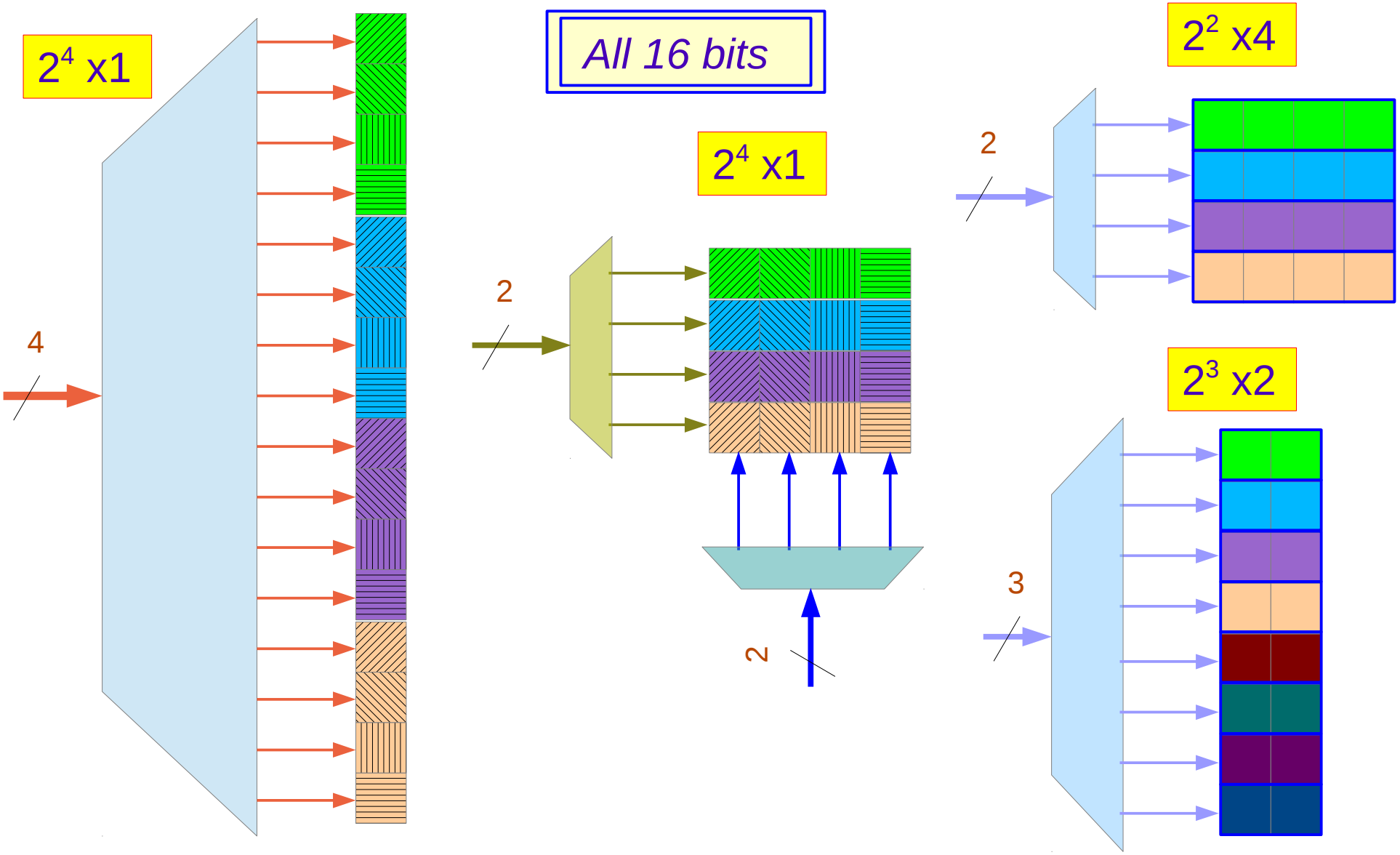
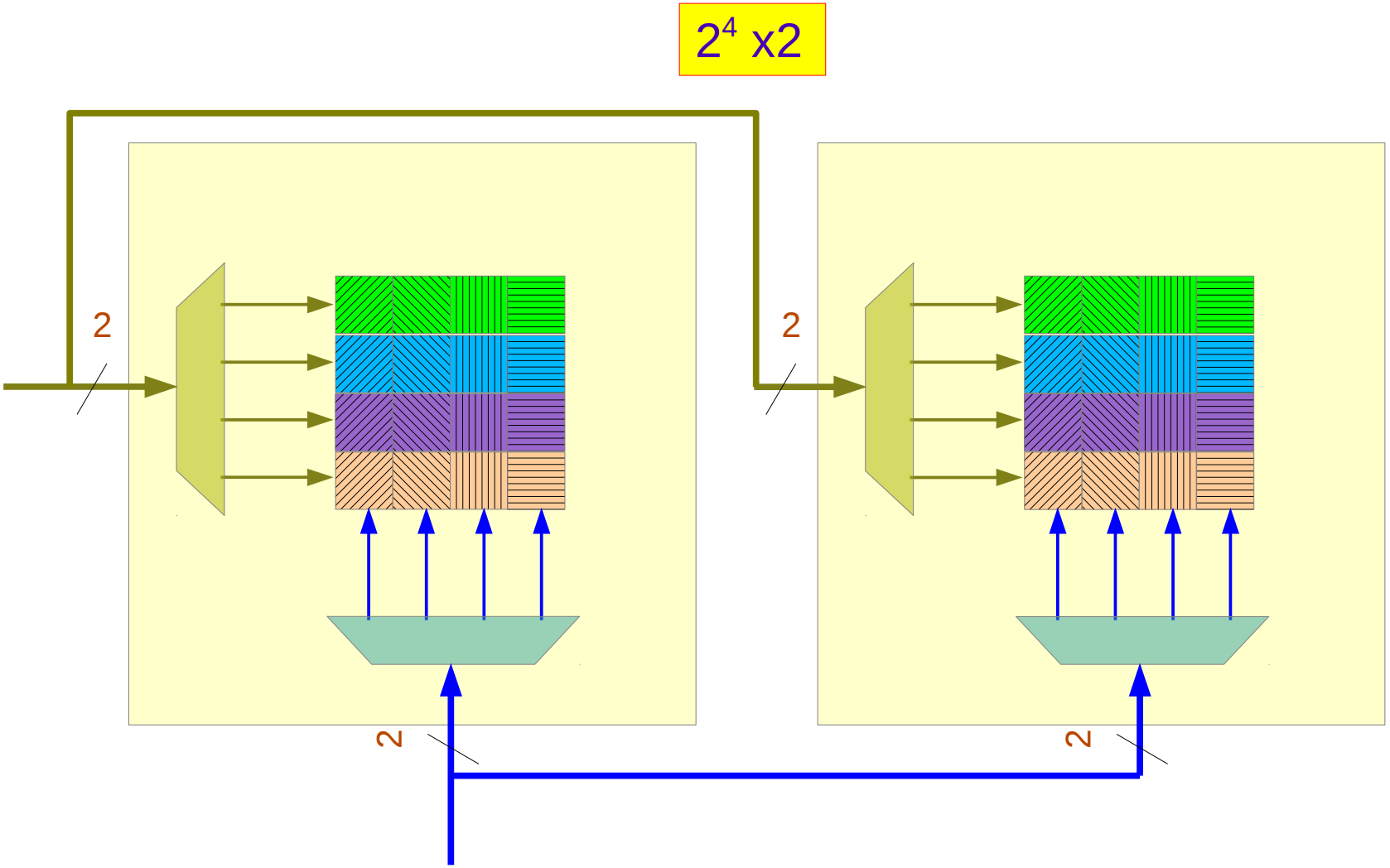
DRAM – Coincidence Selection (1)



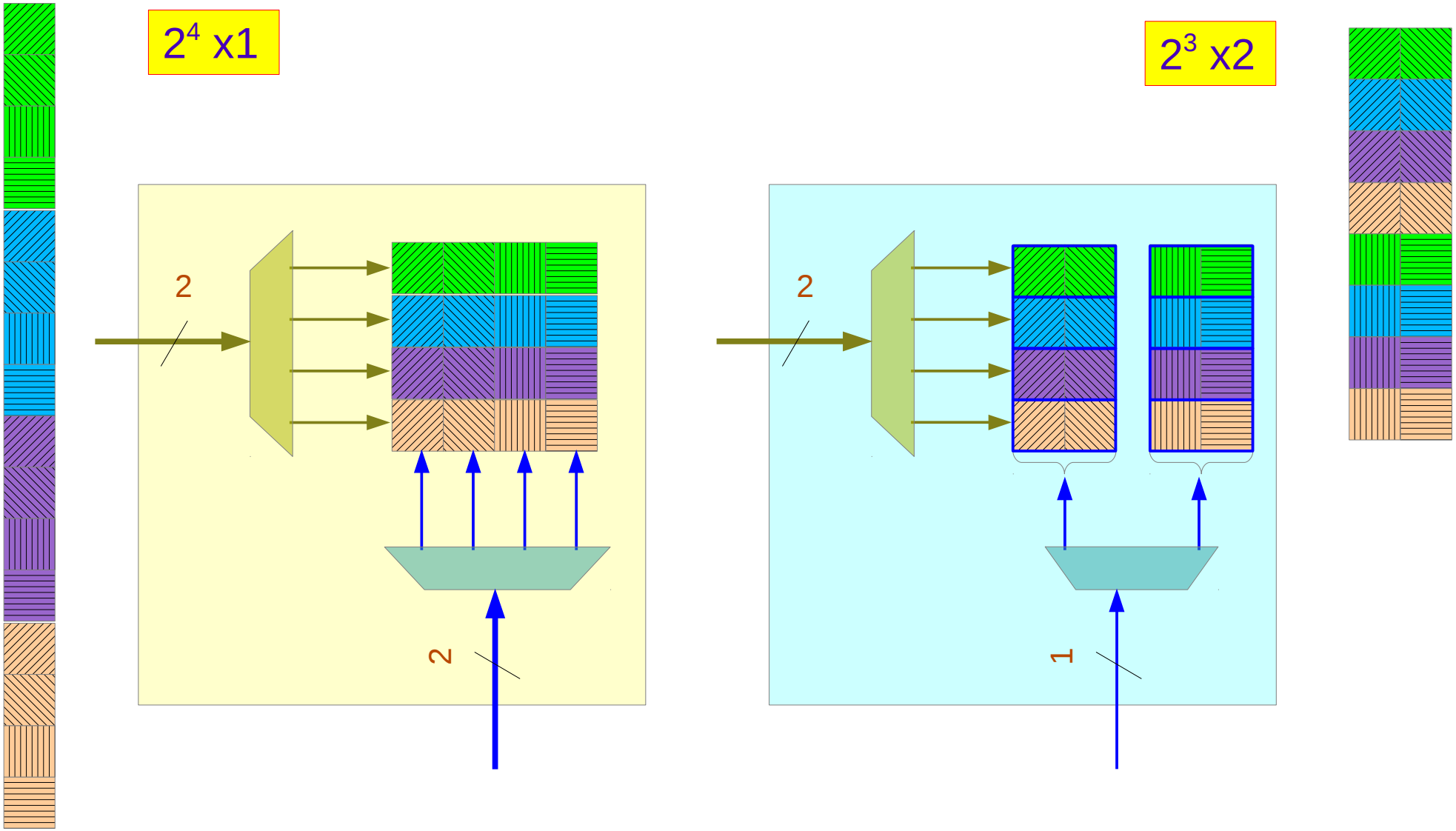
DRAM – Coincidence Selection (2)



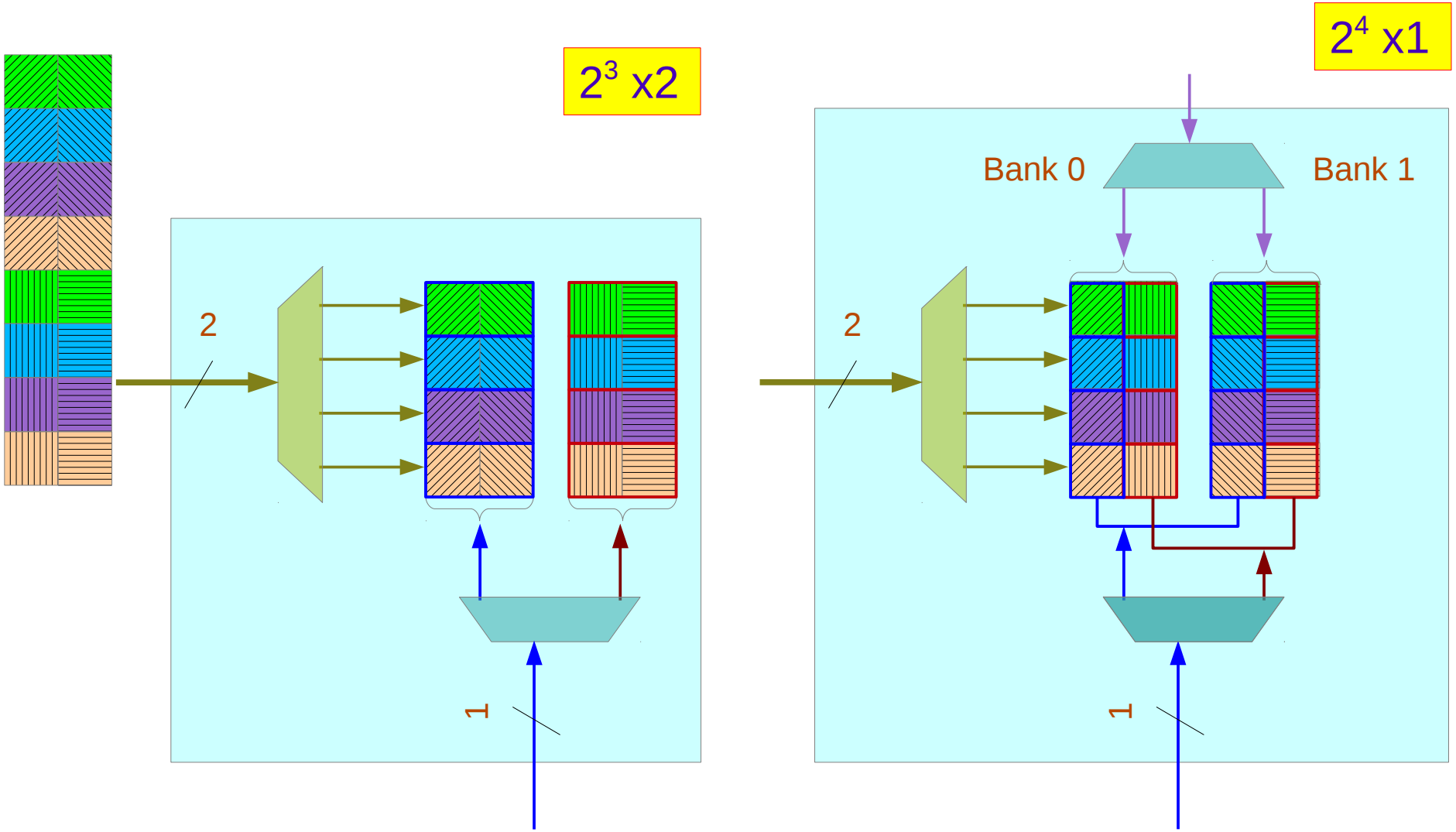
DRAM – Coincidence Selection (3)



DRAM – Coincidence Selection (4)



DRAM – Coincidence Selection (5)



DRAM – PreCharge

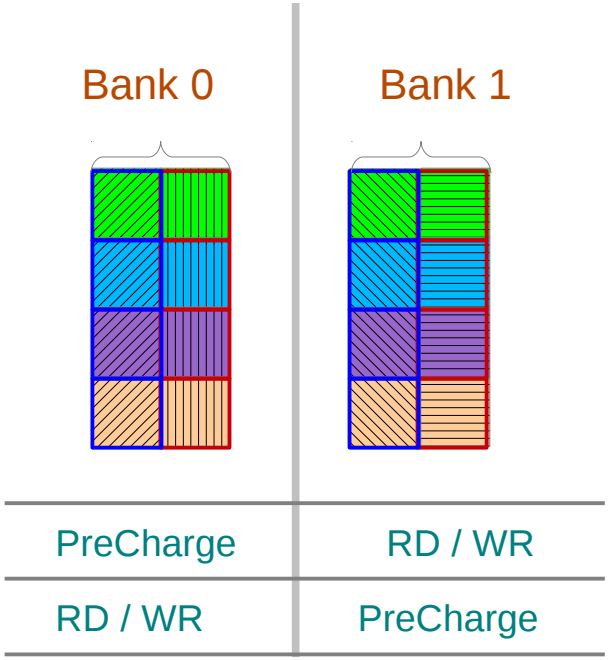
DDR RAM executes commands given by the chipset.
(Activate, Read, Write, Precharge, etc)

To activate a bank with a row for reading or writing,
the bank is to be charged.

This amplifies the signal from that row for a read

A memory bank is usually precharged
without waiting for a read/write request and then charging.

Precharging one memory bank can usually be overlapped
with **accessing** another memory bank.

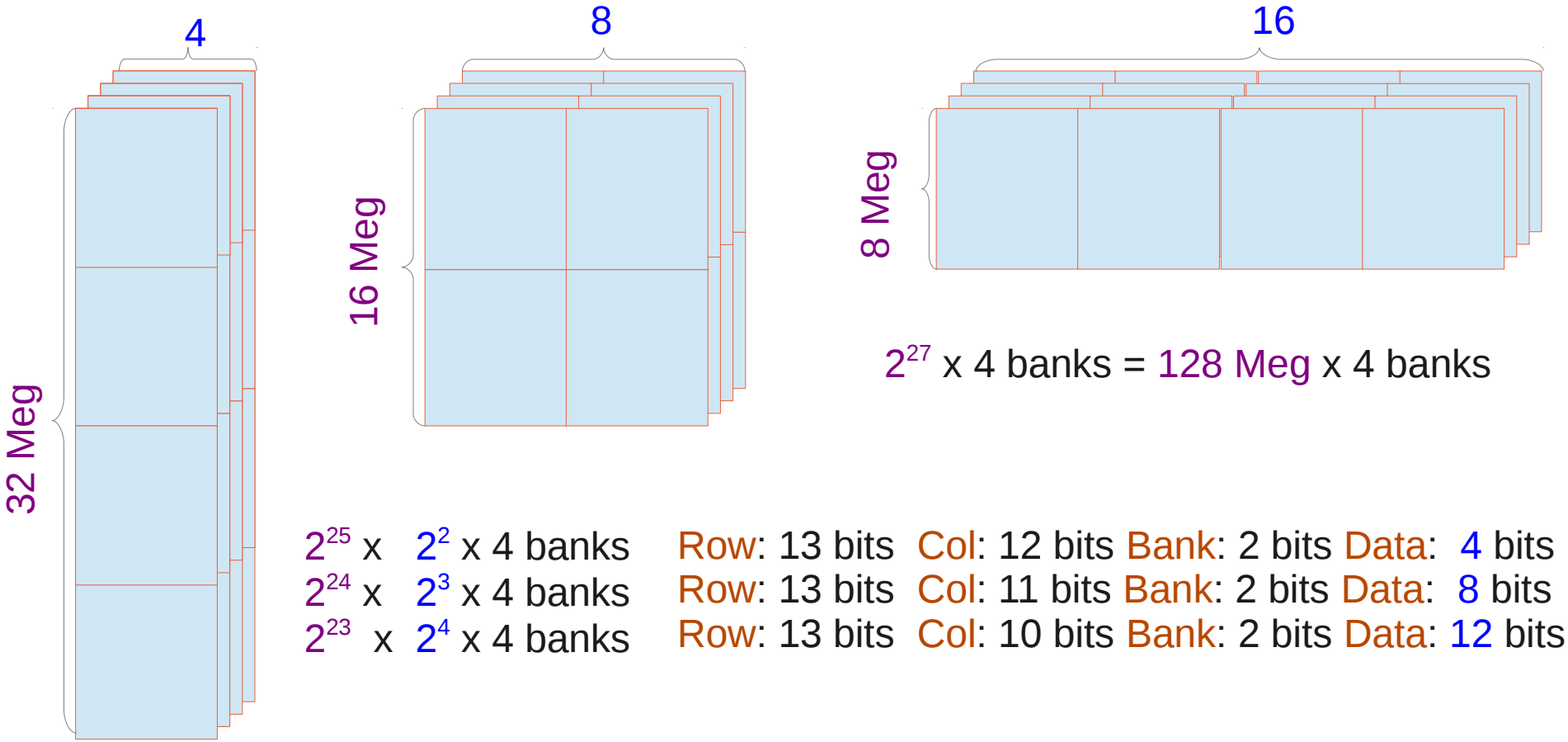


DRAM – 512Mb Example

MT46V128M4 – 32 Meg x 4 x 4 banks
MT46V64M8 – 16 Meg x 8 x 4 banks
MT46V32M16 – 8 Meg x 16 x 4 banks

2^{25} x 2^{2} x 4 banks
2^{24} x 2^{3} x 4 banks
2^{23} x 2^{4} x 4 banks

All 512 Mbits



2^{27} x 4 banks = 128 Meg x 4 banks

2^{25} x 2^{2} x 4 banks
2^{24} x 2^{3} x 4 banks
2^{23} x 2^{4} x 4 banks

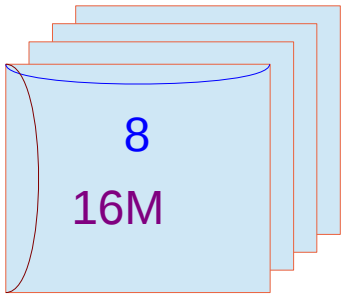
Row: 13 bits Col: 12 bits Bank: 2 bits Data: 4 bits
Row: 13 bits Col: 11 bits Bank: 2 bits Data: 8 bits
Row: 13 bits Col: 10 bits Bank: 2 bits Data: 12 bits

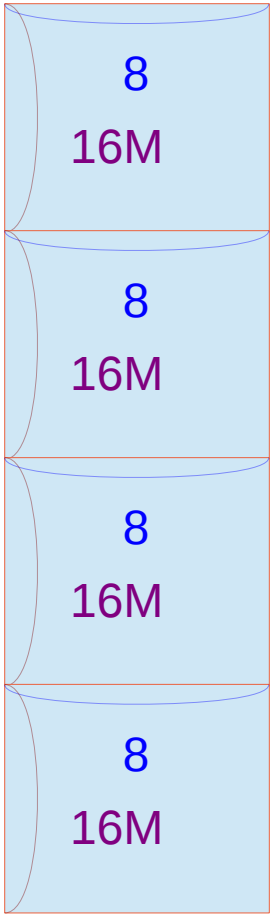
DIMM Example (1)

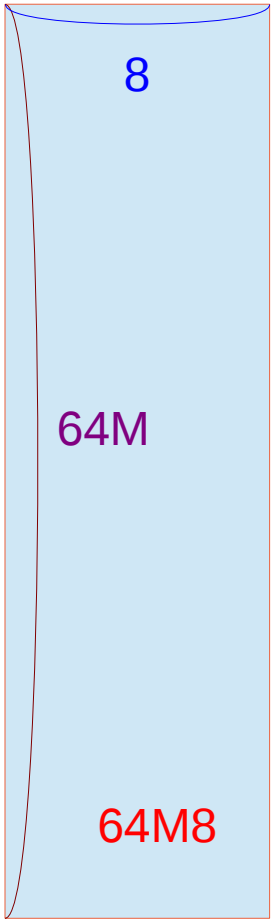
MT46V64M8 – 16 Meg x 8 x 4 banks 2^{24} x 2^{3} x 4 banks

All 512 Mbits

Row: 13 bits Col: 11 bits Bank: 2 bits Data: 8 bits







DIMM Example (2)

MT46V64M8 – 16 Meg x 8 x 4 banks 2^{24} x 2^{3} x 4 banks

Row: 13 bits Col: 11 bits Bank: 2 bits Data: 8 bits

All 512 Mbits

128M x 8 Bytes = $\mathbf{2^{27}}$ **x** $\mathbf{2^{3}}$ Bytes = 1 GBytes

References

[1] http://en.wikipedia.org/
[2] M. M. Mano, C. R. Kime, “Logic and Computer Design Fundamentals”, 4th ed.
[3] http://www.ccs.neu.edu/course/com3200/parent/NOTES/DDR.html “DDR RAM by Gene Cooperman”