

Types of Flip-flops (1A)

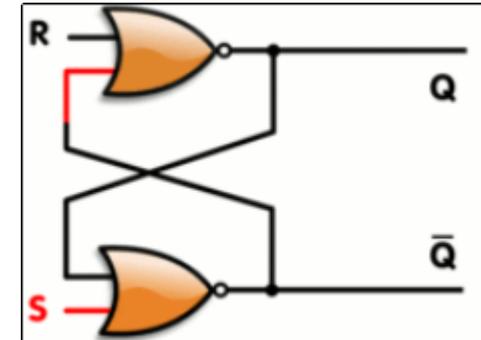
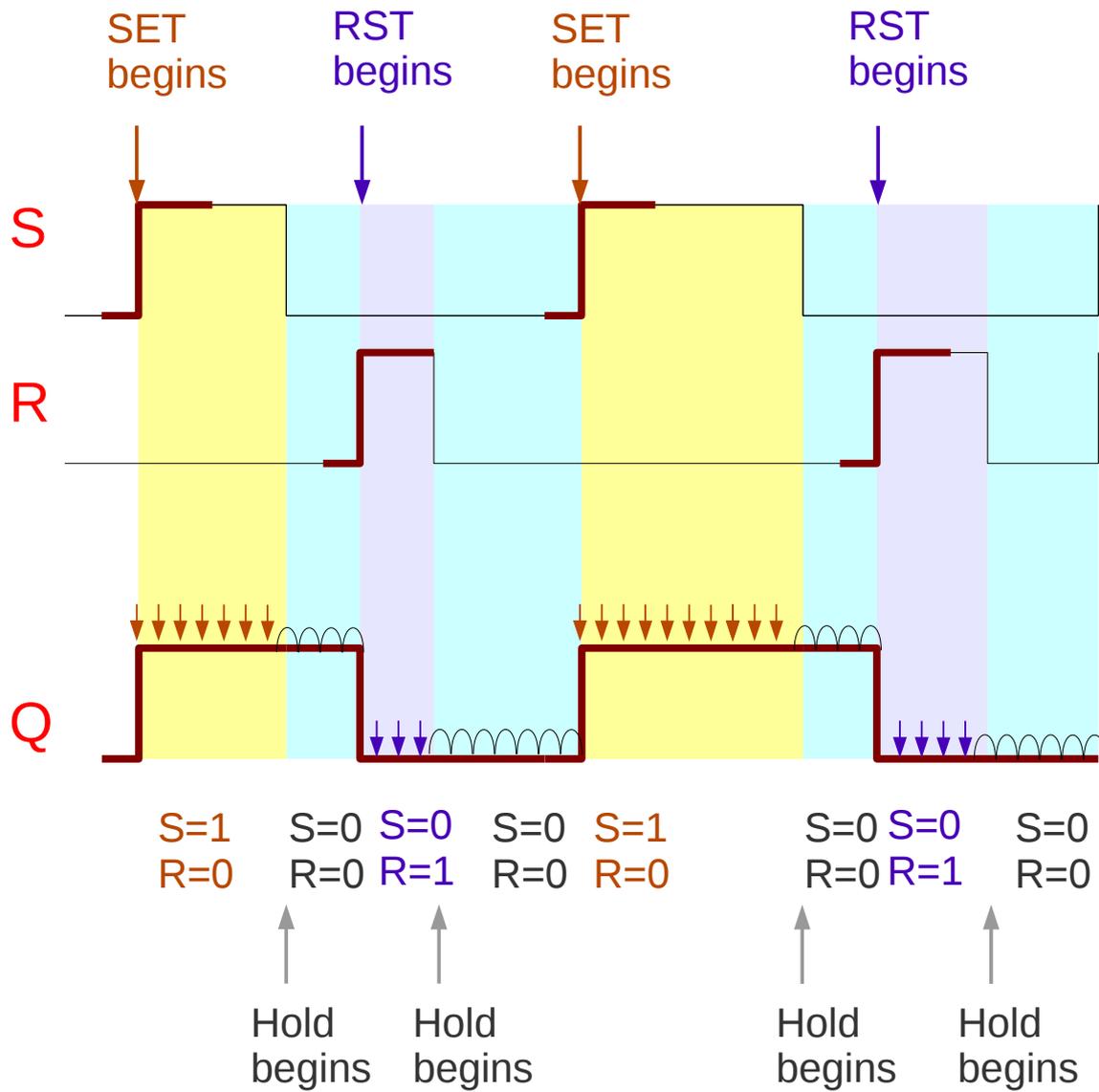
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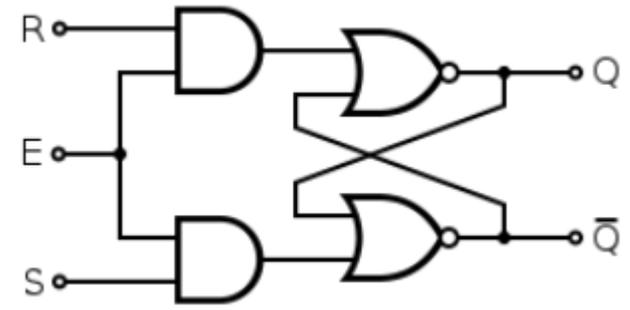
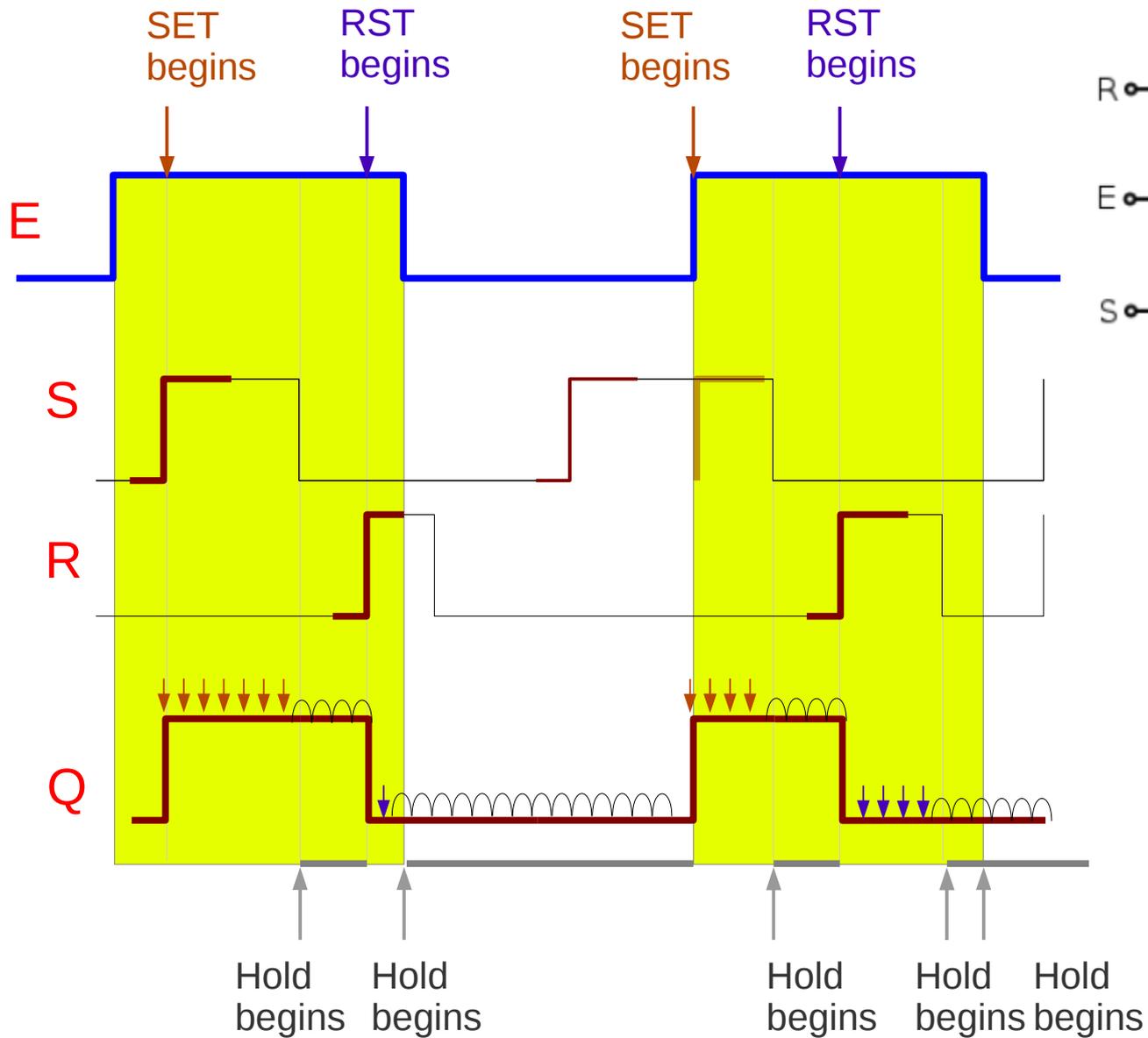
Please send corrections (or suggestions) to youngwlim@hotmail.com.

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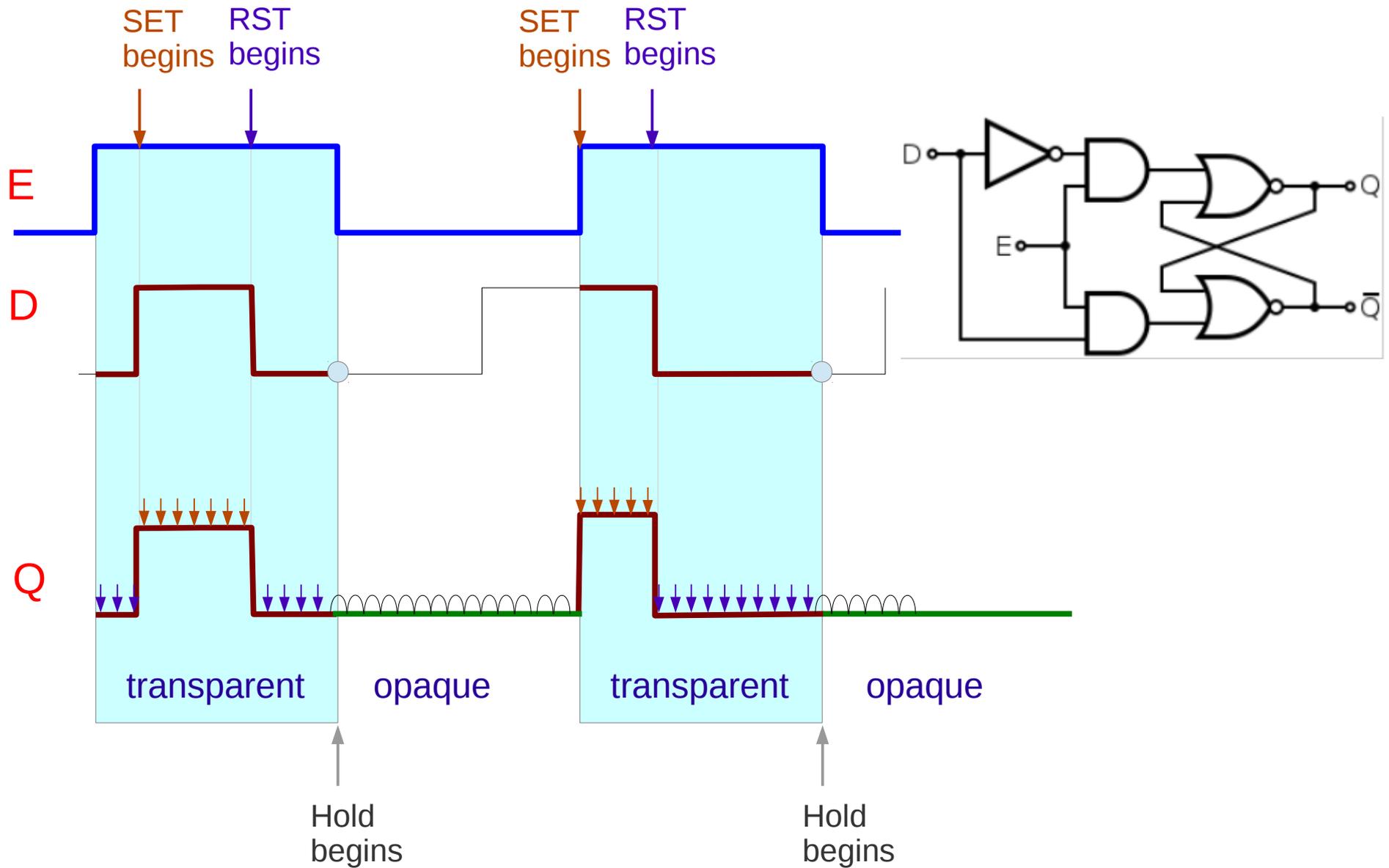
NOR-based RS Latch



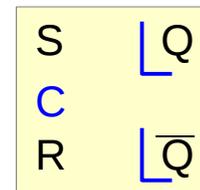
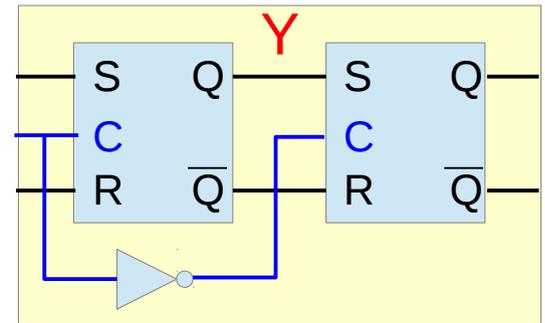
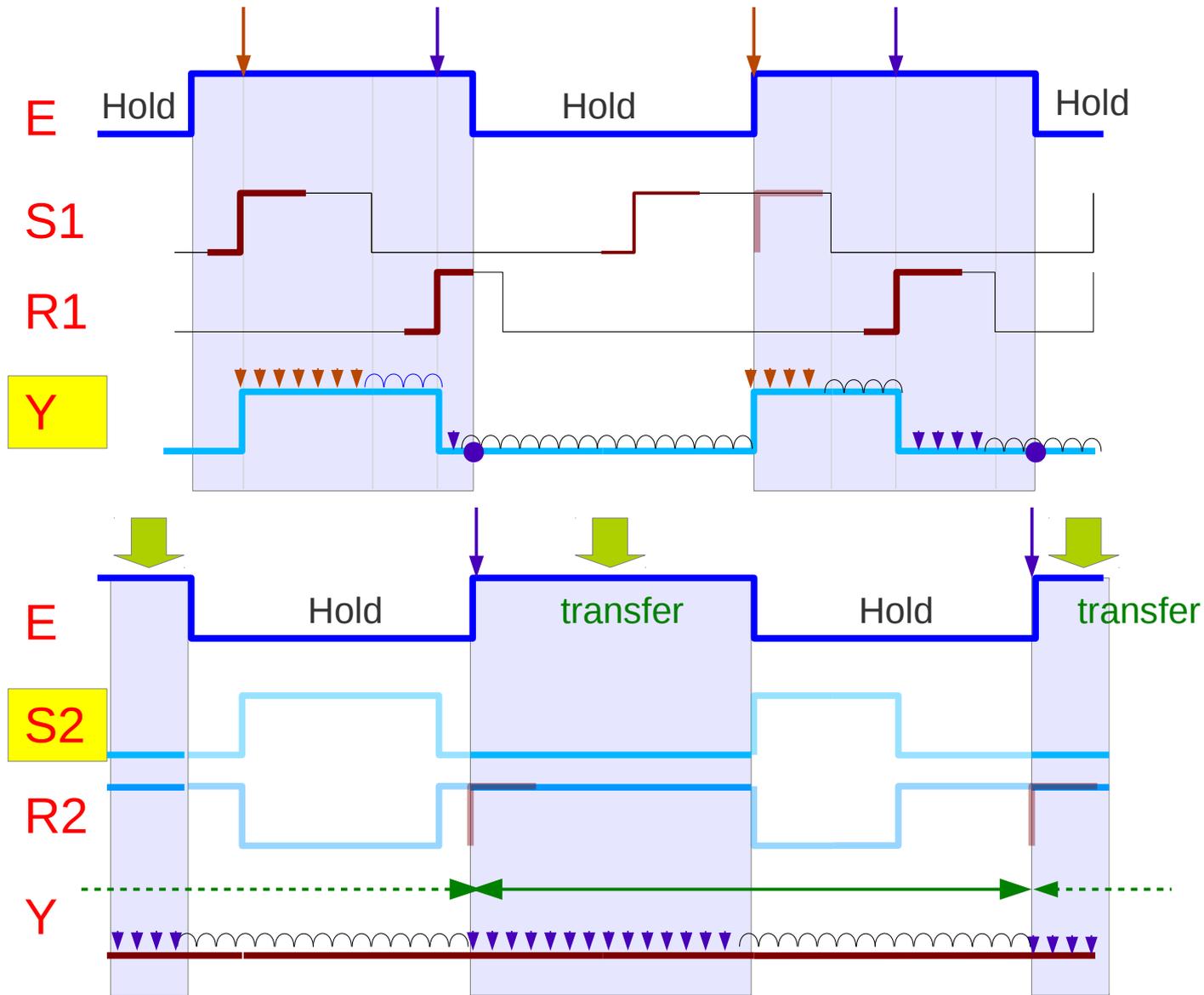
Gated RS Latch



Gated D Latch



Master Slave SR FlipFlop

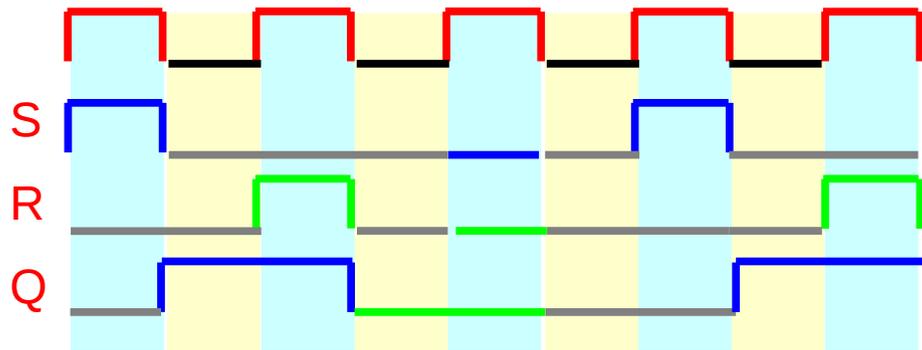


L denotes

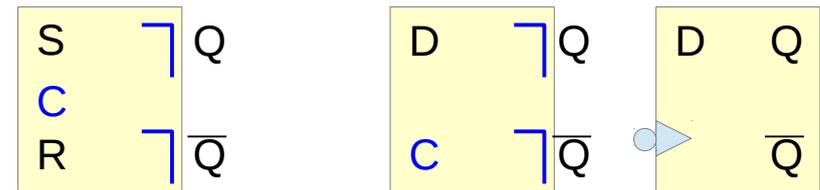
the output can change only on the negative clock edge

Types of FlipFlops

Master Slave Flip-Flops (Pulse Triggered)

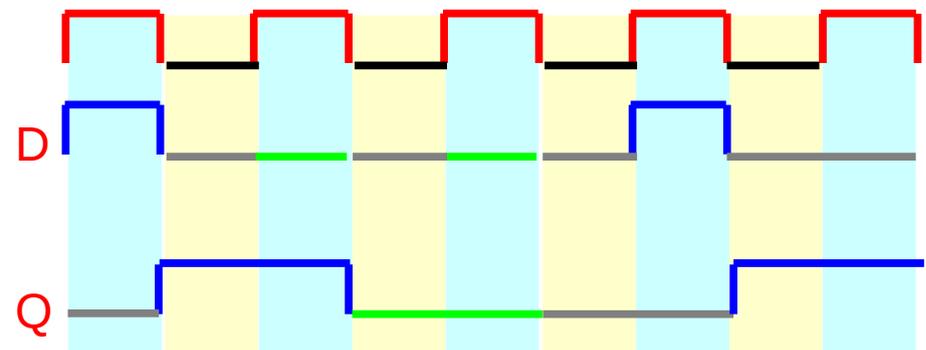
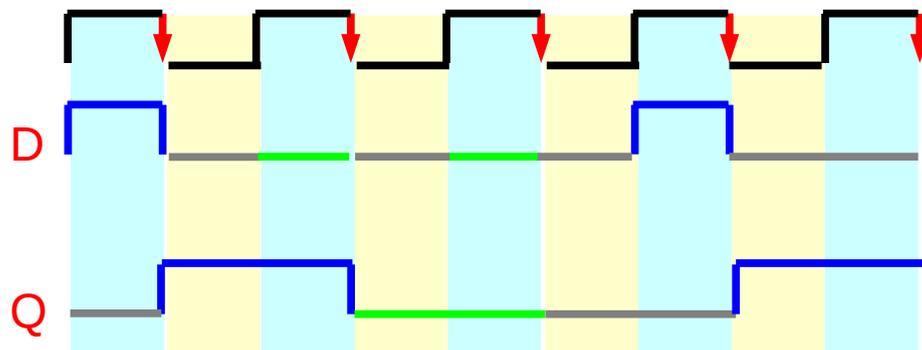


sensitive to any change of the input during $C=1$
the inputs must be set up before the rising edge
and must not be changed before the falling edge.



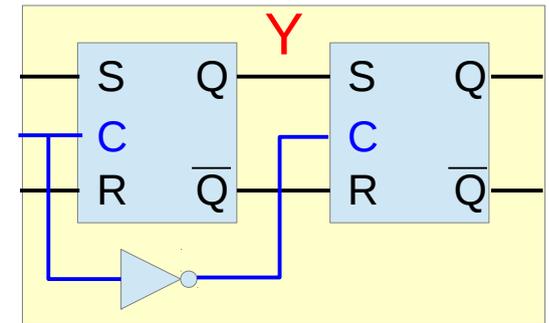
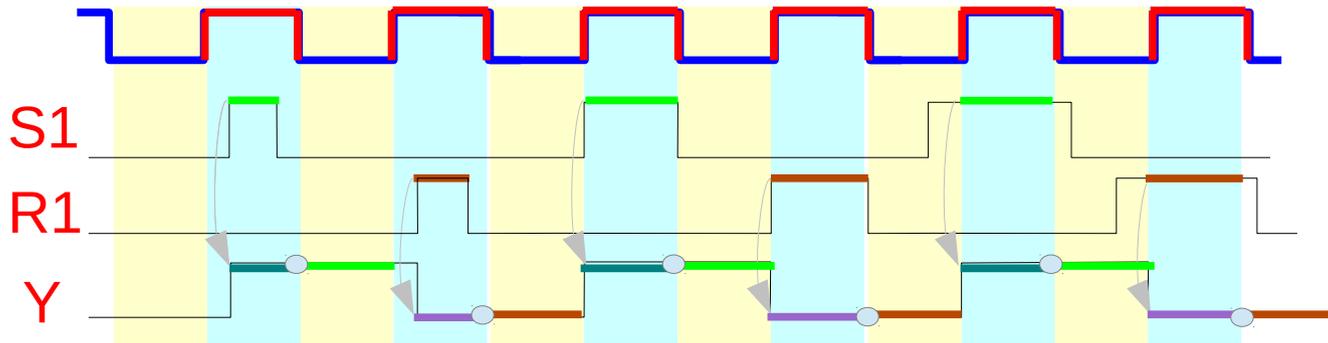
Edge Triggered Flip-Flops (Data Lock-out)

Can also view as a Master Slave Flip-Flop

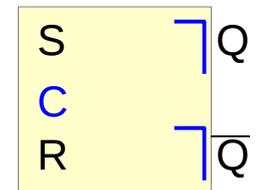
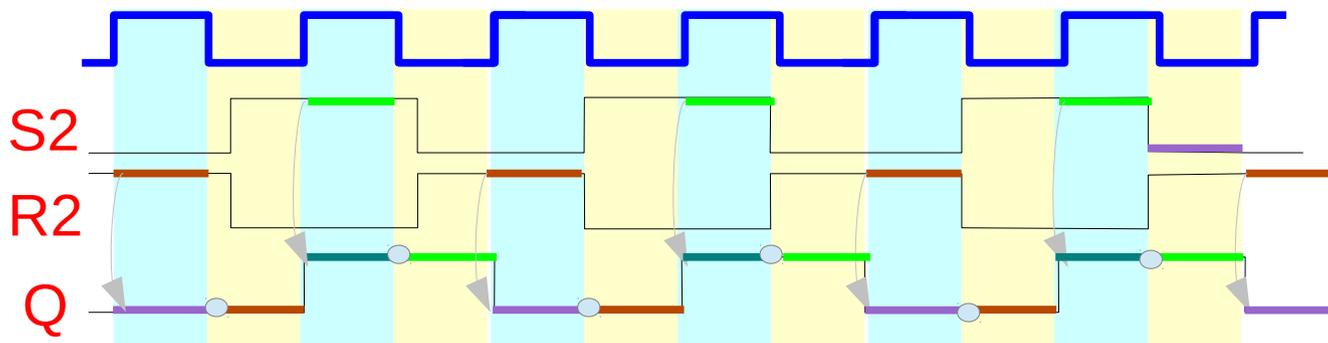


Master-Slave SR FlipFlop

Master SR Latch

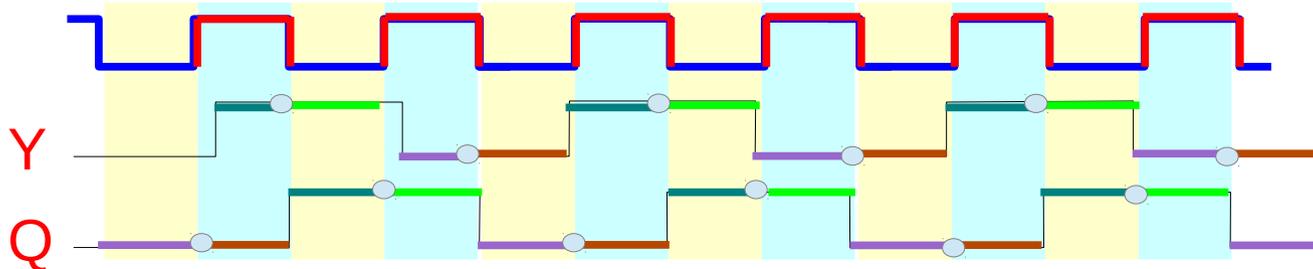


Slave SR Latch



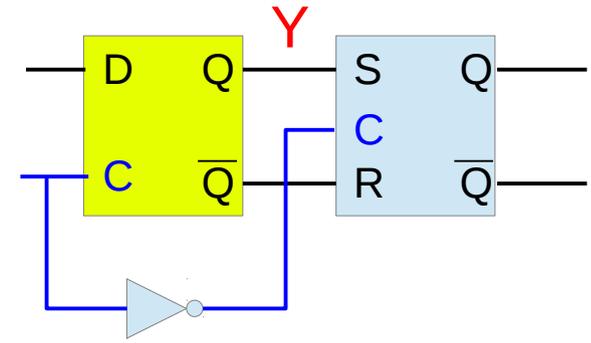
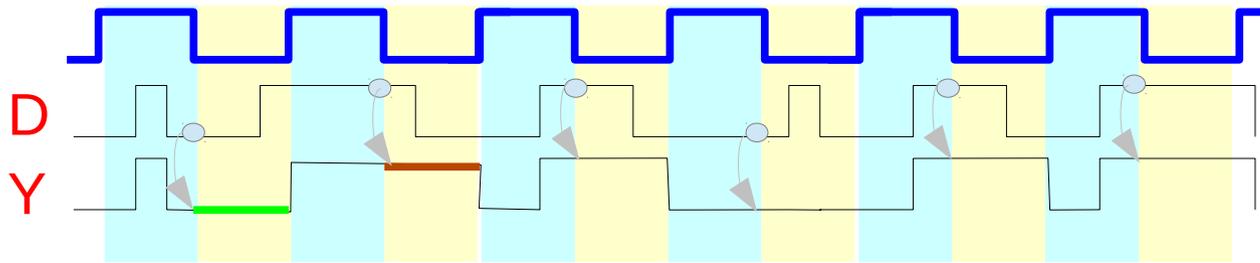
postponed output symbol

Master-Slave SR F/F

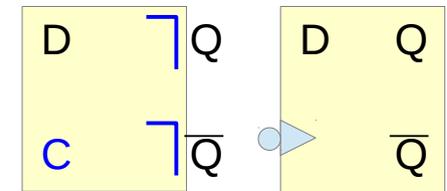
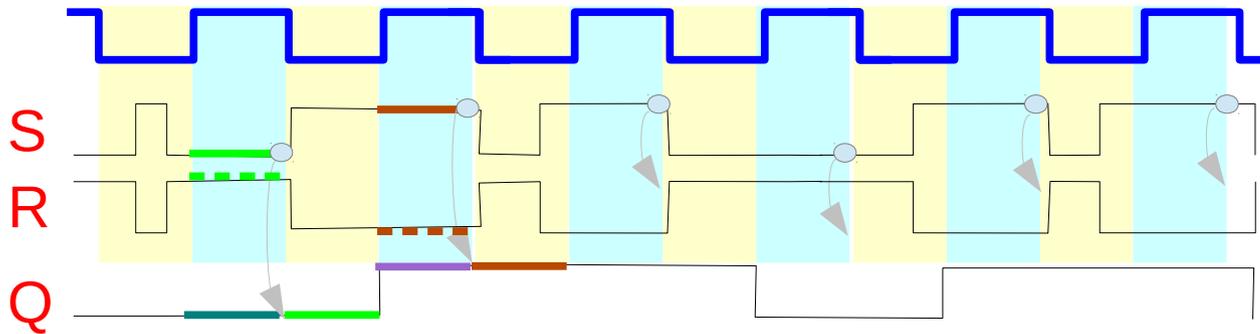


Edge Triggered D FlipFlop (1)

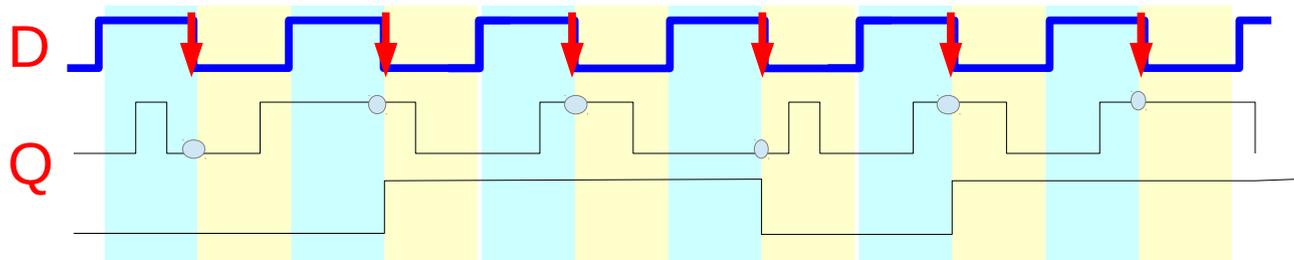
Master D Latch



Slave SR Latch

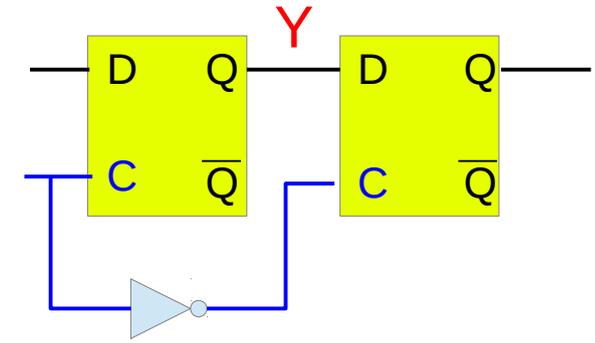
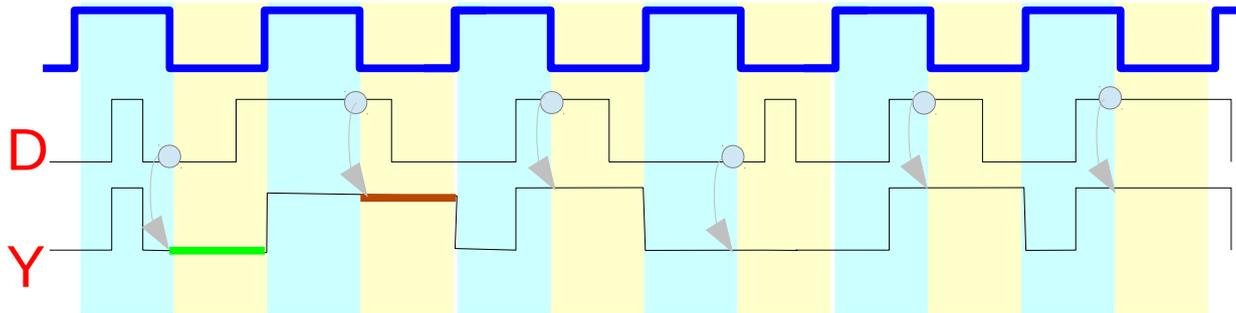


Edge Triggered D F/F

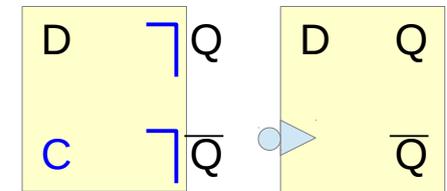
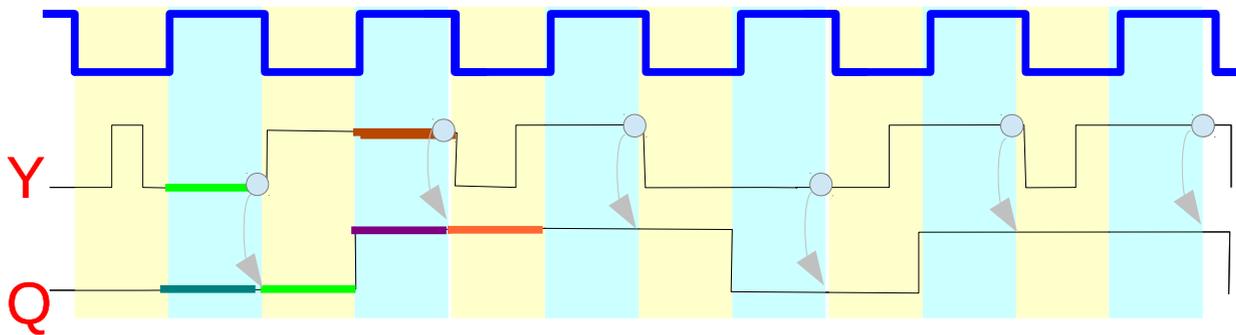


Edge Triggered D FlipFlop (2)

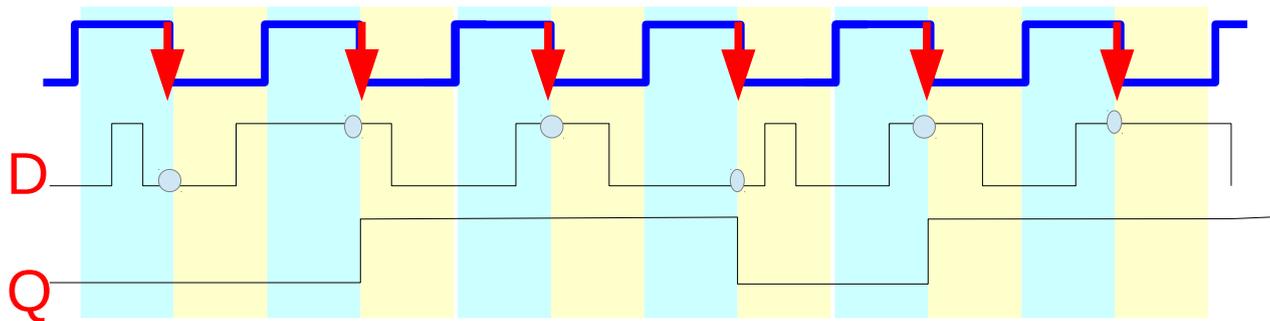
Master D Latch



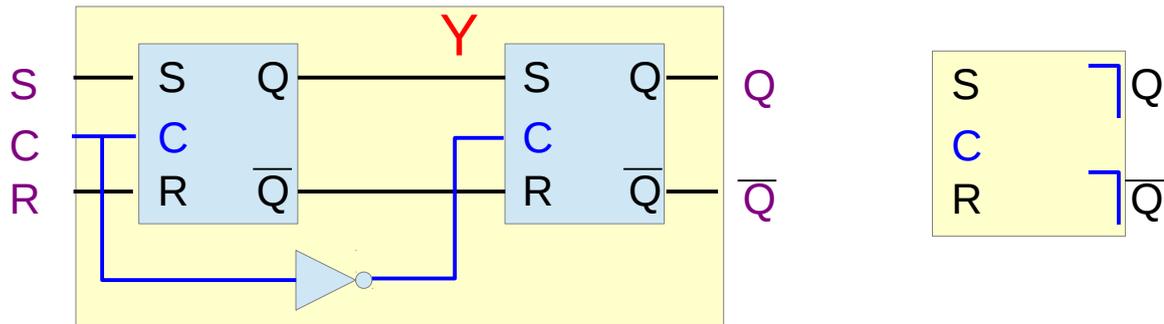
Slave D Latch



Edge Triggered D F/F



Master Slave FlipFlops (1)

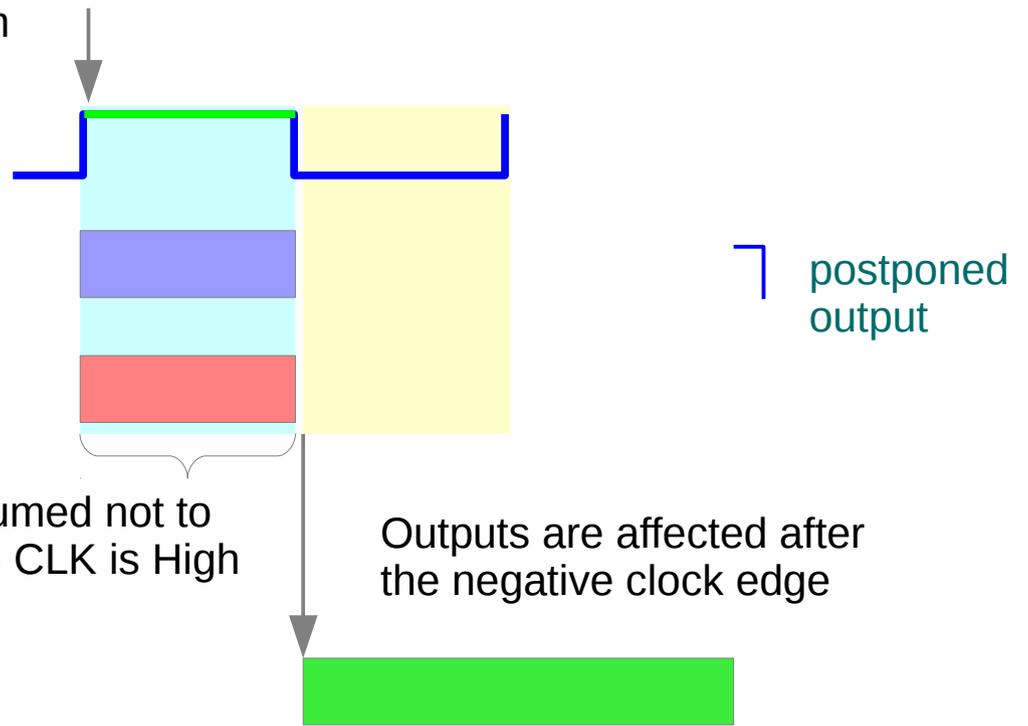


Inputs are accepted from the positive clock edge

ones catching
(glitch catching)

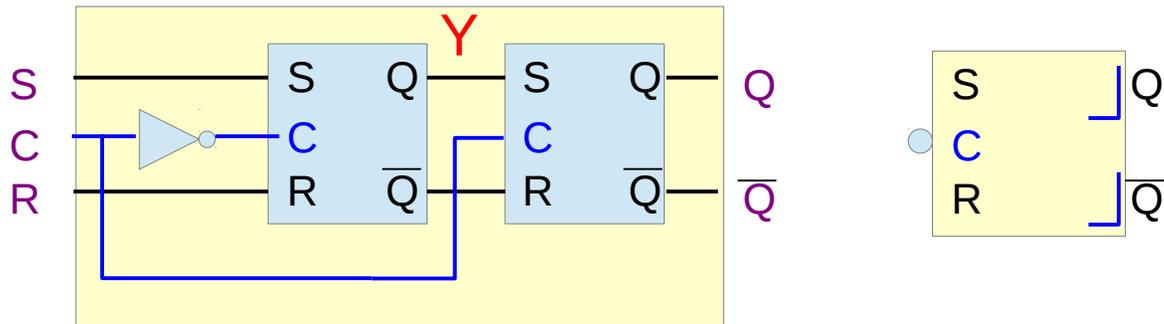


Inputs is assumed not to change when CLK is High



Outputs are affected after the negative clock edge

Master Slave FlipFlops (2)



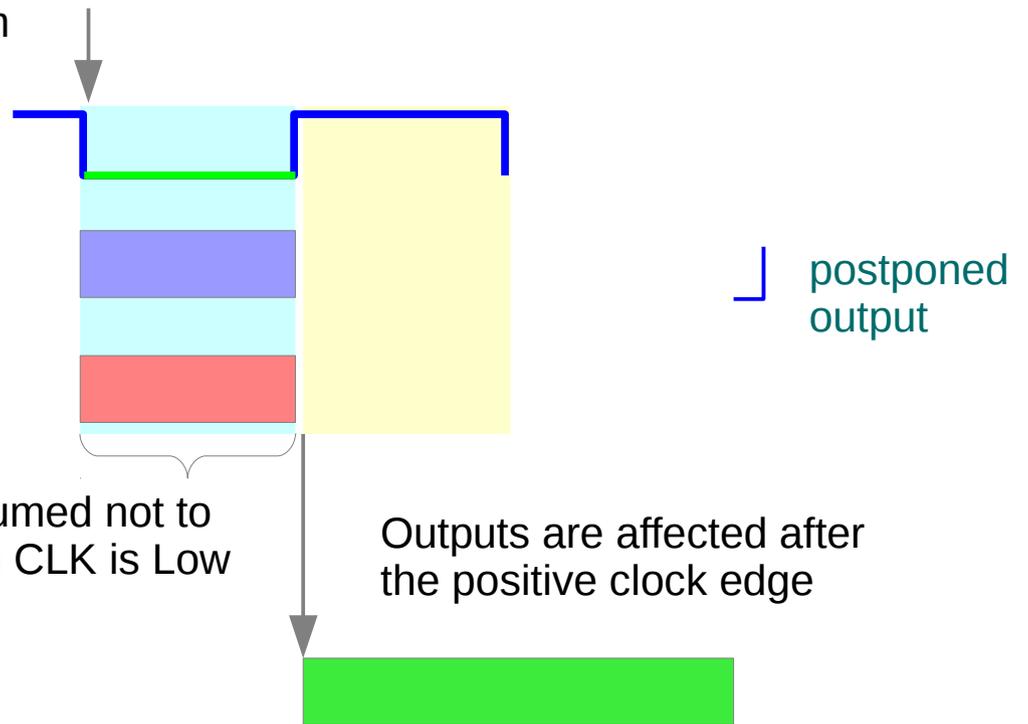
Inputs are accepted from the negative clock edge

ones catching
(glitch catching)



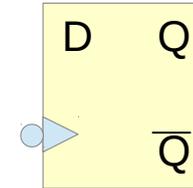
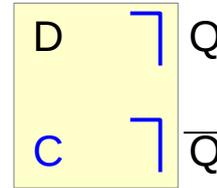
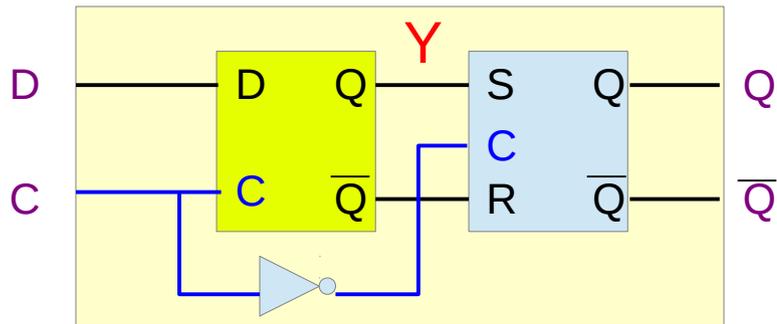
Inputs is assumed not to change when CLK is Low

Q

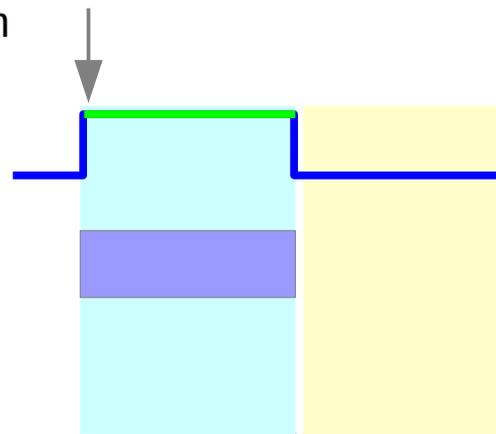


Outputs are affected after the positive clock edge

Master Slave FlipFlops (3)



Inputs are accepted from the positive clock edge



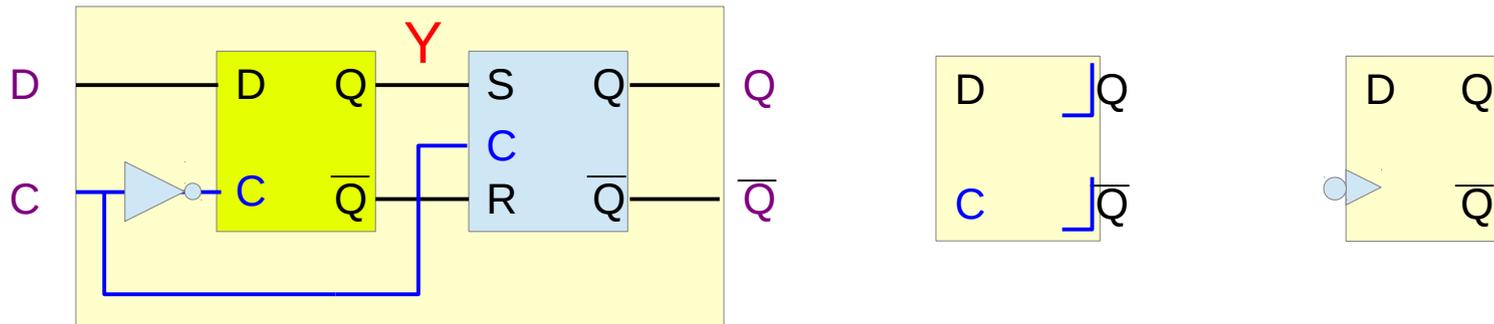
postponed output

~~ones catching
(glitch catching)~~

Inputs is assumed not to change when CLK is High

Outputs are affected after the negative clock edge

Master Slave FlipFlops (4)

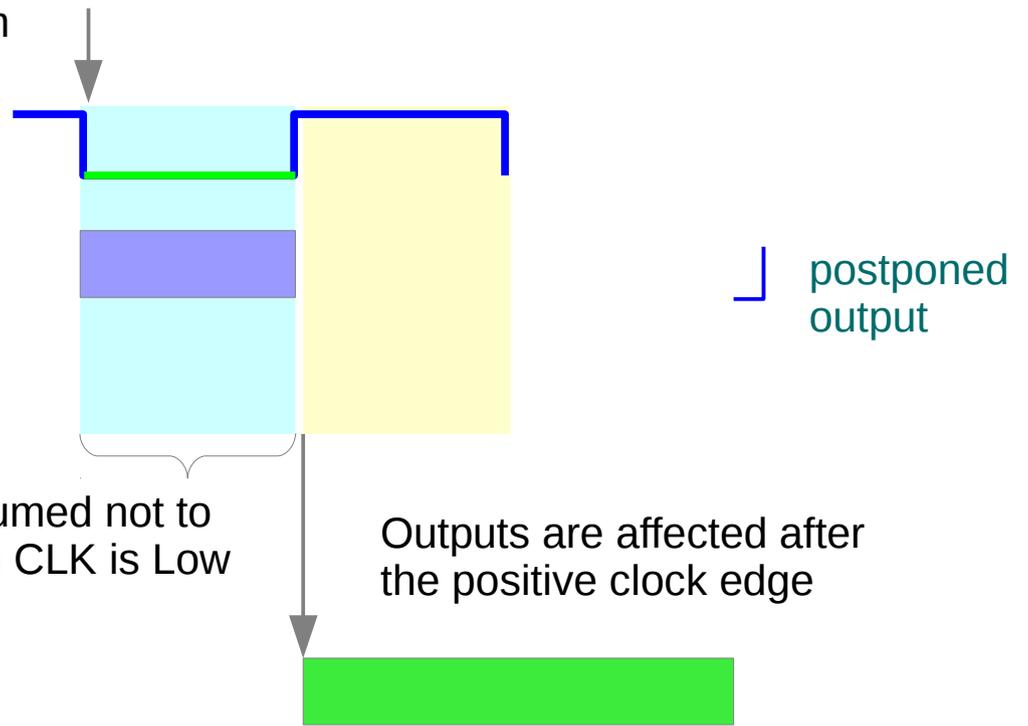


Inputs are accepted from the negative clock edge

ones catching
(glitch catching)



Inputs is assumed not to change when CLK is Low



Outputs are affected after the positive clock edge

References

- [1] <http://en.wikipedia.org/>
- [2] M. M. Mano, C. R. Kime, "Logic and Computer Design Fundamentals", 4th ed.