Synchronizer
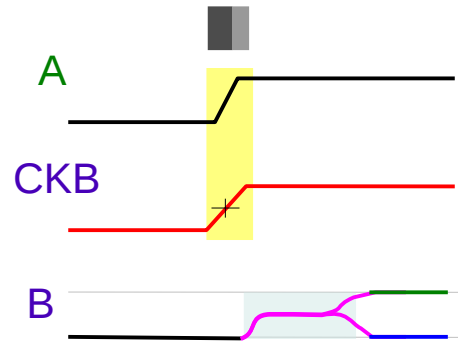
Young Won Lim
12/16/13

Please send corrections (or suggestions) to youngwlim@hotmail.com.

This document was produced by using OpenOffice and Octave.

Propagation of Metastable States

CKA

A

CKB

B

unrelated clock domain

A

CKB

B
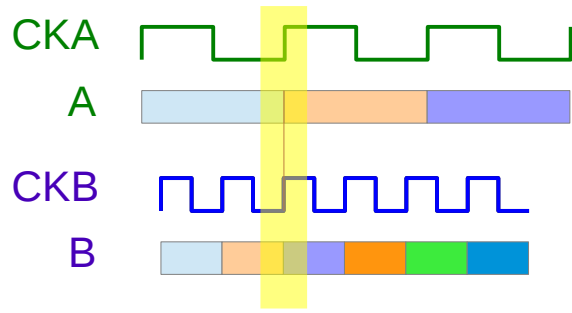
violation of setup and hold time
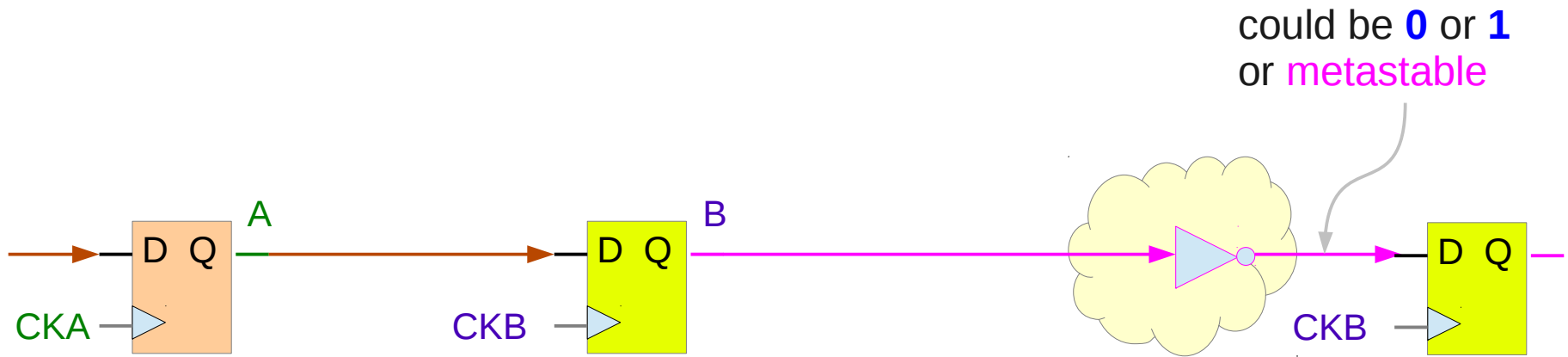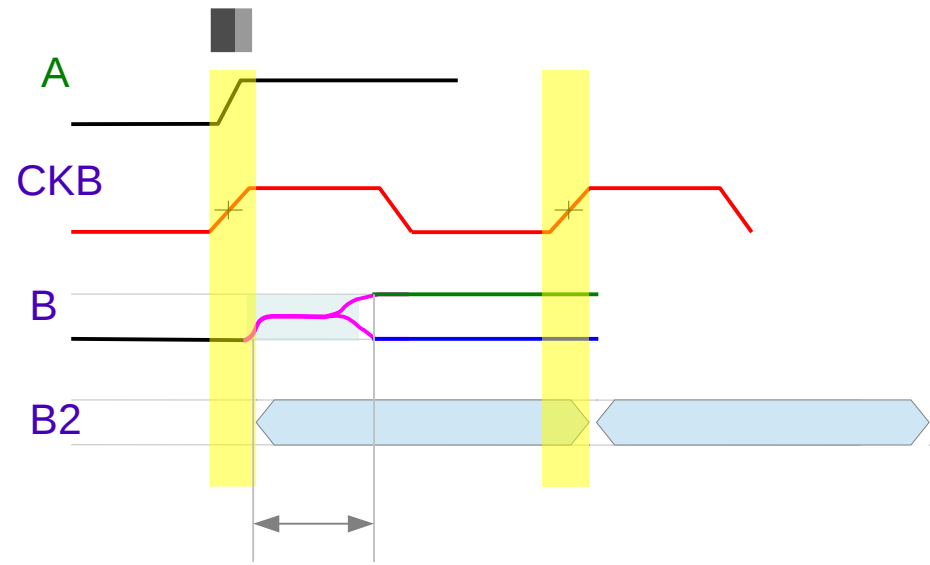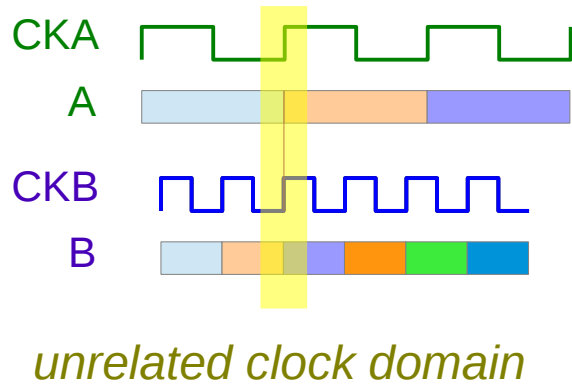
could be **0** or **1**
or metastable

A

D Q

CKA

B

D Q

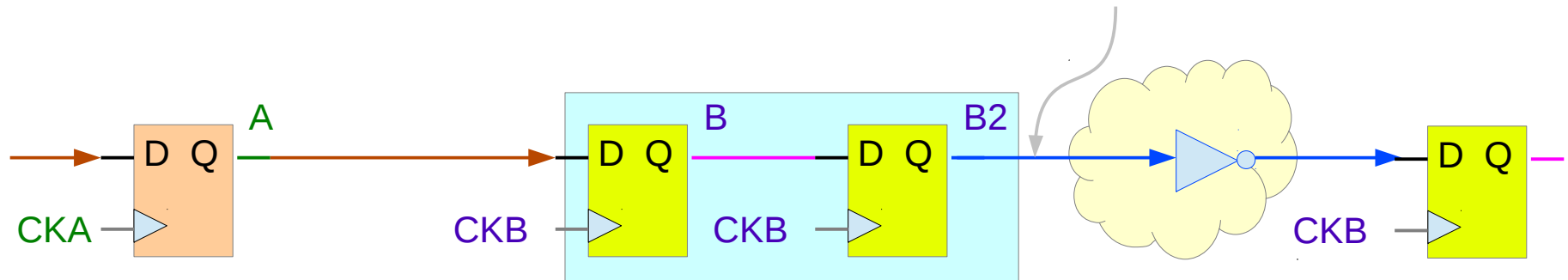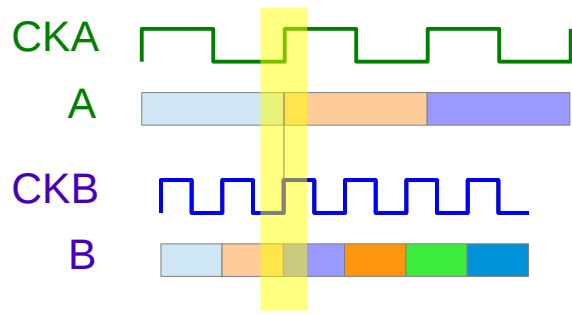CKB

D Q

CKB

Propagation of Metastable States
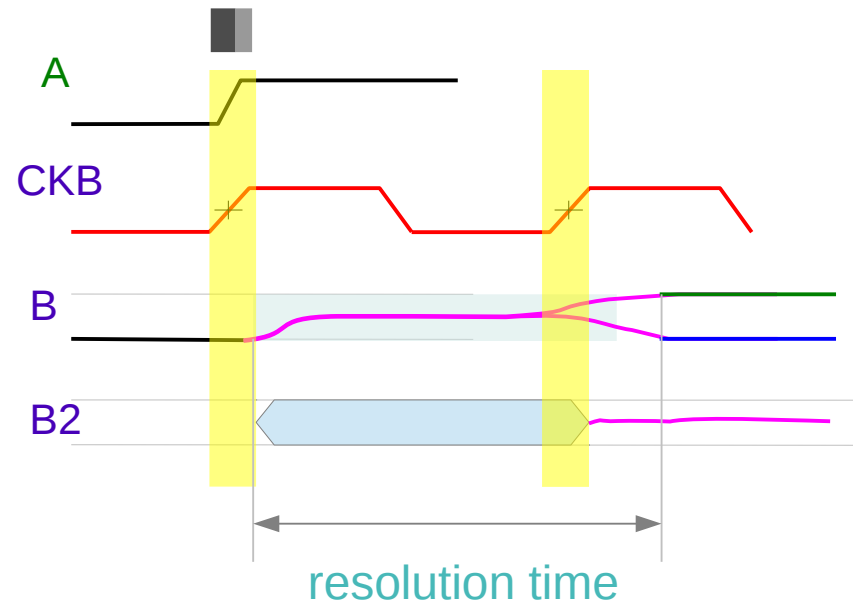

unrelated clock domain

CKA

A

CKB

B

A

CKB

B

B2

most of the time, B2 does not
see metastable state of B

Resolution Time

CKA

A

CKB

B

unrelated clock domain

A

CKB

B

B2

resolution time

A

CKA

B

CKB

B2

CKB

CKB
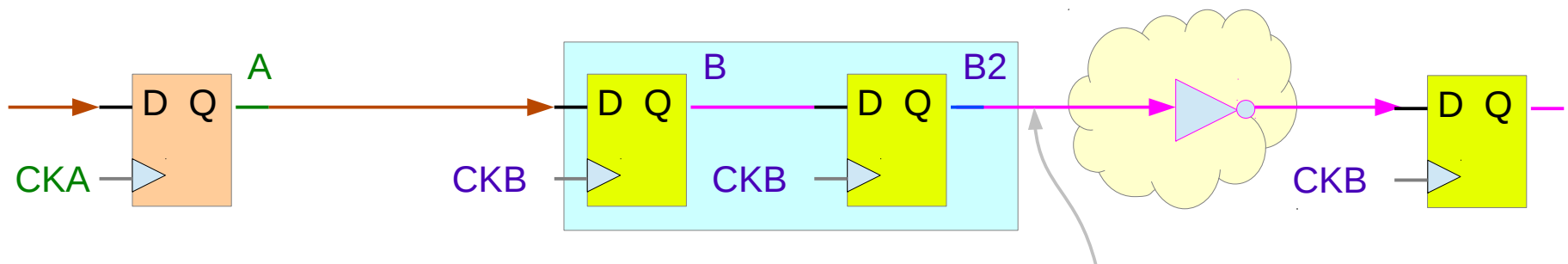
But still, Pr (B2 sees metastable state of B) ≠ 0,
though this probability is significantly reduced

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Waiting and Guarding FlipFlops

waiting for the metastable state to be resolved
guarding all the rest gates
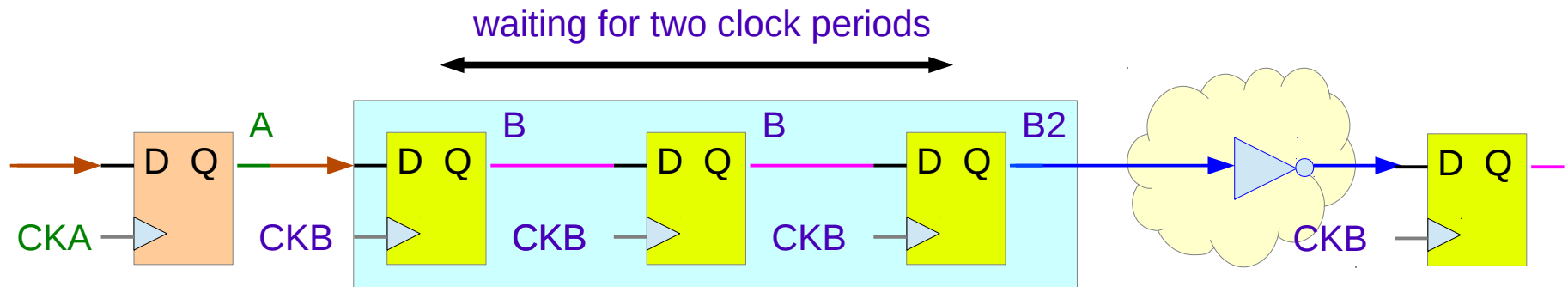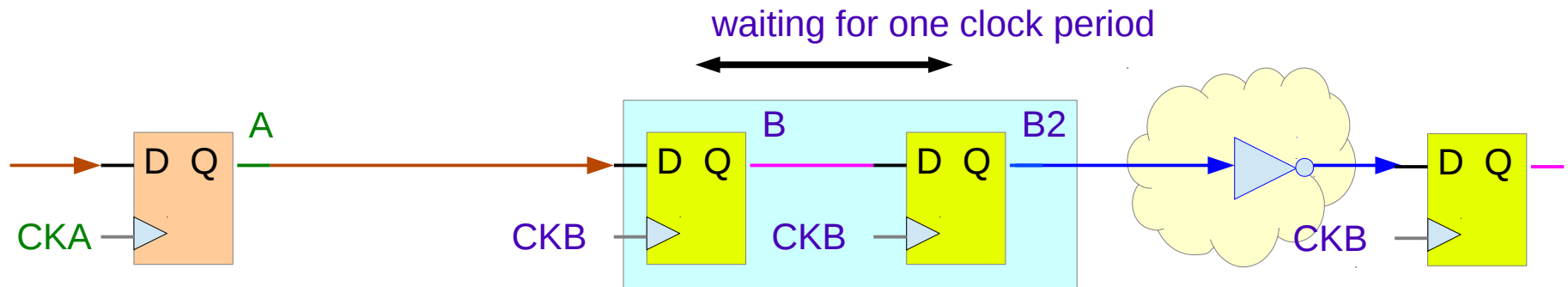
Resolution Time

References

[1]   http://en.wikipedia.org/

[2]   M. M. Mano, C. R. Kime, "Logic and Computer Design Fundamentals", 4th ed.

[3]   J. Stephenson, Understanding Metastability in FPGAs. Altera Corporation white paper. July 2009.