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### **Resolution Time**



unrelated clock domain



$$P(t_{res} > t) = \frac{T_0}{T_c} e^{-t/\tau}$$

 τ time constant depending on a specific flip flop implementation

## P(failure)



$$P(failure) = \frac{T_0}{T_c} e^{-(T_c - T_{setup})/\tau}$$

### Mean Time Between Failures



unrelated clock domain

$$P(t_{res} > t) = \frac{T_0}{T_c} e^{-t/\tau}$$

$$P(t_{res} > T_c - T_{setup}) = \frac{T_0}{T_c} e^{-(T_c - T_{setup})/\tau}$$

$$P(failure) = \frac{T_0}{T_c} e^{-(T_c - T_{setup})/\tau}$$

input A changes N times per second



#### **Resolution Time**

#### References

[1] http://en.wikipedia.org/

[2] M. M. Mano, C. R. Kime, "Logic and Computer Design Fundamentals", 4<sup>th</sup> ed.

[3] J. Stephenson, Understanding Metastability in FPGAs. Altera Corporation white paper. July 2009.