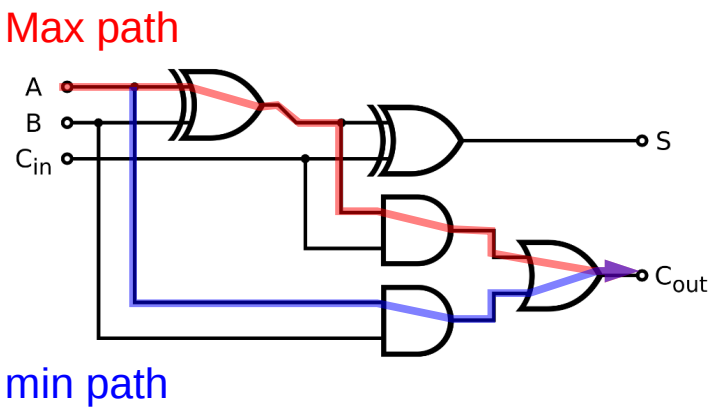
Min Max Timing

Please send corrections (or suggestions) to youngwlim@hotmail.com.

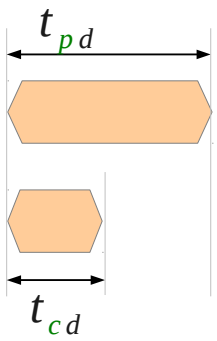
This document was produced by using OpenOffice and Octave.

Max Path / Min Path



Max delay

min delay

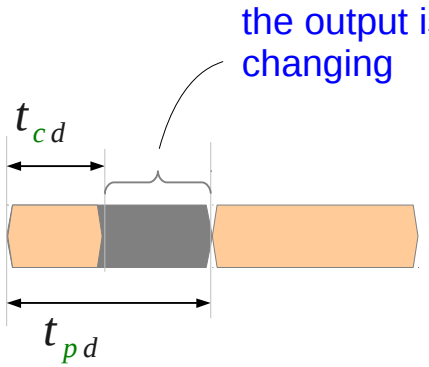


contamination delay

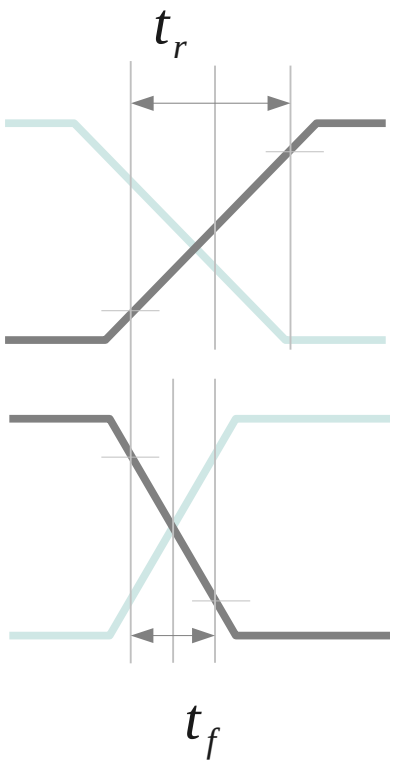
propagation delay

$$t_{cd} \leq t_{delay} \leq t_{pd}$$

min delay Max delay

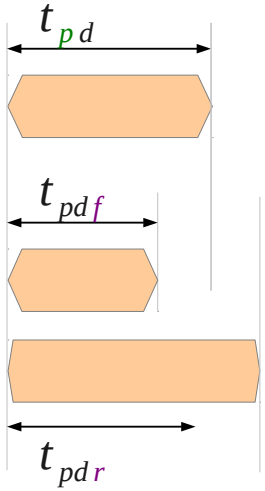


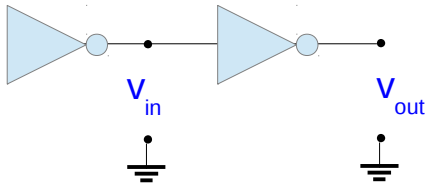
Rise / Fall Times



Max delay

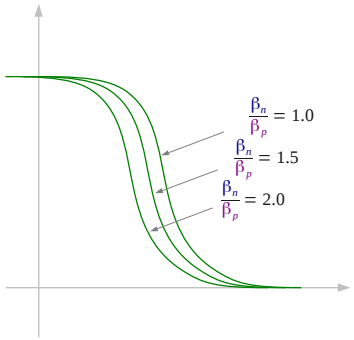
min delay

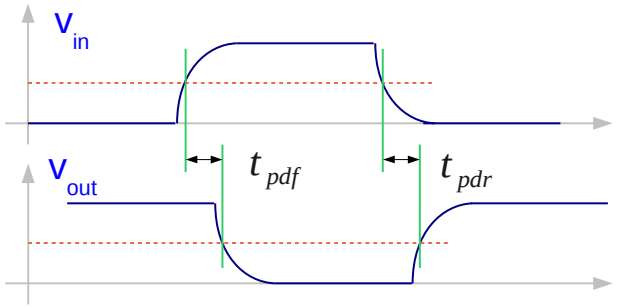




$$\frac{\beta_n}{\beta_p} > 1 \qquad \frac{R_n}{R_p} < 1$$

$$\frac{t_f}{t_r} = \frac{2.2\,\tau_n}{2.2\,\tau_p} \qquad \frac{\tau_n}{\tau_p} = \frac{R_n C_{out}}{R_p C_{out}} = \frac{R_n}{R_p} < 1$$



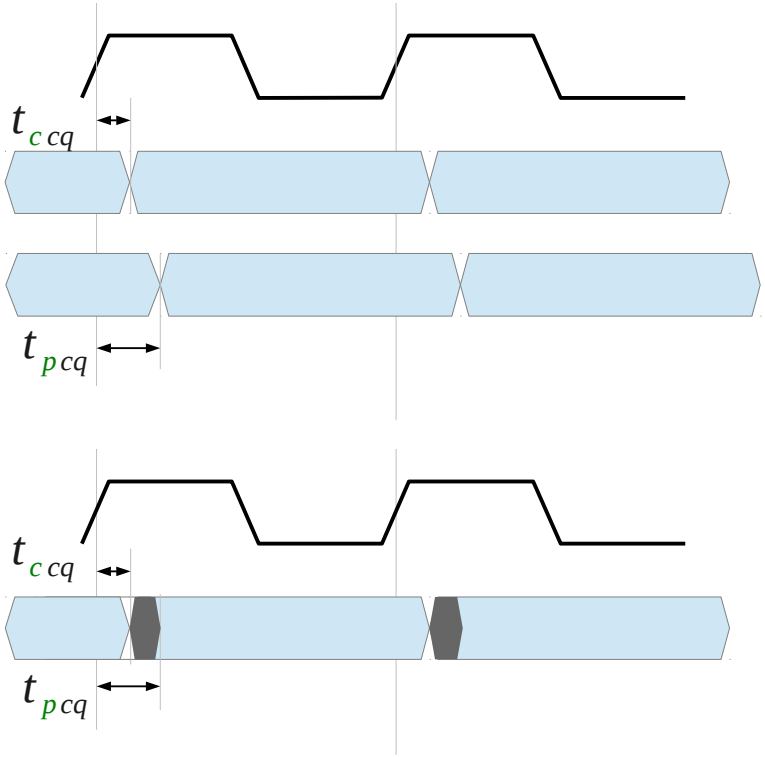


PVT Variation

- Process
- Voltage
- Temperature

High temperature	Max delay
Low temperature	min delay

FF Output Delay



contamination delay

propagation delay

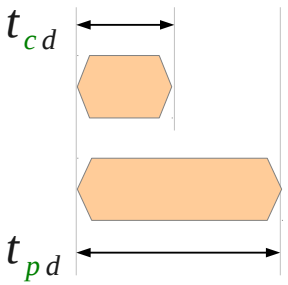
flipflop clock-to-q

$$t_{c\,cq} \leq t_{delay} \leq t_{p\,cq}$$

min delay

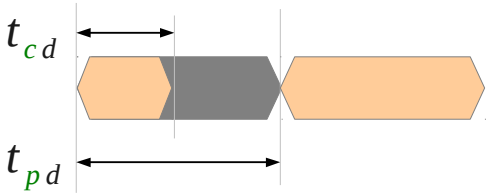
Max delay

Path Delay



contamination delay

propagation delay



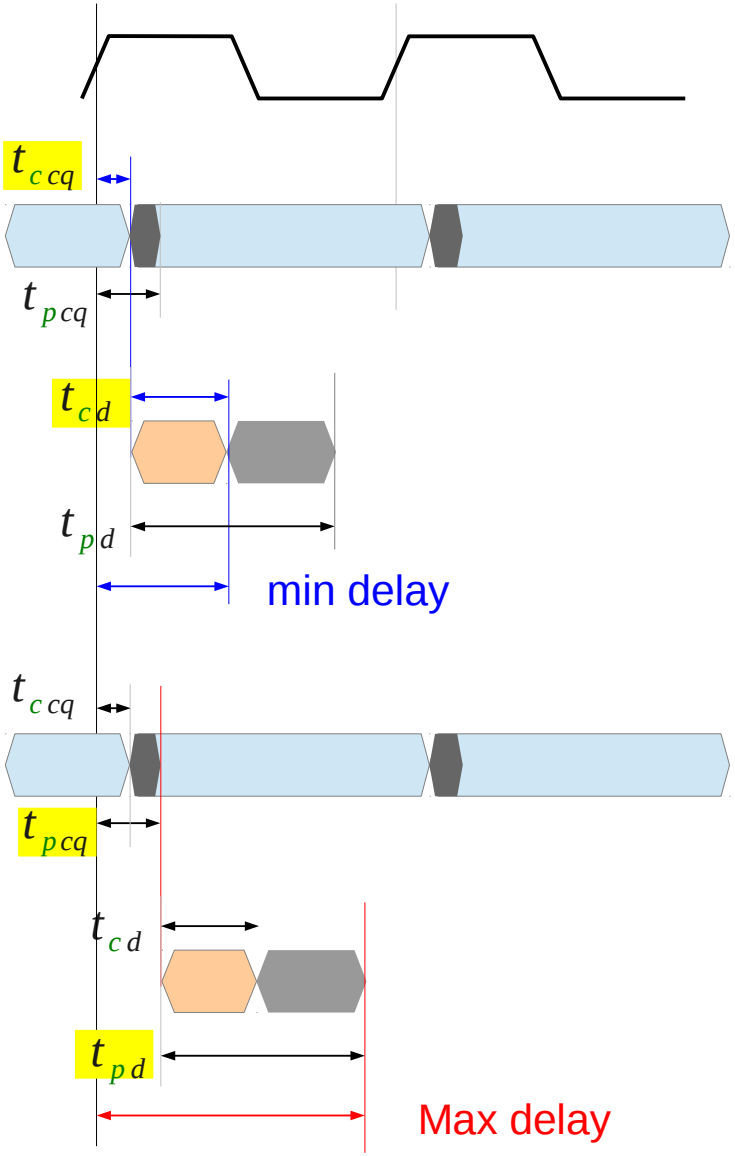
combinational logic delay

$$t_{cd} \leq t_{delay} \leq t_{pd}$$

min delay

Max delay

Reg-to-Reg Delay (1)



$$t_{ccq} \le t_{FF} \le t_{pcq}$$

min delay Max delay

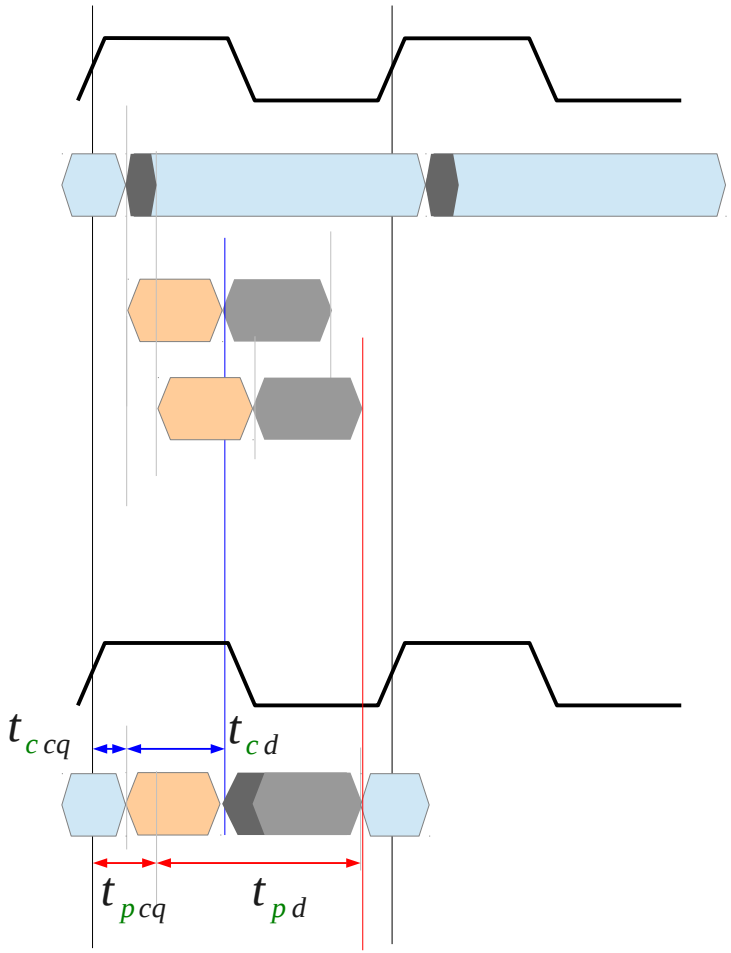
$$t_{cd} \le t_{comb} \le t_{pd}$$

min delay Max delay

$$t_{ccq} + t_{cd} \le t_{delay} \le t_{pcq} + t_{pd}$$

min delay Max delay

Reg-to-Reg Delay (2)



$$t_{c\,cq} \le t_{FF} \le t_{p\,cq}$$

min delay Max delay

$$t_{c\,d} \le t_{comb} \le t_{p\,d}$$

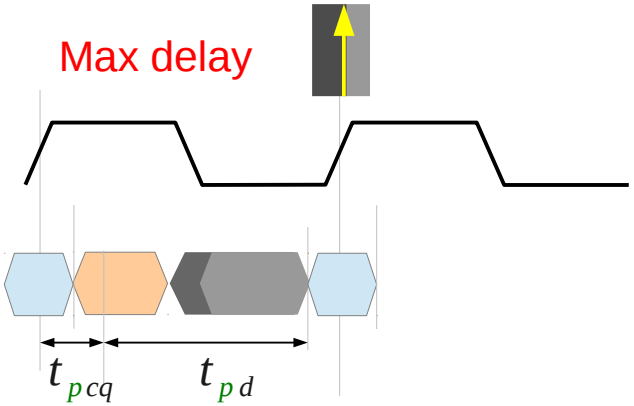
min delay Max delay

$$t_{c\,cq} + t_{c\,d} \le t_{delay} \le t_{p\,cq} + t_{p\,d}$$

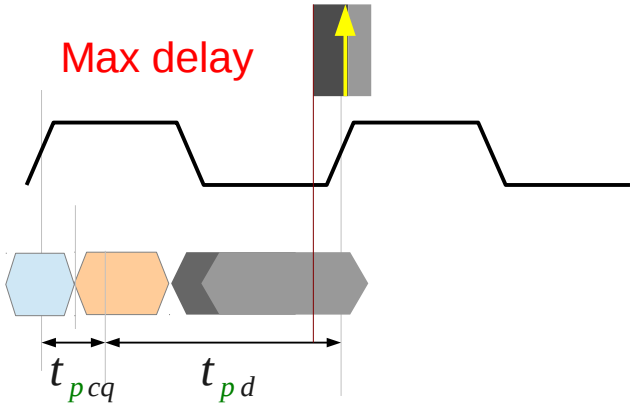
min delay Max delay

Setup Time / Hold Time

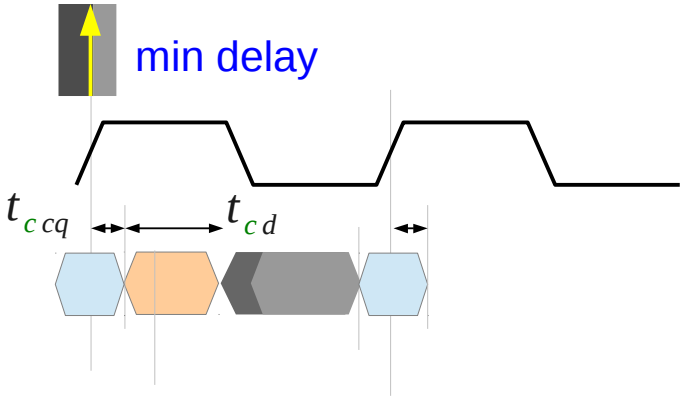
Setup Time OK



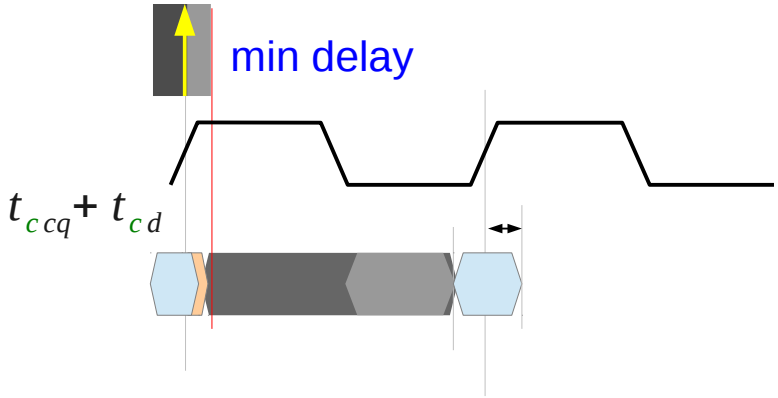
Setup Time Violation



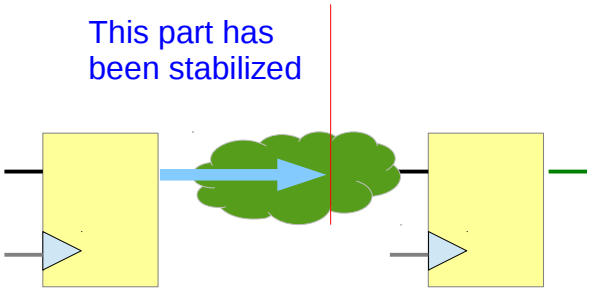
Hold Time OK



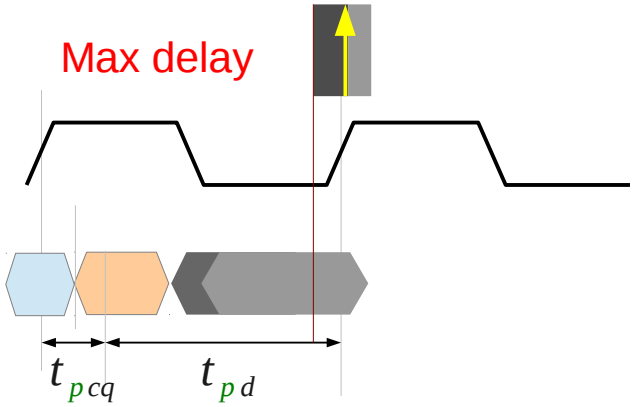
Hold Time Violation

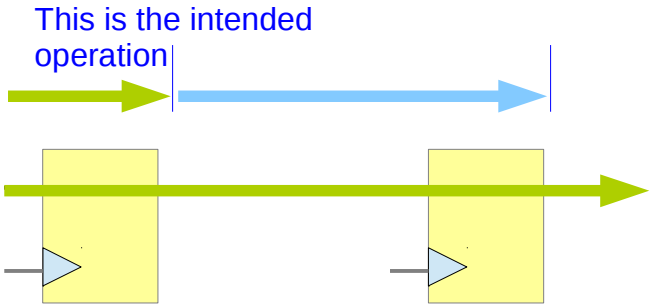


Setup Time / Hold Time



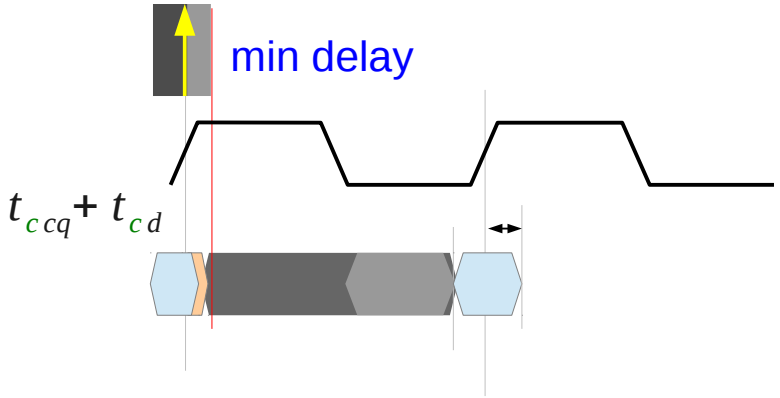
Setup Time Violation





Since the delay is too
small signal passes
through the 2nd FF

Hold Time Violation



Resolution Time

References

[1] http://en.wikipedia.org/
[2] M. M. Mano, C. R. Kime, “Logic and Computer Design Fundamentals”, 4th ed.
[3] J. Stephenson, Understanding Metastability in FPGAs. Altera Corporation white paper. July 2009.