

Clock Skew

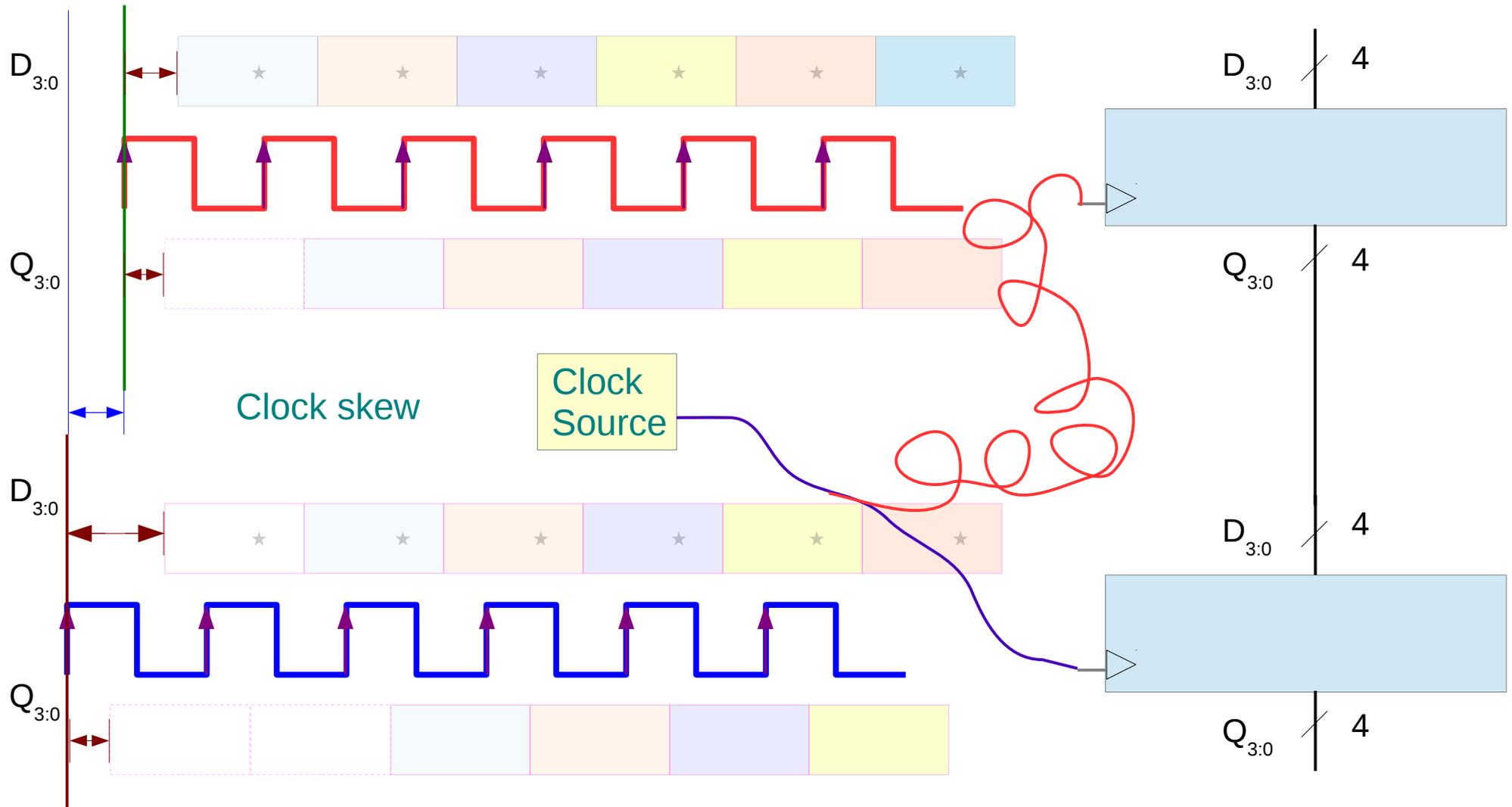
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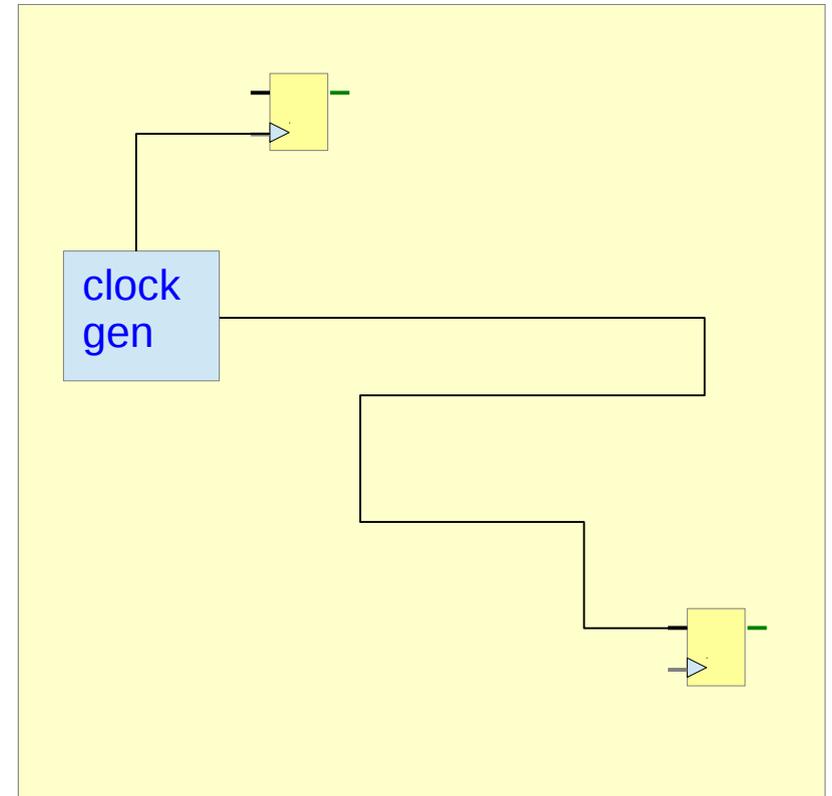
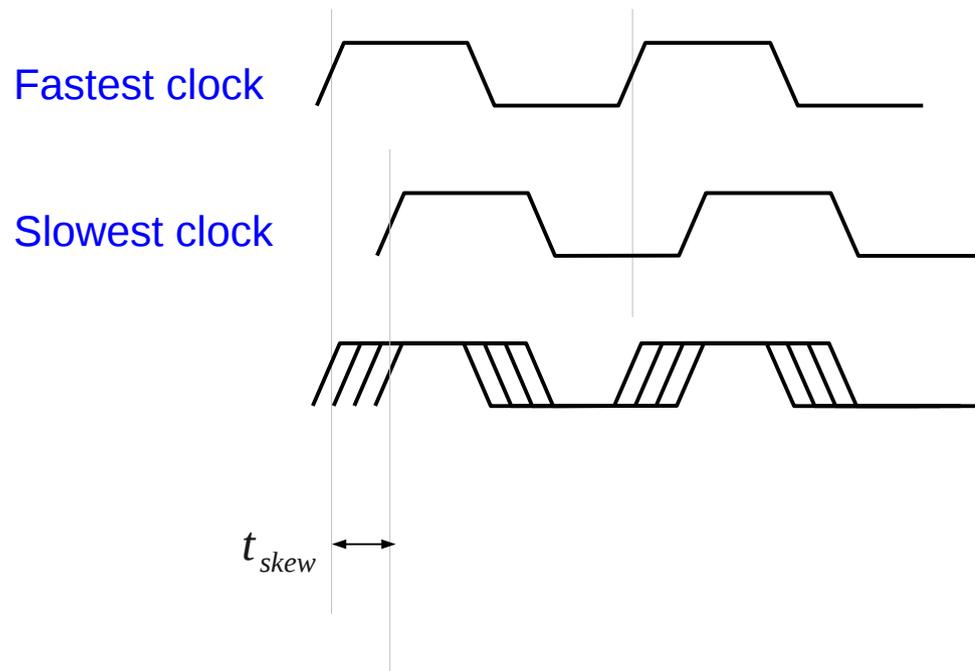
Please send corrections (or suggestions) to youngwlim@hotmail.com.

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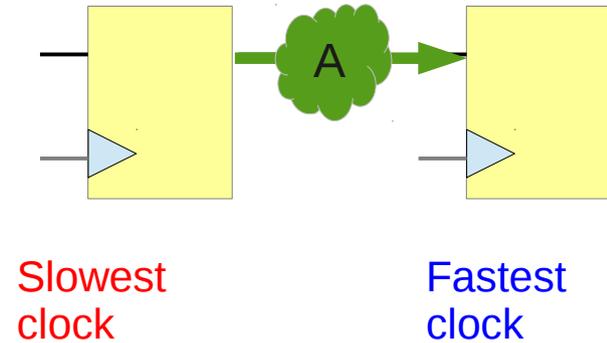
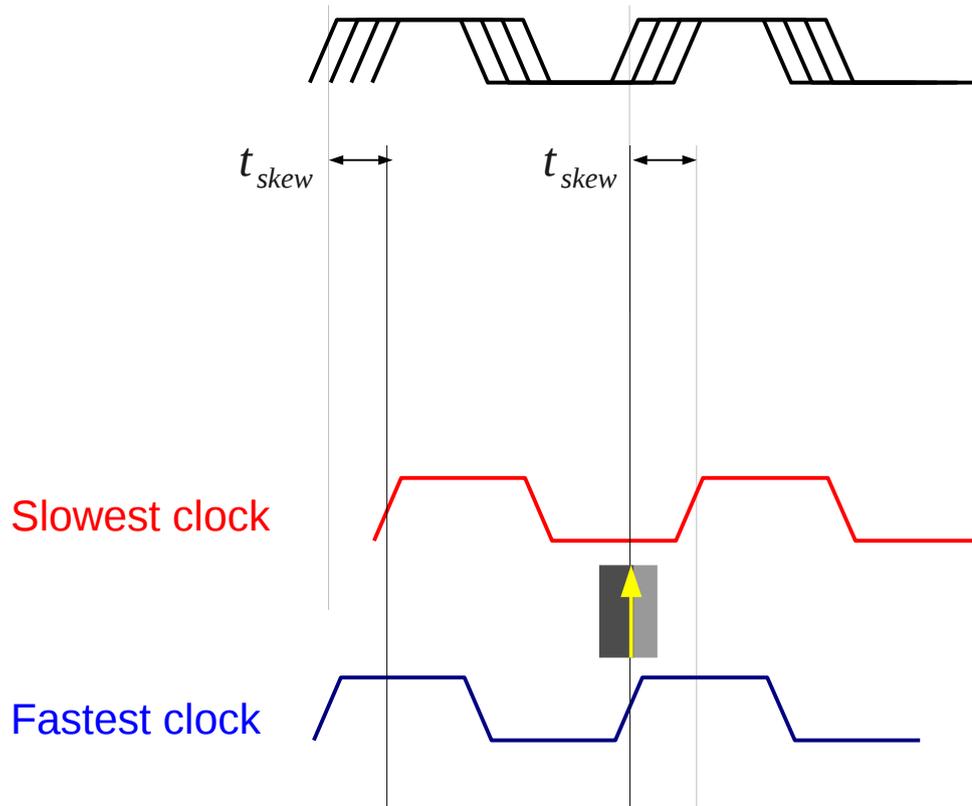
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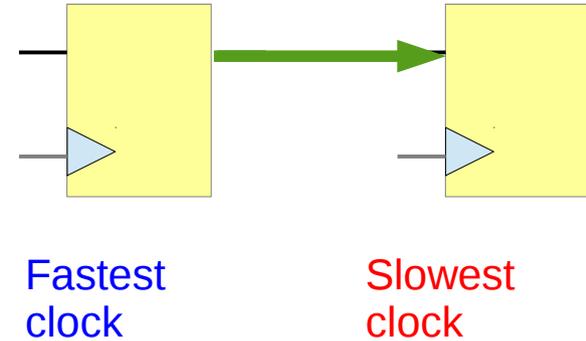
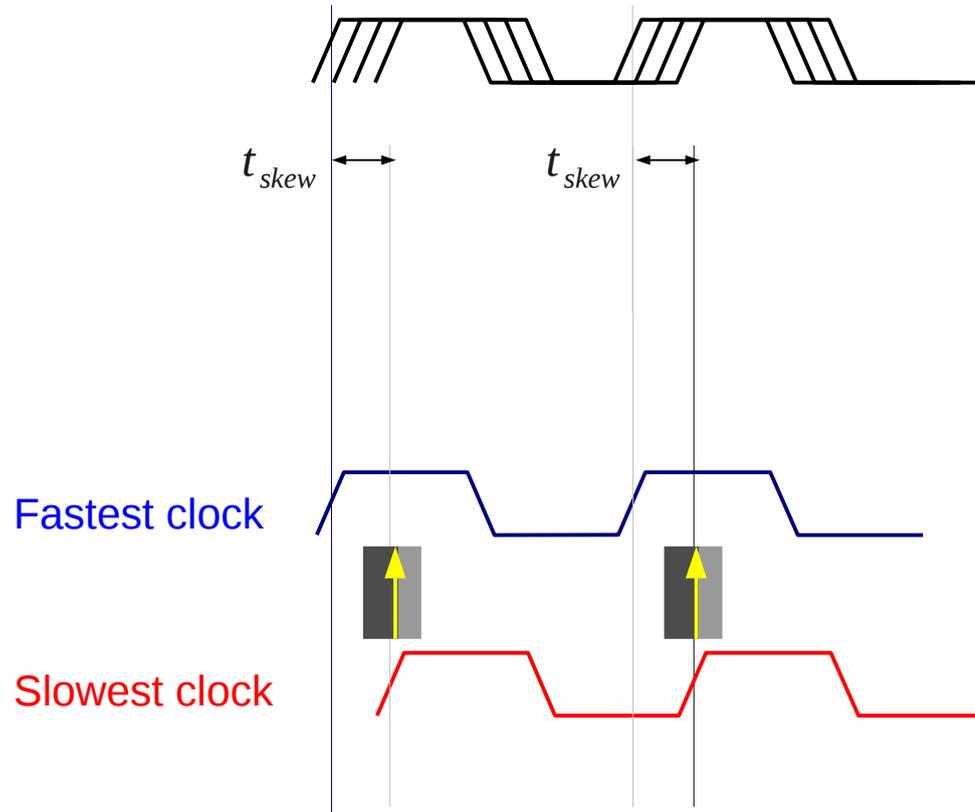
Clock Skew



Setup Time with Clock Skew



Hold Time with Clock Skew



Setup Time Constraints with Clock Skew

Hold Time Constraints with Clock Skew

Resolution Time

References

- [1] <http://en.wikipedia.org/>
- [2] M. M. Mano, C. R. Kime, "Logic and Computer Design Fundamentals", 4th ed.
- [3] J. Stephenson, Understanding Metastability in FPGAs. Altera Corporation white paper. July 2009.