MIPS Assembly

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1/16/14

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```
and $s3,$s1,$s2
or  $s3,$s1,$s2
xor $s3,$s1,$s2
nor $s3,$s1,$s2
```

```
$s3 = $s1 and $s2
$s3 = $s1 or  $s2
$s3 = $s1 xor $s2
$s3 = $s1 nor $s2
```

```
andi $s3,$s1,0x12FA
ori  $s3,$s1,0x12FA
xori $s3,$s1,0x12FA
```

```
$s3 = $s1 and 0x12FA
$s3 = $s1 or  0x12FA
$s3 = $s1 xor 0x12FA
$s3 = $s1 nor 0x12FA
```

```
sll   $t0, $s1, 4        $t0   =  $s1 <<  4
srl   $t0, $s1, 4        $t0   =  $s1 >>  4
sra   $t0, $s1, 4        $t0   =  $s1 >>> 4
```

```
sllv  $t0, $s1, $s2      $t0   =  $s1 <<  ($s2)
srlv  $t0, $s1, $s2      $t0   =  $s1 >>  ($s2)
srav  $t0, $s1, $s2      $t0   =  $s1 >>> ($s2)
```

```
int a = 0x12fa;


#     $s0 = a
      addi $s0, $0,  0x12fa



int a = 0x12fa34fa;


#     $s0 = a
      lui   $s0, 0x12fa
      ori   $s0, $s0, 0x34fa
```

```
#     $s0 = a
      addi $s0, $0,  4          $s0 =   $0  +   4
      addi $s1, $0,  1          $s1 =   $0  +   1
      sll  $s1, $s1, 2          $s1 =   $s1 <<  2
      beq  $s0, $s1, target     if ($s0 == $s1) goto target
      addi $s1, $s1, 1          $s1 =   $s1 +   1
      sub  $s1, $s1, $s0        $s1 =   $s1 -   $s0

target:
      add  $s0, $s1, $s0        $s0 =   $s1  +  $s0
```

```
beq $s0, $s1, target
bne $s0, $s1, target
j   target
jr  $t0
```

```
        addi $s0, $0,  4          $s0 =   $0  +   4
        addi $s1, $0,  1          $s1 =   $0  +   1
        sll  $s1, $s1, 2          $s1 =   $s1 <<  2
        j    target               if ($s0 == $s1) goto target
        addi $s1, $s1, 1          $s1 =   $s1 +   1
        sub  $s1, $s1, $s0        $s1 =   $s1 -   $s0

target:
        add  $s0, $s1, $s0        $s0 =   $s1  +  $s0


        beq  $s0, $s1, target
        bne  $s0, $s1, target
```

References

[1] http://en.wikipedia.org/
[2] M. M. Mano, C. R. Kime, “Logic and Computer Design Fundamentals”, 4th ed.
[3] J. Stephenson, Understanding Metastability in FPGAs. Altera Corporation white paper. July 2009.