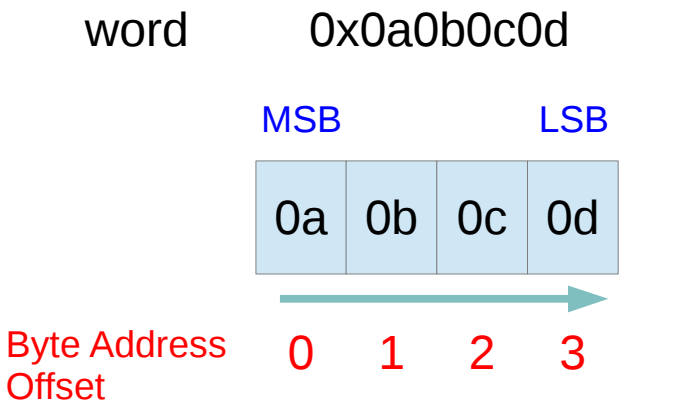
Endian

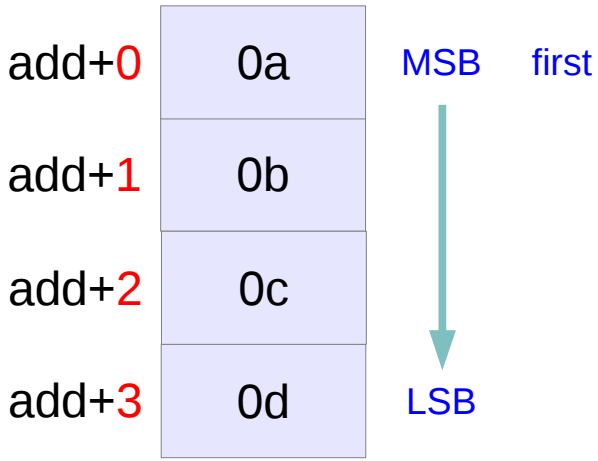
Please send corrections (or suggestions) to youngwlim@hotmail.com.

This document was produced by using OpenOffice and Octave.

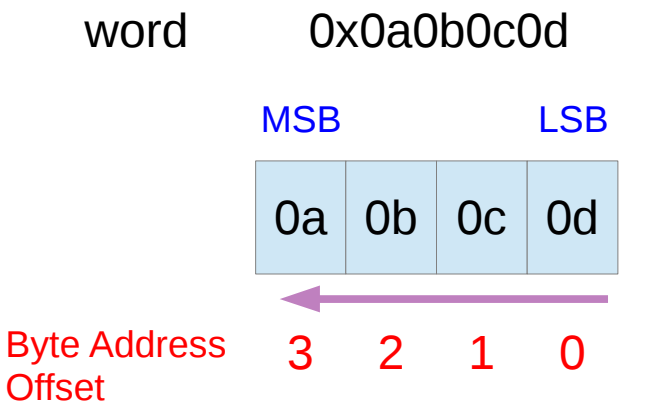
Byte Order

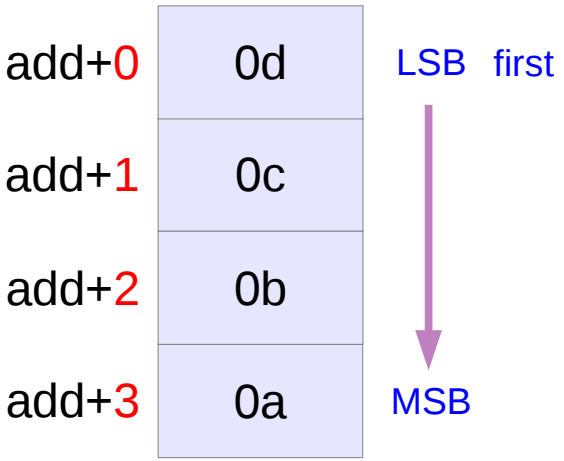
Big Endian





Little Endian

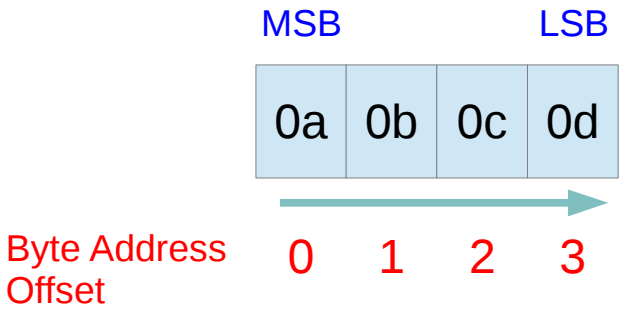




Byte Order in a Memory

Big Endian

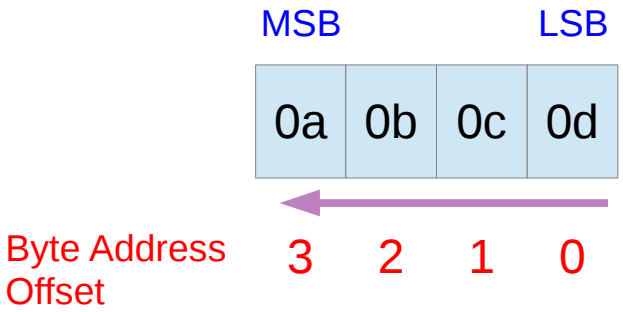
word 0x0a0b0c0d



c	d	e	f
40	f3	07	88
8	9	a	b
01	ef	28	42
4	5	6	7
f2	f1	ac	07
0	1	2	3
0a	0b	0c	0d

Little Endian

word 0x0a0b0c0d

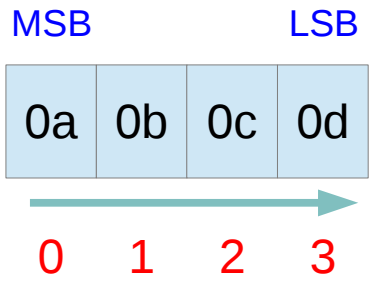


e	e	d	c
40	f3	07	88
b	a	9	8
01	ef	28	42
7	6	5	4
f2	f1	ac	07
3	2	1	0
0a	0b	0c	0d

Bit Numbering

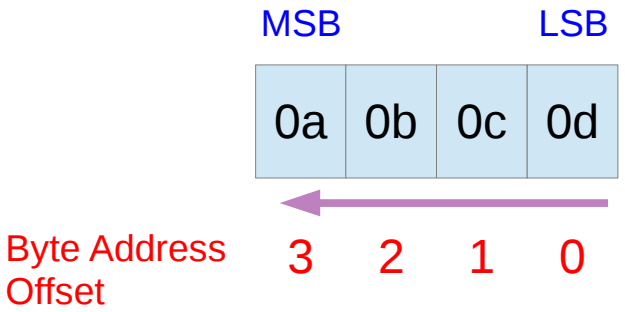
Big Endian

word 0x0a0b0c0d

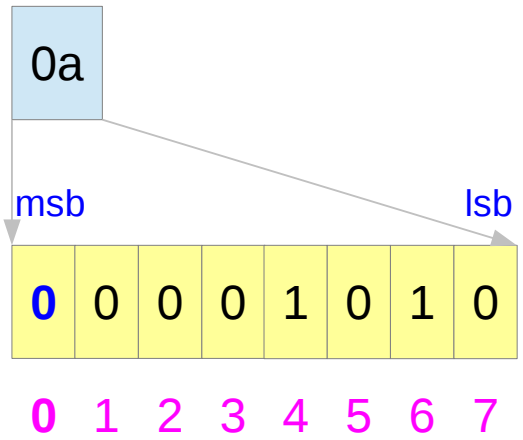


Little Endian

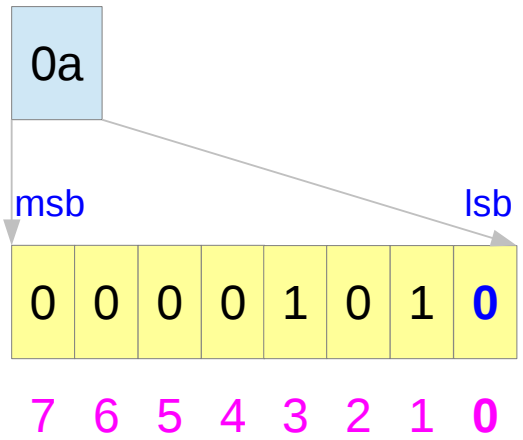
word 0x0a0b0c0d



msb 0 numbering



lsb 0 numbering



Example

Big Endian

	0a				0b				0c				0d			
	0 0 0 0 1 0 1 0				0 0 0 0 1 0 1 1				0 0 0 0 1 1 0 0				0 0 0 0 1 1 0 1			
Bit Offset	**0** 1 2 3 4 5 6 7				**0** 1 2 3 4 5 6 7				**0** 1 2 3 4 5 6 7				**0** 1 2 3 4 5 6 7			
Byte Address Offset	**0**				**1**				**2**				**3**			

Network Byte Order **W[0:31]**

Host Byte Order **W[31:0]**

Little Endian

	0a				0b				0c				0d			
	0 0 0 0 1 0 1 0				0 0 0 0 1 0 1 1				0 0 0 0 1 1 0 0				0 0 0 0 1 1 0 1			
Bit Offset	7 6 5 4 3 2 1 **0**				7 6 5 4 3 2 1 **0**				7 6 5 4 3 2 1 **0**				7 6 5 4 3 2 1 **0**			
Byte Address Offset	**3**				**2**				**1**				**0**			

CPU Endian Usage

- Little endian CPUs include Intel and DEC.
- Big endian CPUs include Motorola 680x0, Sun Sparc and IBM (e.g., PowerPC).
- MIPs and ARM can be configured either way.

References

[1] http://en.wikipedia.org/
[2] D.M. Harris, S. L. Harris, “Digital Design and Computer Architecture”
[3] http://www.linuxjournal.com/node/6788/print