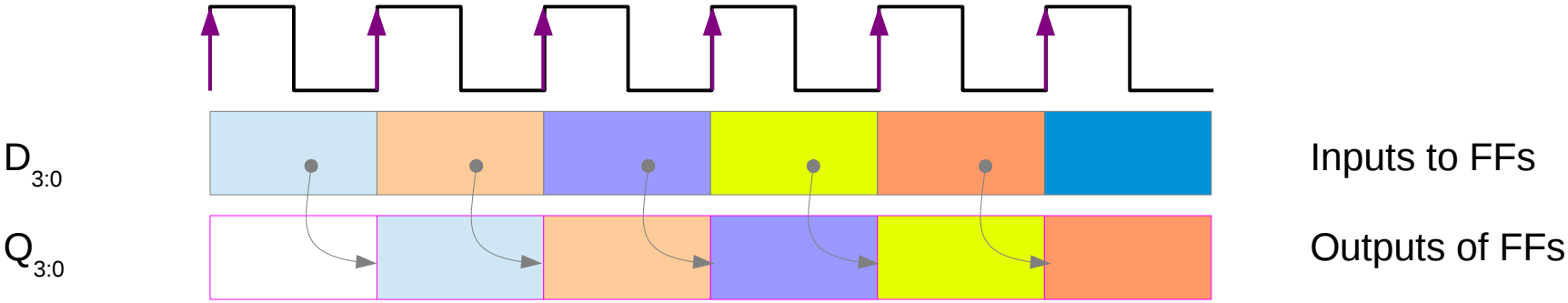
# Finite Sate Machine (4B)

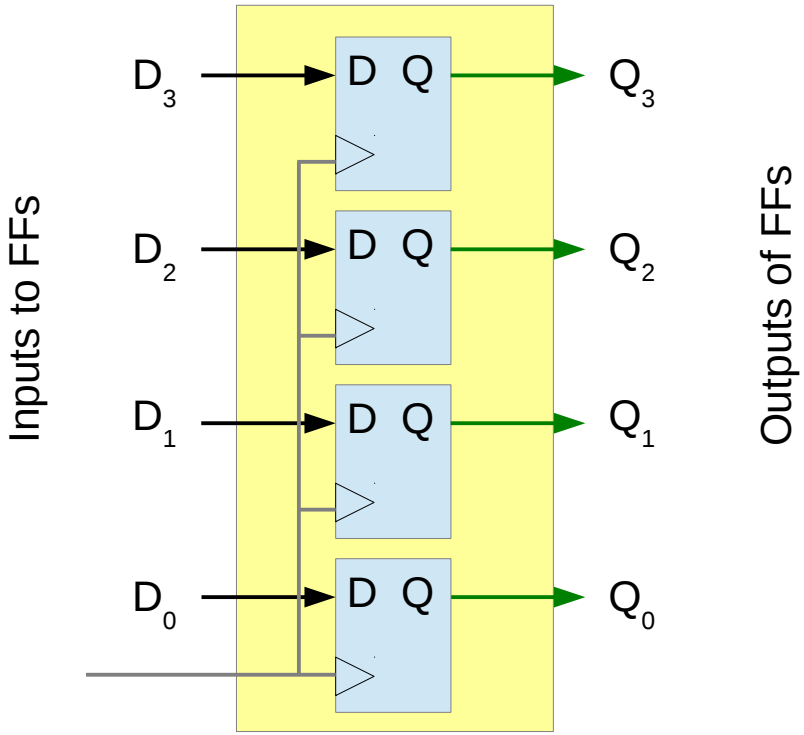
Young Won Lim
3/8/16

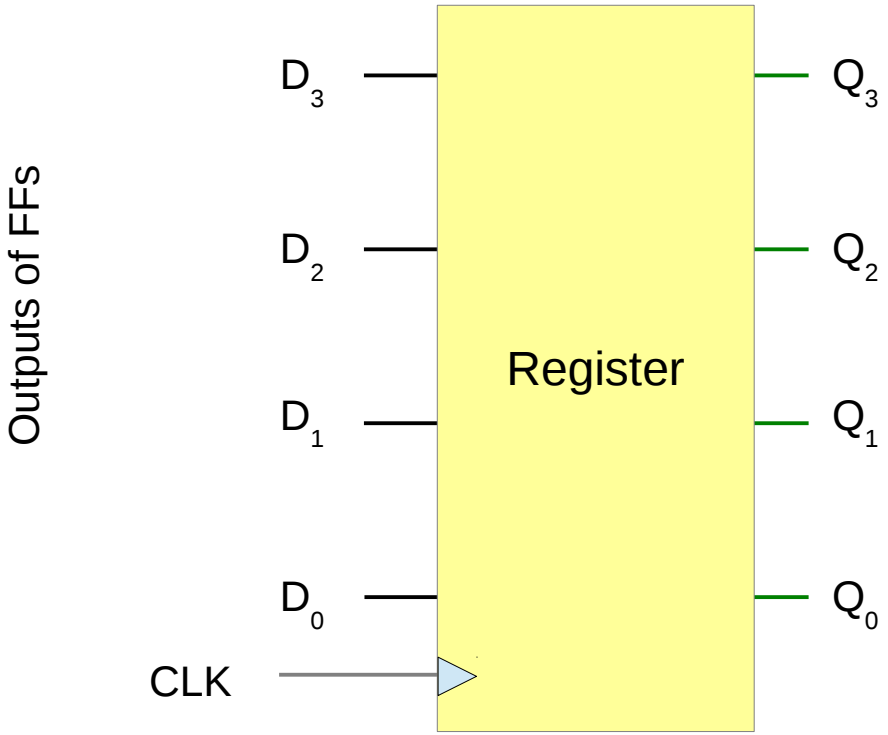
Please send corrections (or suggestions) to youngwlim@hotmail.com.

This document was produced by using OpenOffice and Octave.

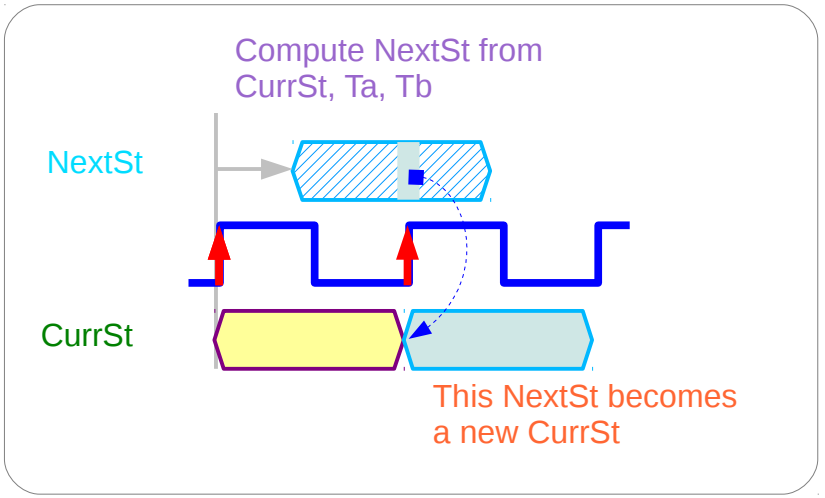
# FF Timing (Ideal)

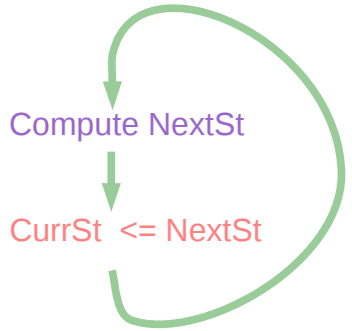


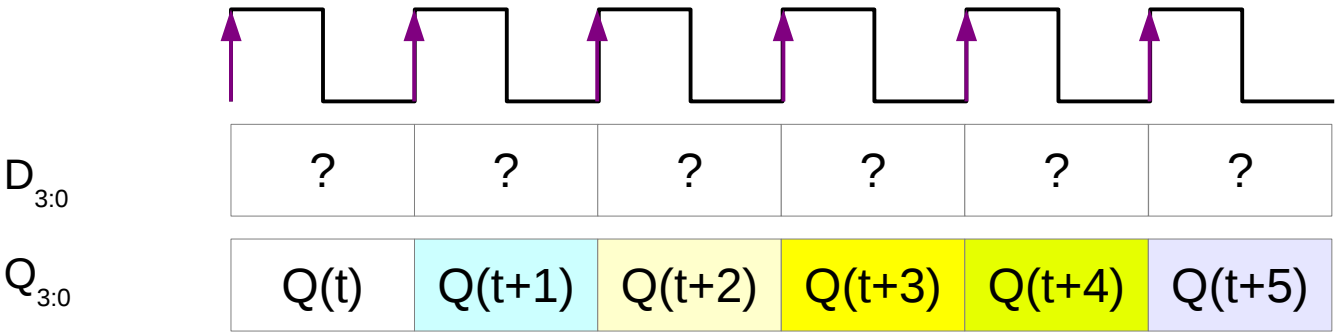



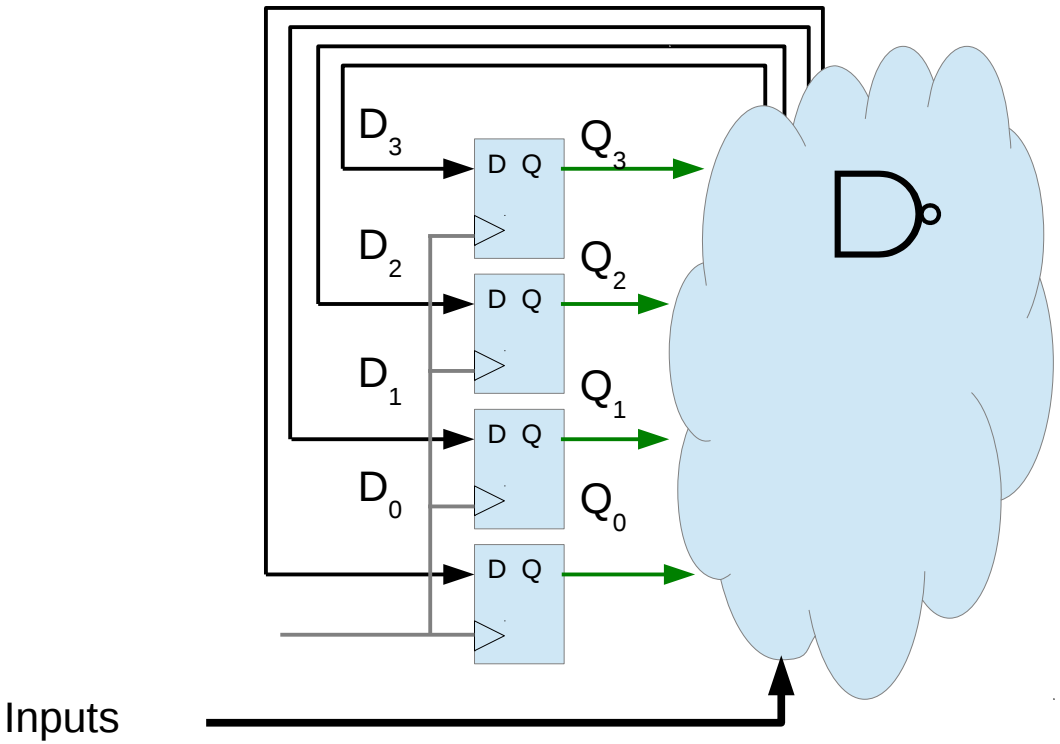
# When NextSt becomes CurrSt



# Finding FF Inputs



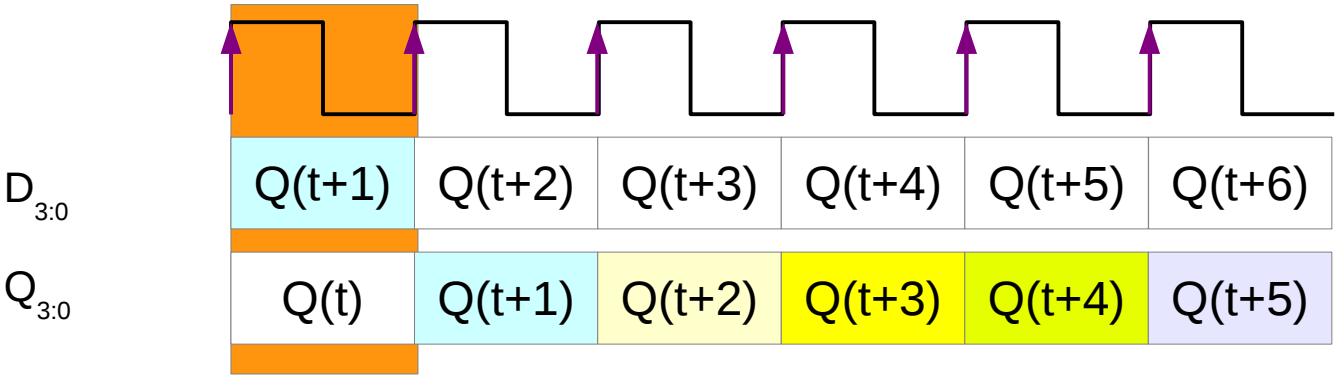

**During** the $t^{th}$ clock edge period,

Compute the next state Q(t+1) using the current state Q(t) and other external inputs

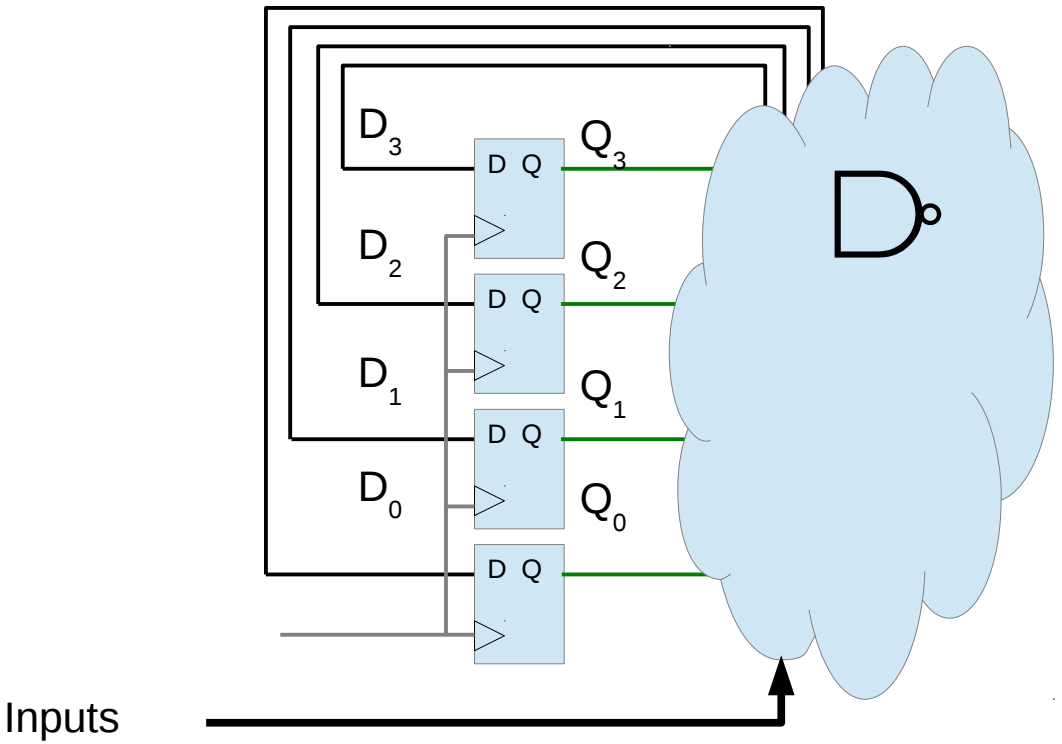
Place it to FF inputs

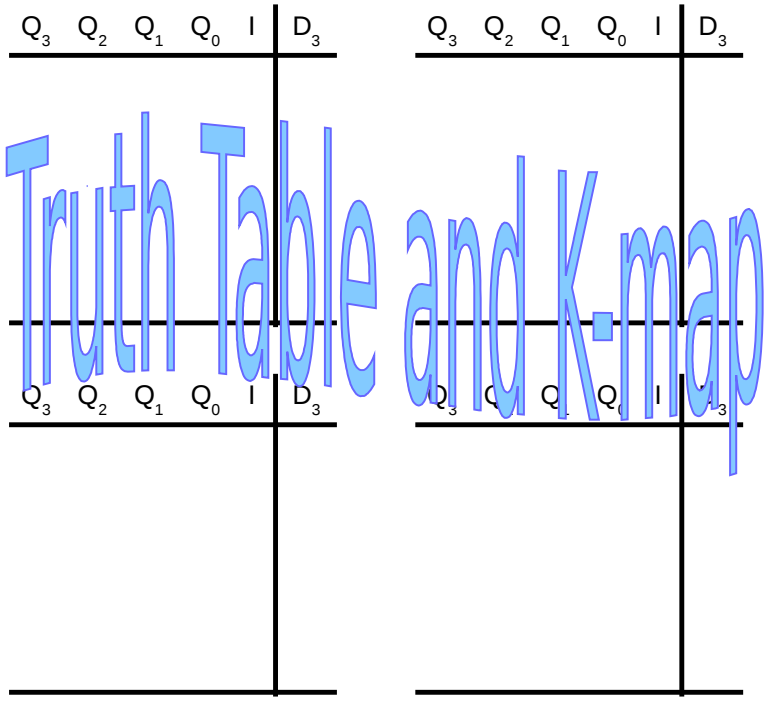
**After** the next clock edge, $(t+1)^{th}$, the computed next state Q(t+1) becomes the current state

# Method of Finding FF Inputs

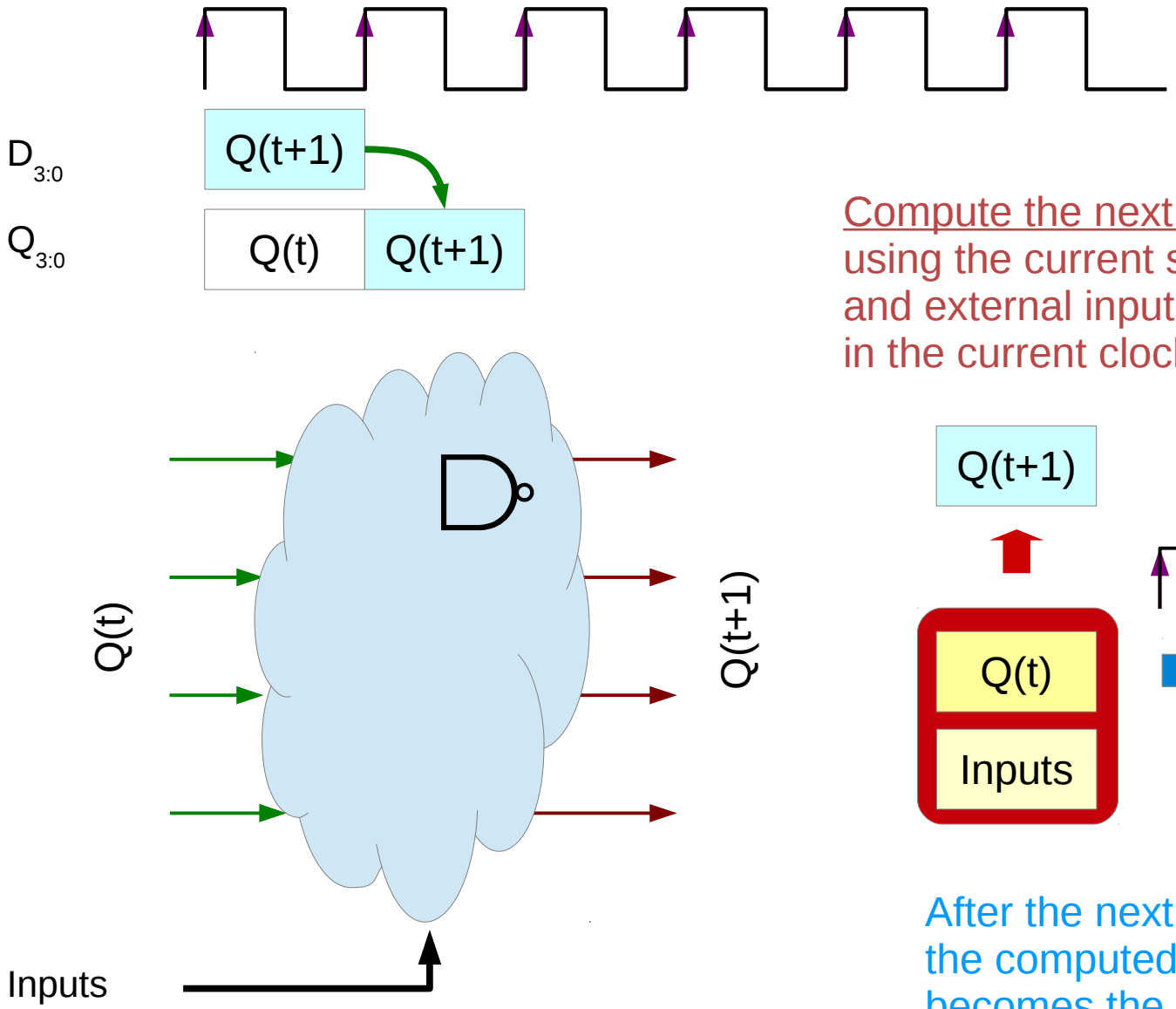



Find the boolean functions
D3, D2, D1, D0
in terms of Q3, Q2, Q1, Q0,
and external inputs
for all possible cases.



# State Transition




Compute the next state
using the current state
and external inputs
in the current clock cycle




After the next clock edge,
the computed next state (FF Inputs)
becomes the current state (FF Outputs)

# Register Timing

## References

[1] http://en.wikipedia.org/
[2] M. M. Mano, C. R. Kime, “Logic and Computer Design Fundamentals”, 4th ed.
[3] D.M. Harris, S. L. Harris, “Digital Design and Computer Architecture”