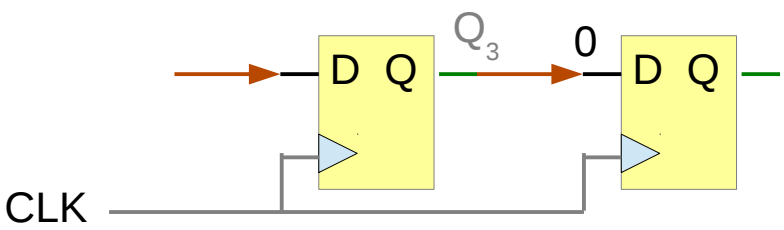
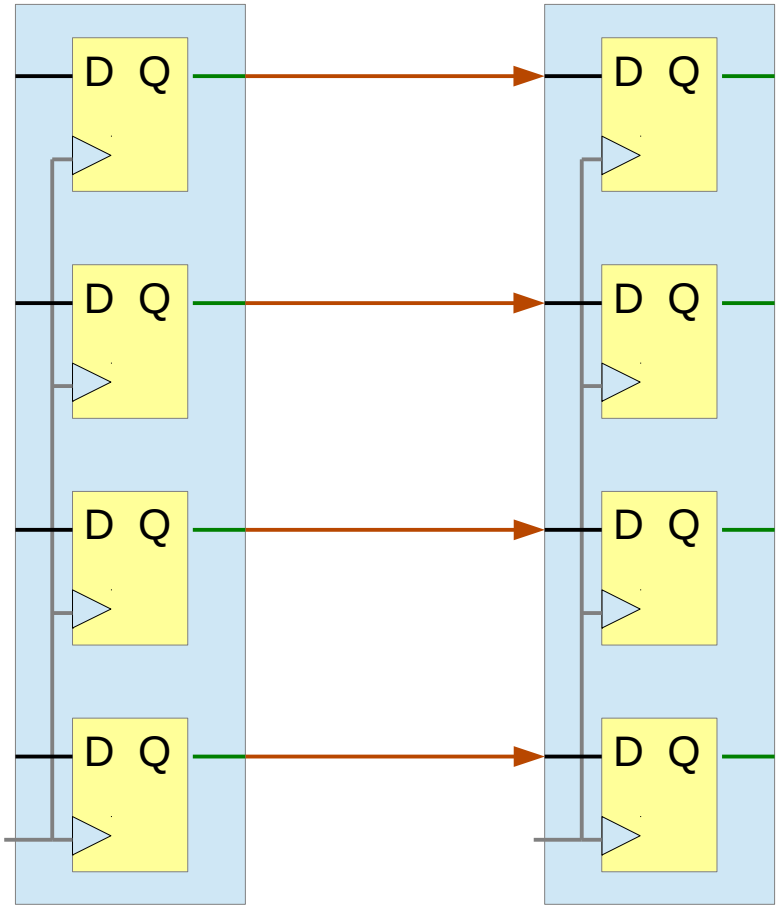
Register (4A)

Please send corrections (or suggestions) to youngwlim@hotmail.com.

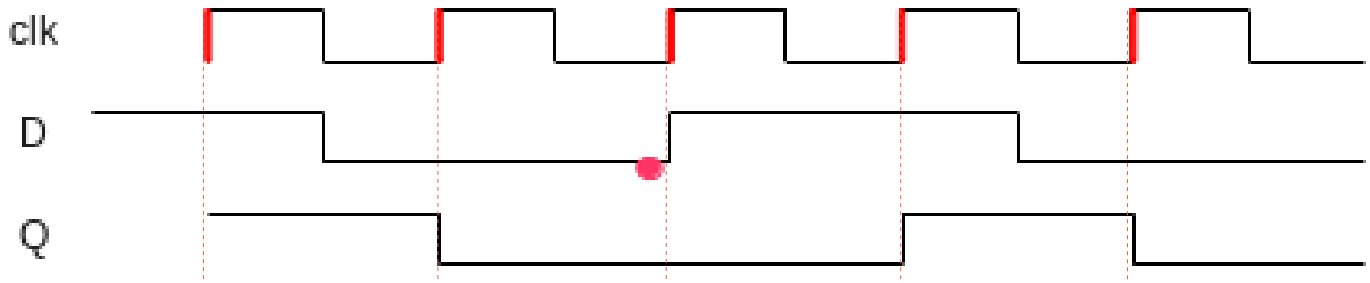
This document was produced by using OpenOffice and Octave.

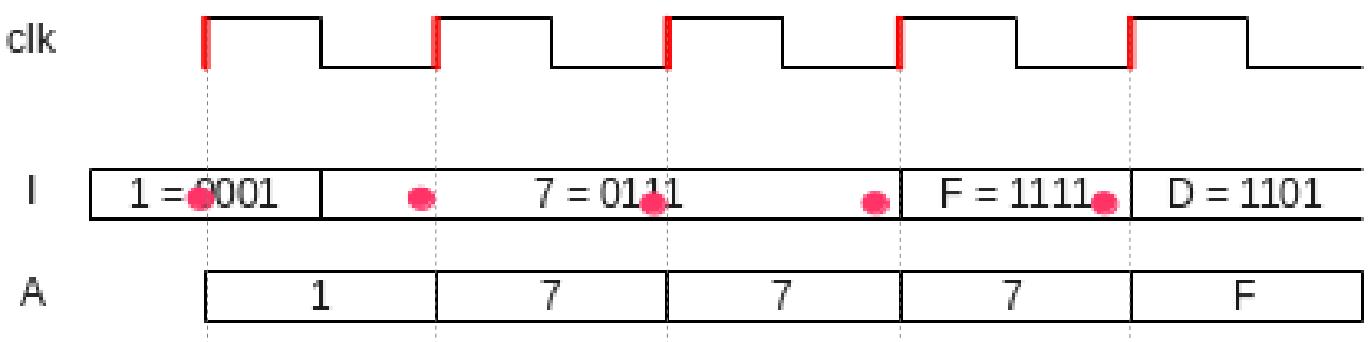
Shift Register v.s. Pipeline Stage Register

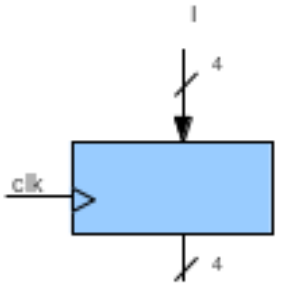




FF and Register Timing

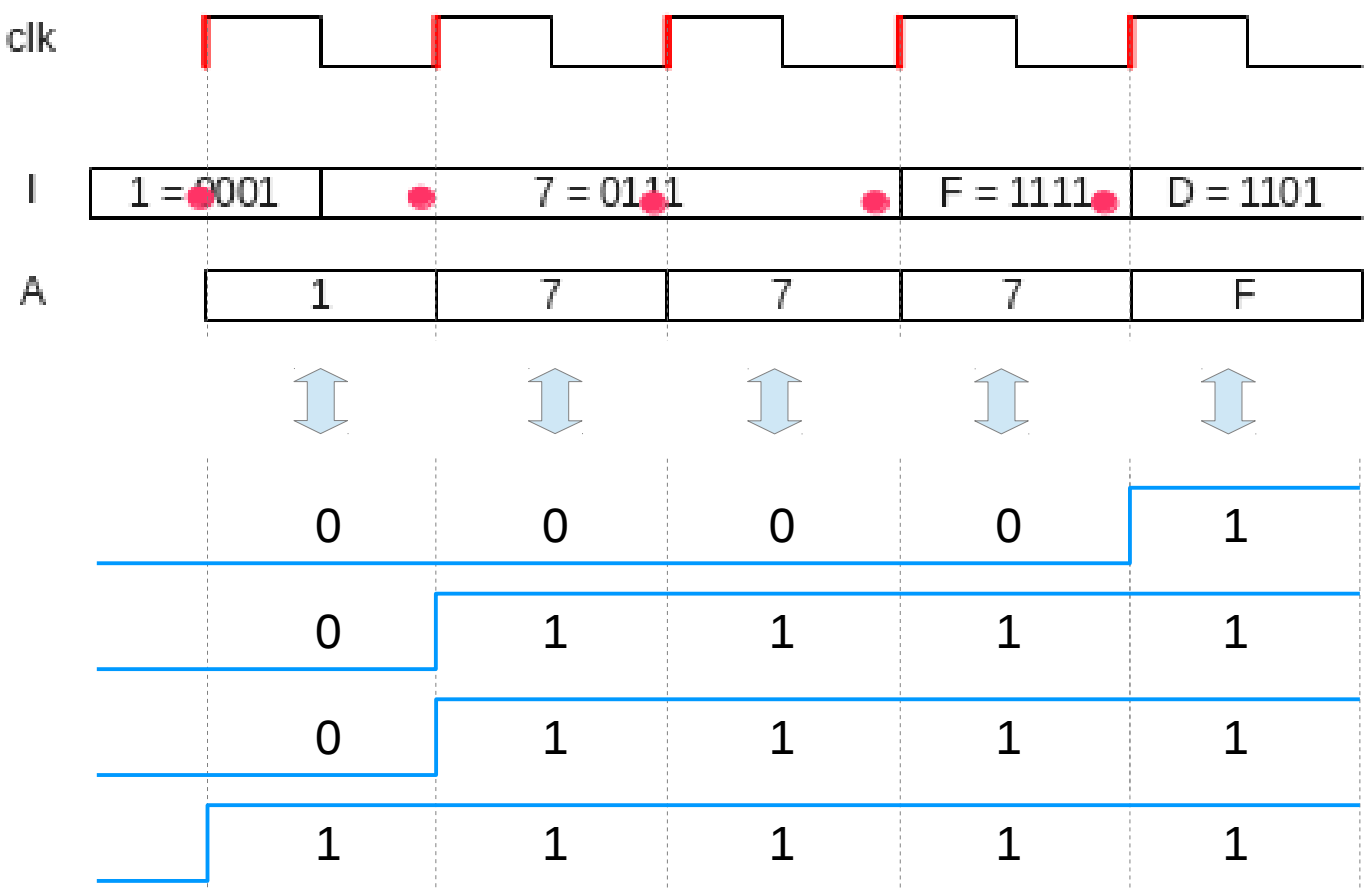


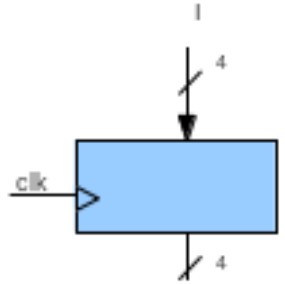




Decimal

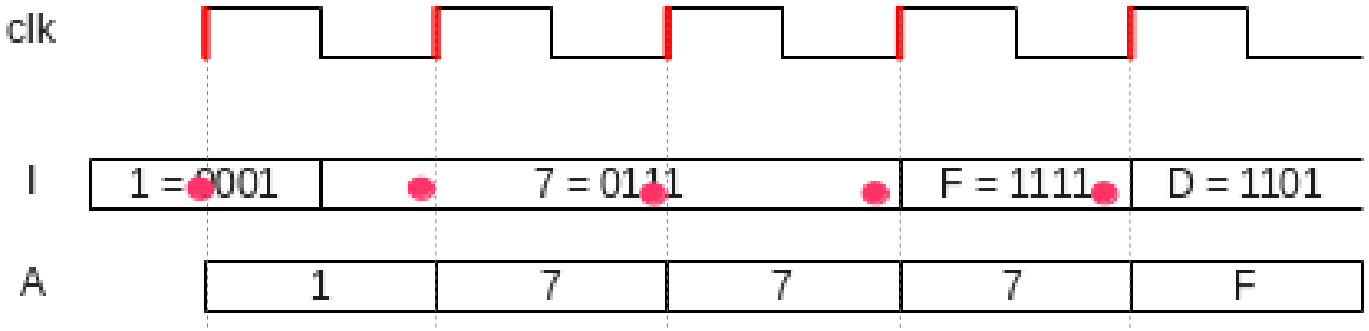
Bus Notation

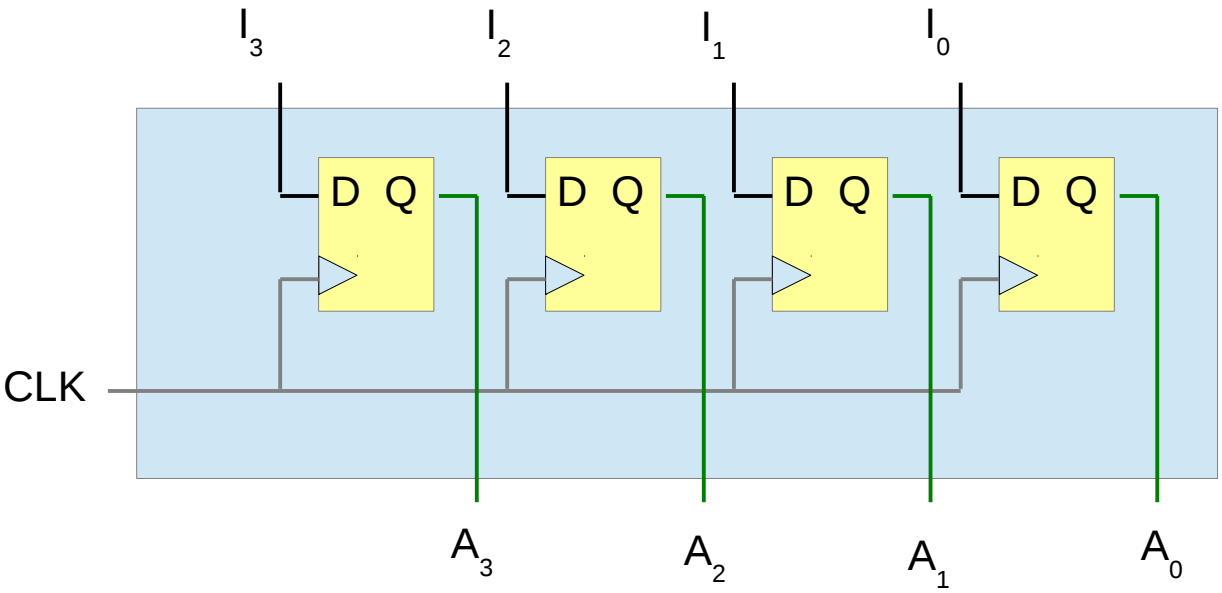


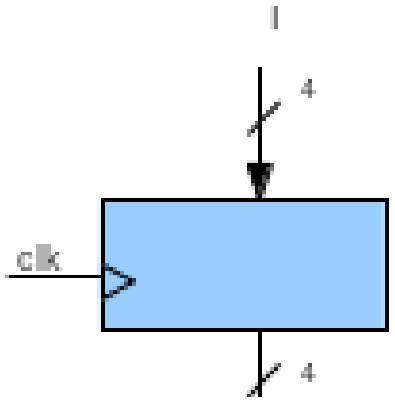


Decimal

Register







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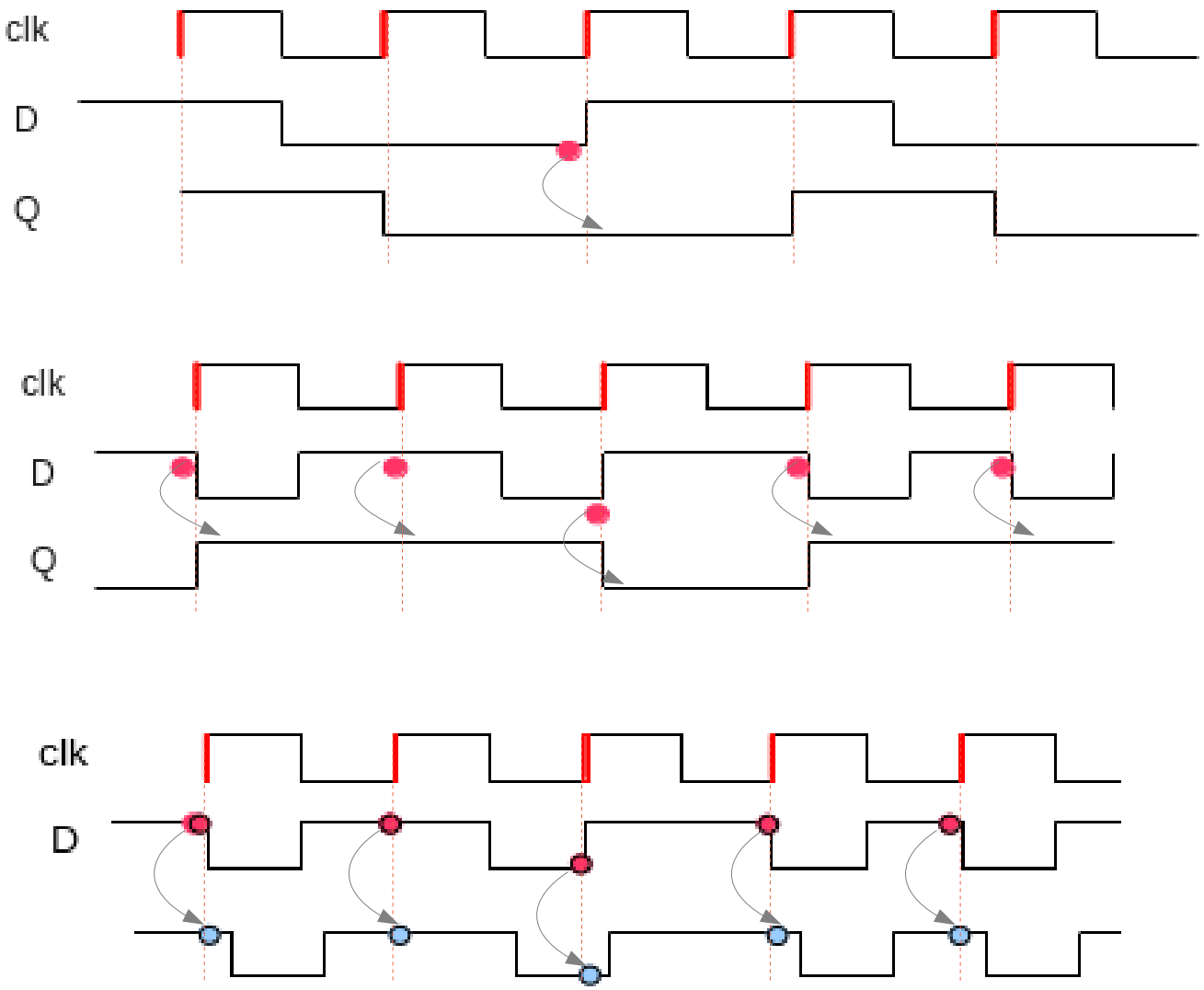
FF Timing

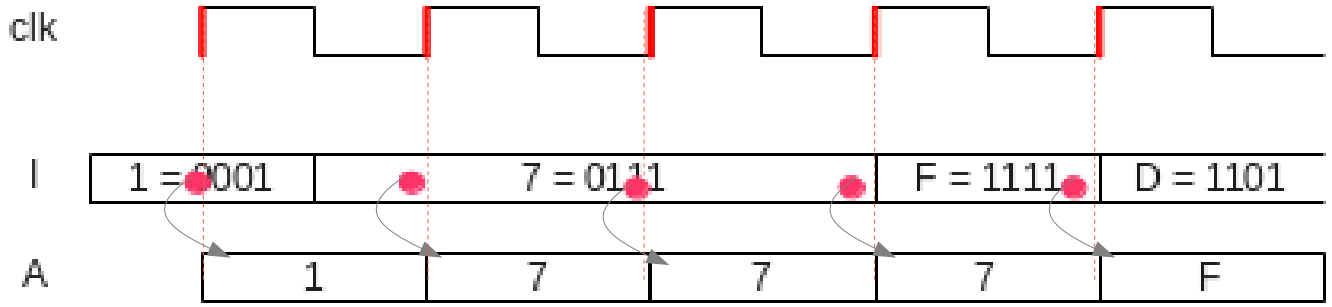


input signal with a delay ignored (ideal case)

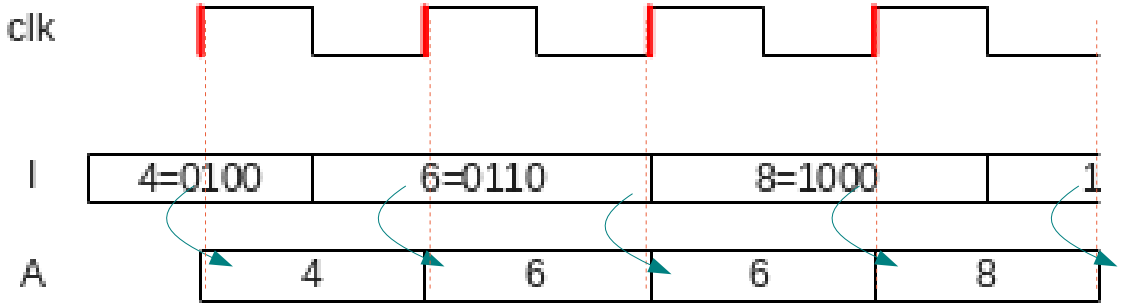
input signal with a delay explicitly shown

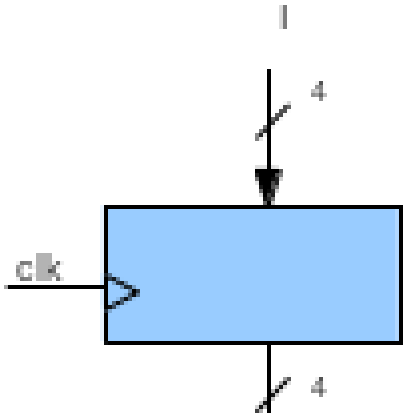
Register Timing

input signal with a delay explicitly shown

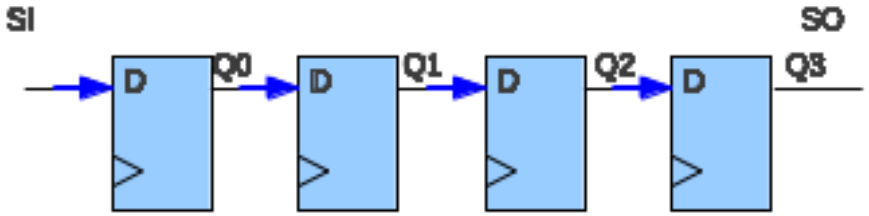


input signal with a delay explicitly shown

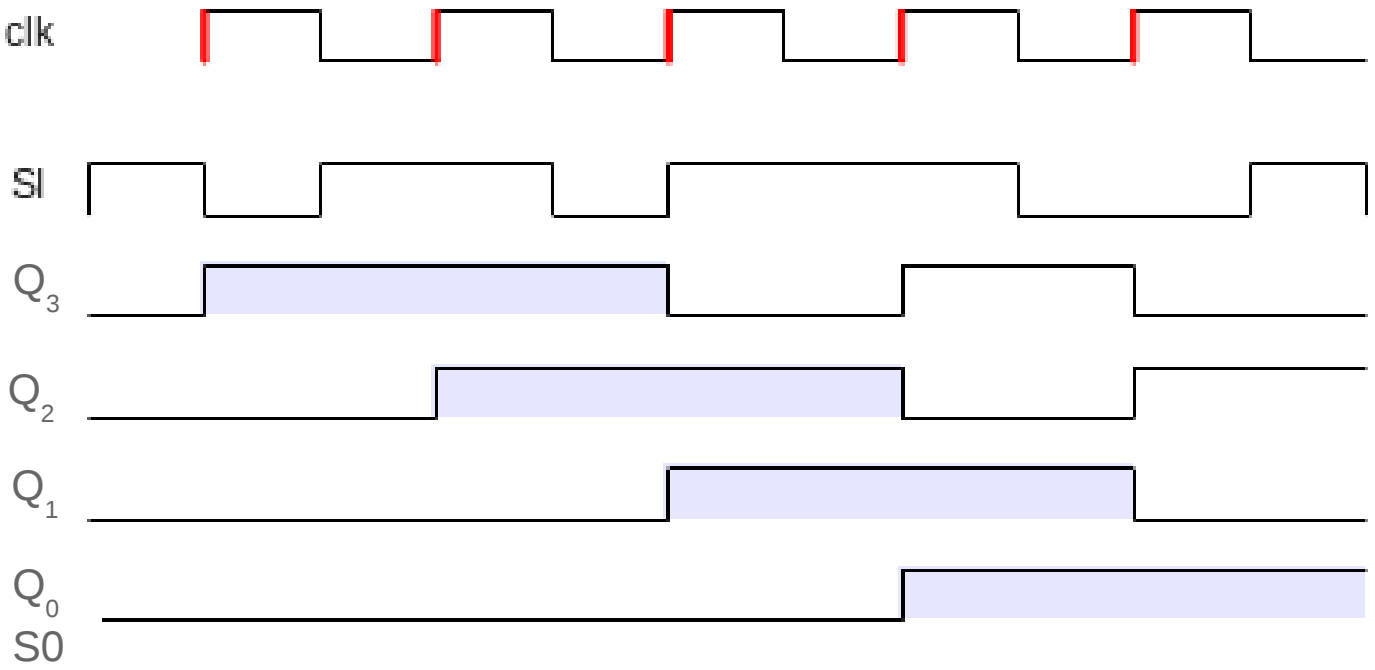




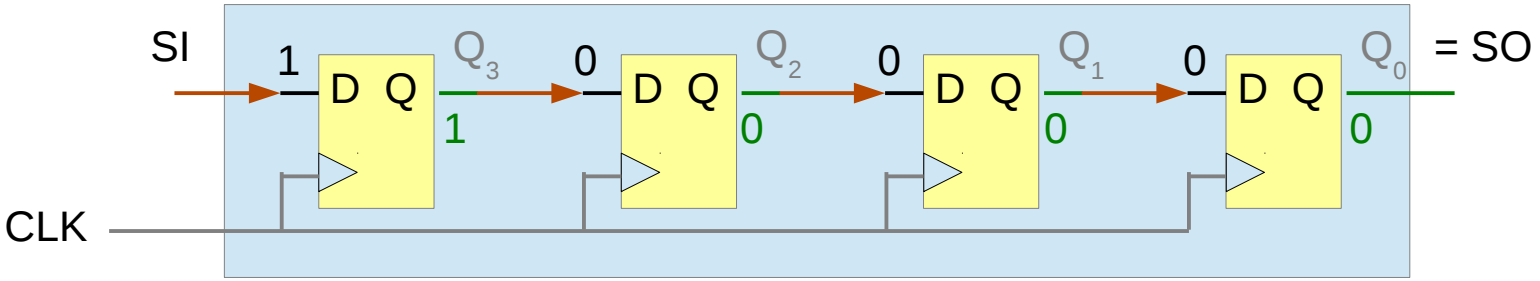
Shift Register Timing



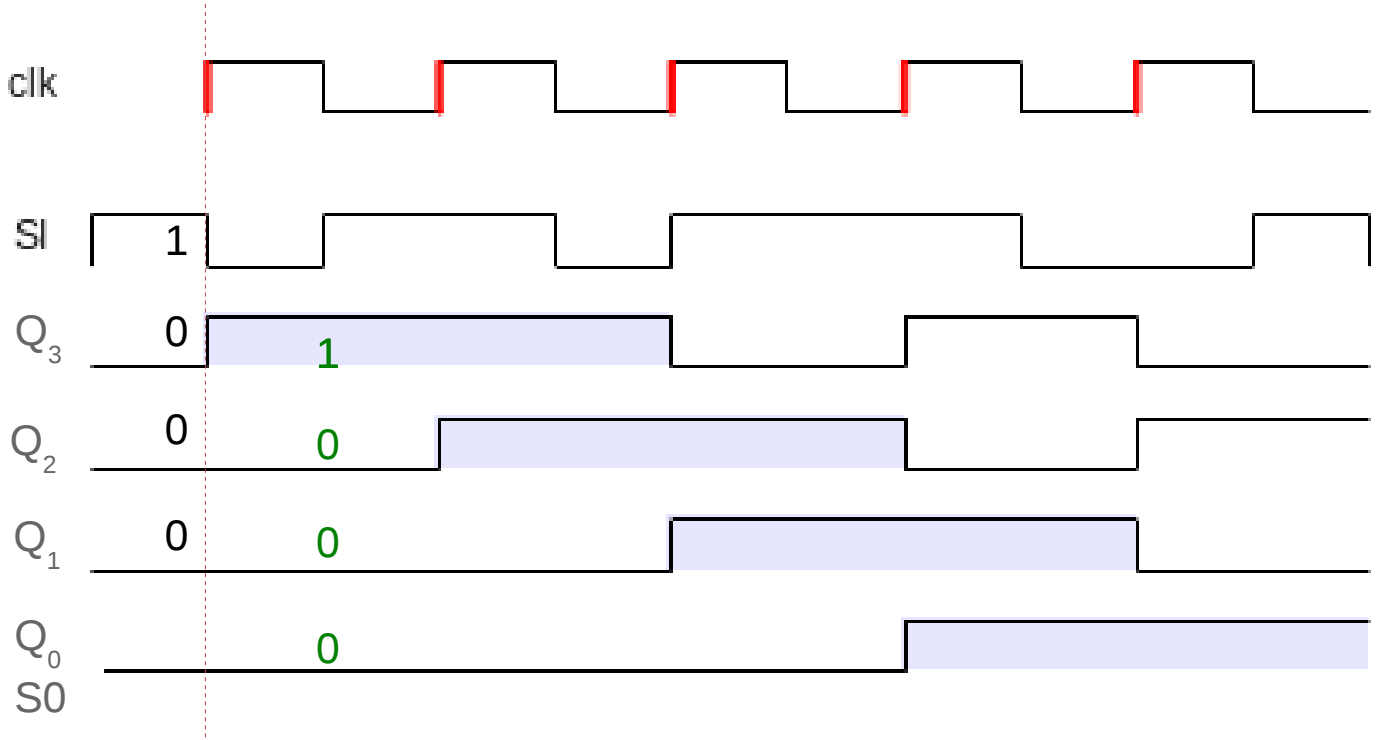
Connected in serial,
but parallel assignments



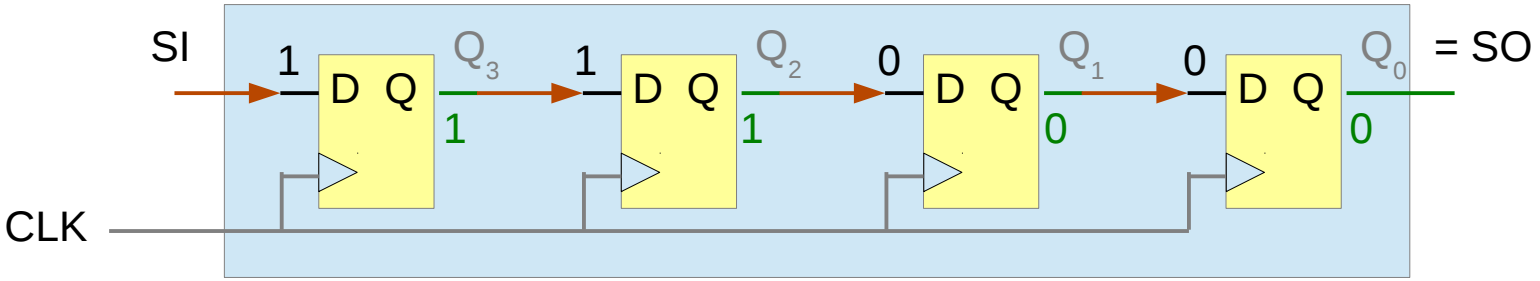
Shift Register Timing – Cycle 1



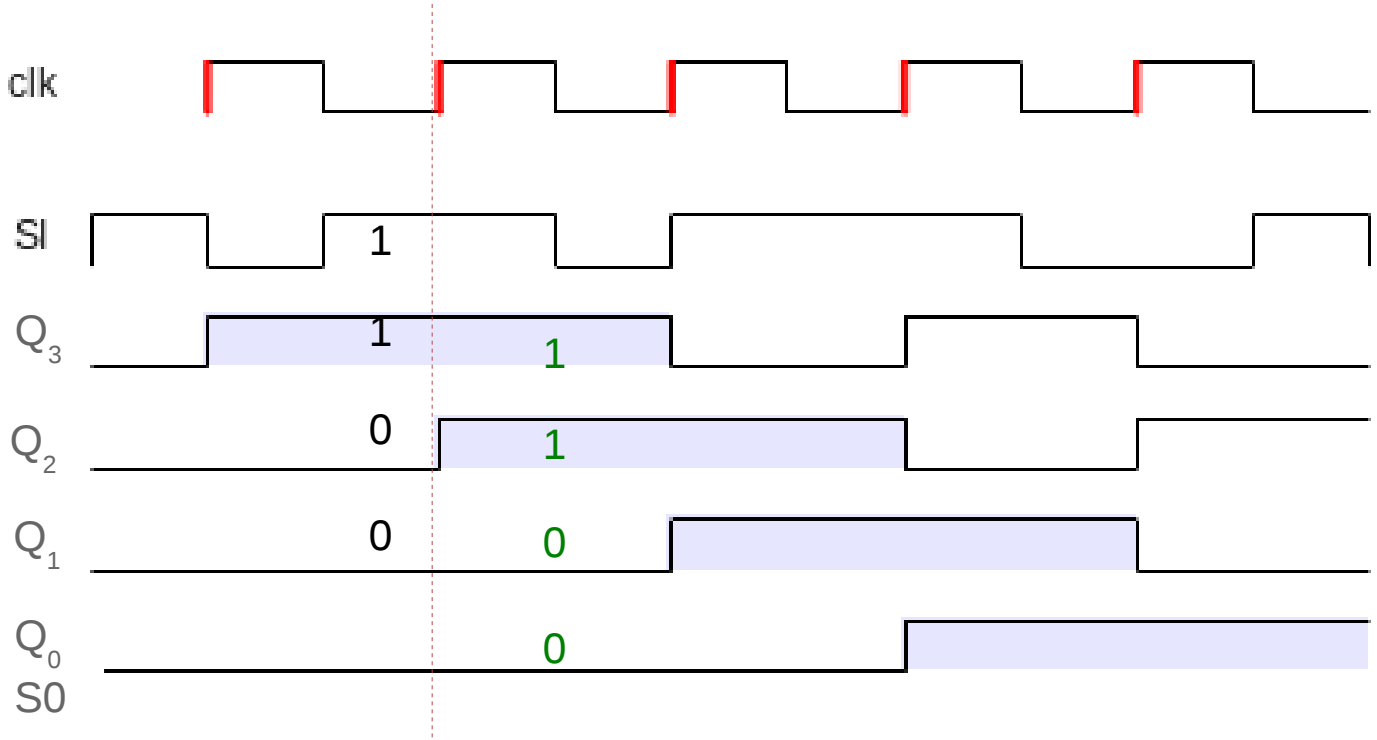
Connected in serial,
but parallel assignments



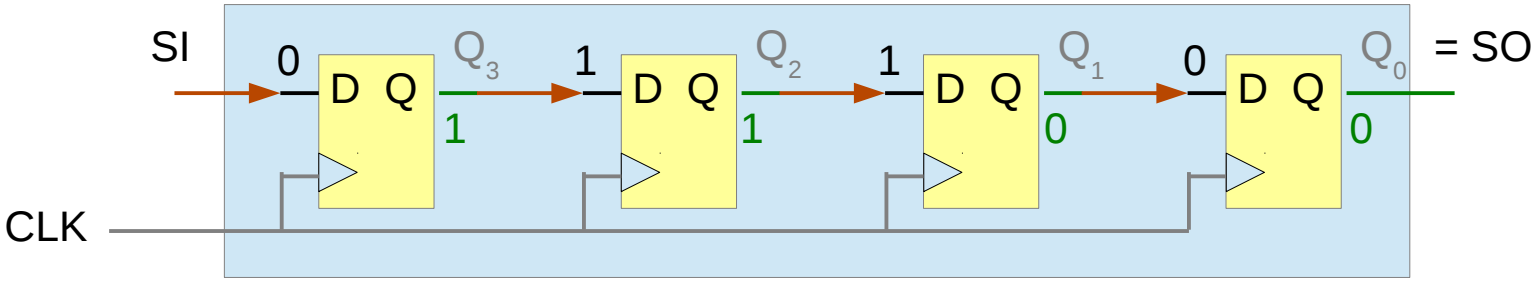
Shift Register Timing – Cycle 2



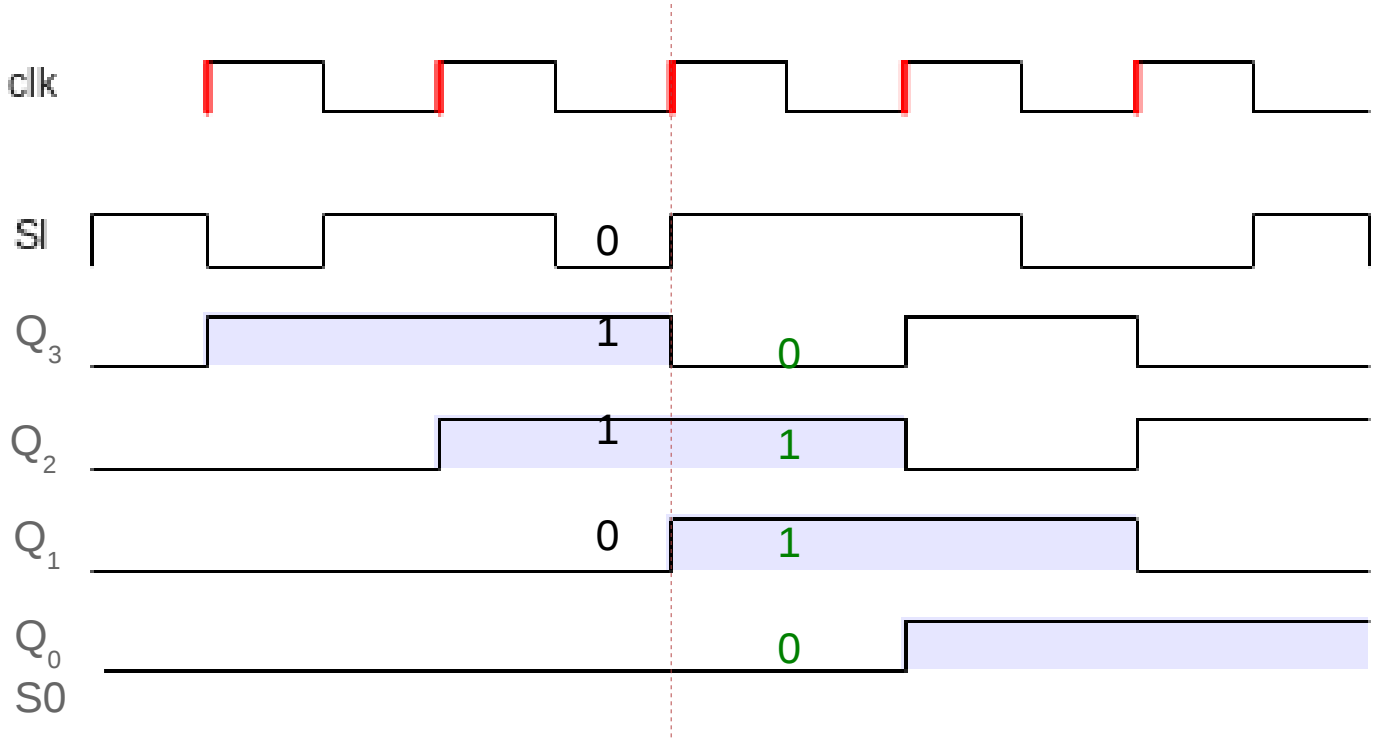
Connected in serial,
but parallel assignments



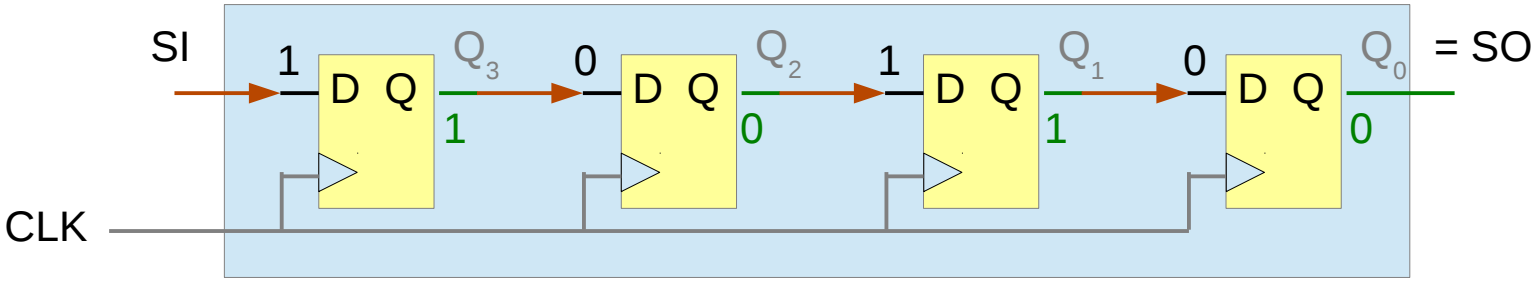
Shift Register Timing – Cycle 3



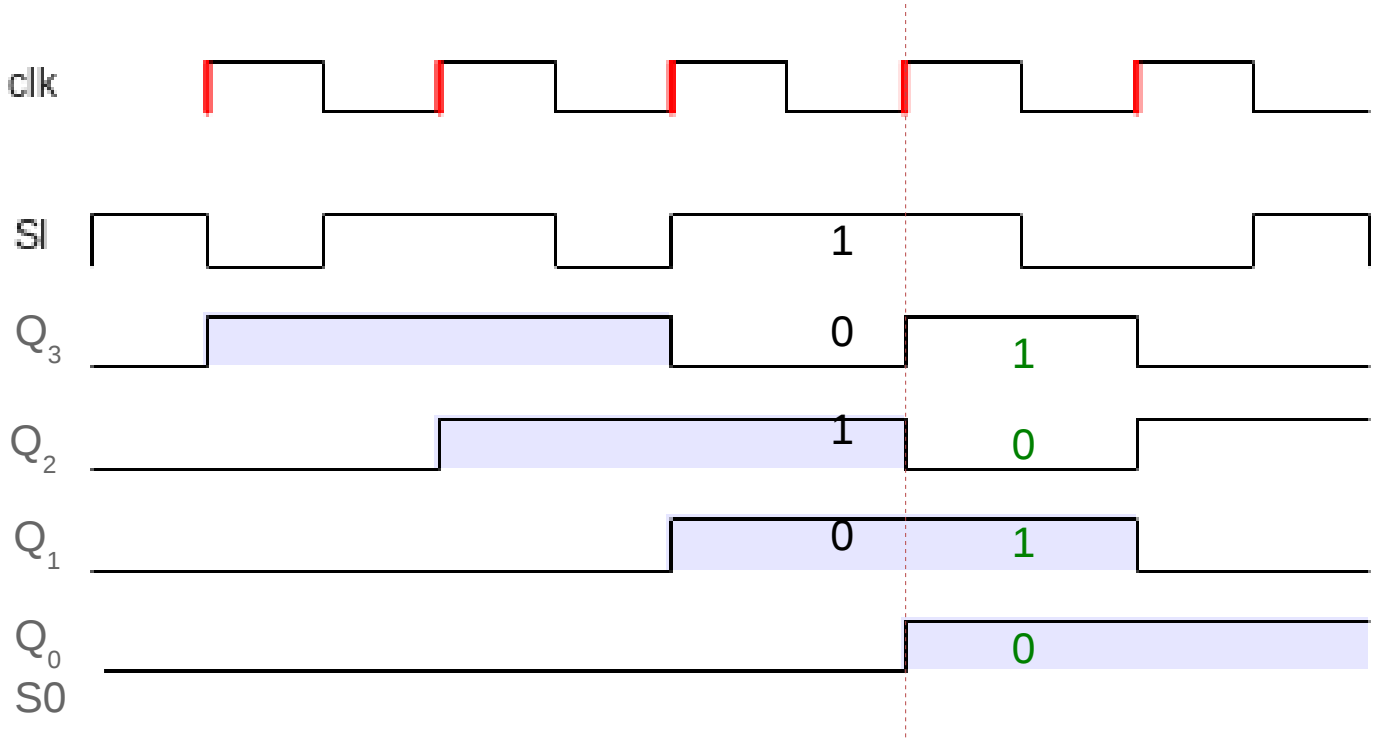
Connected in serial,
but parallel assignments



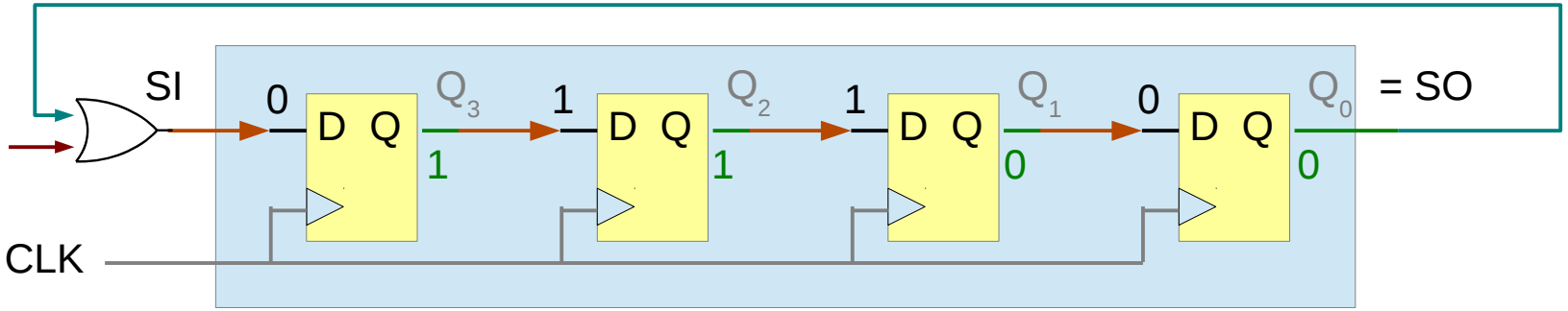
Shift Register Timing – Cycle 4



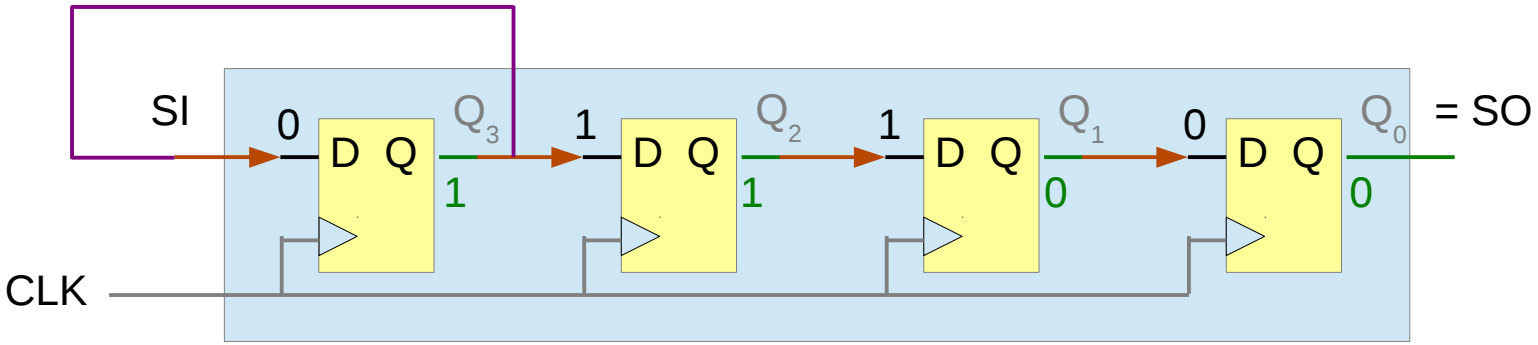
Connected in serial,
but parallel assignments



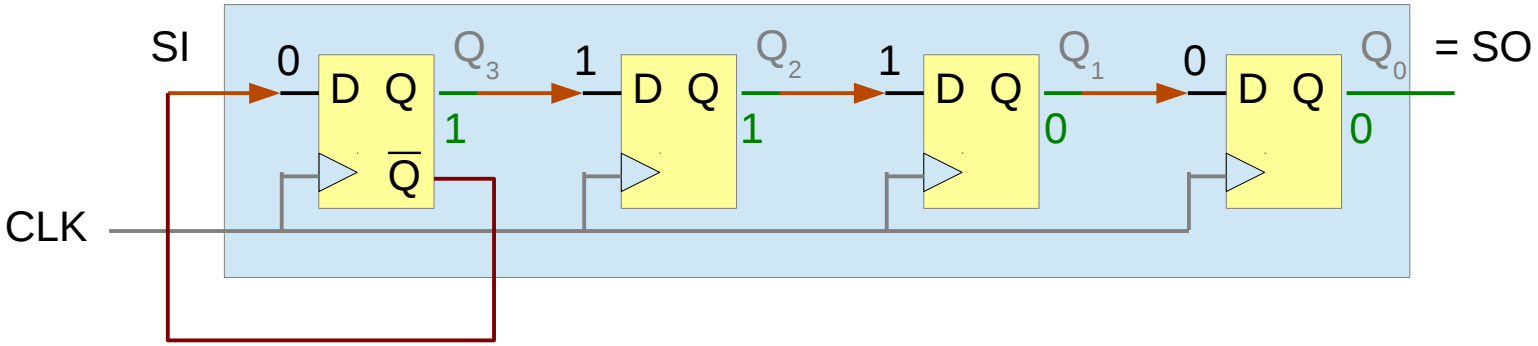
Rotate



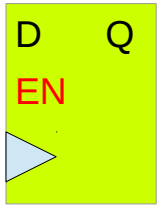
Divide By 2 with a Sign Extension

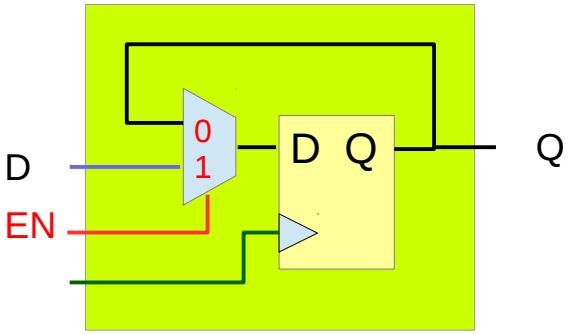


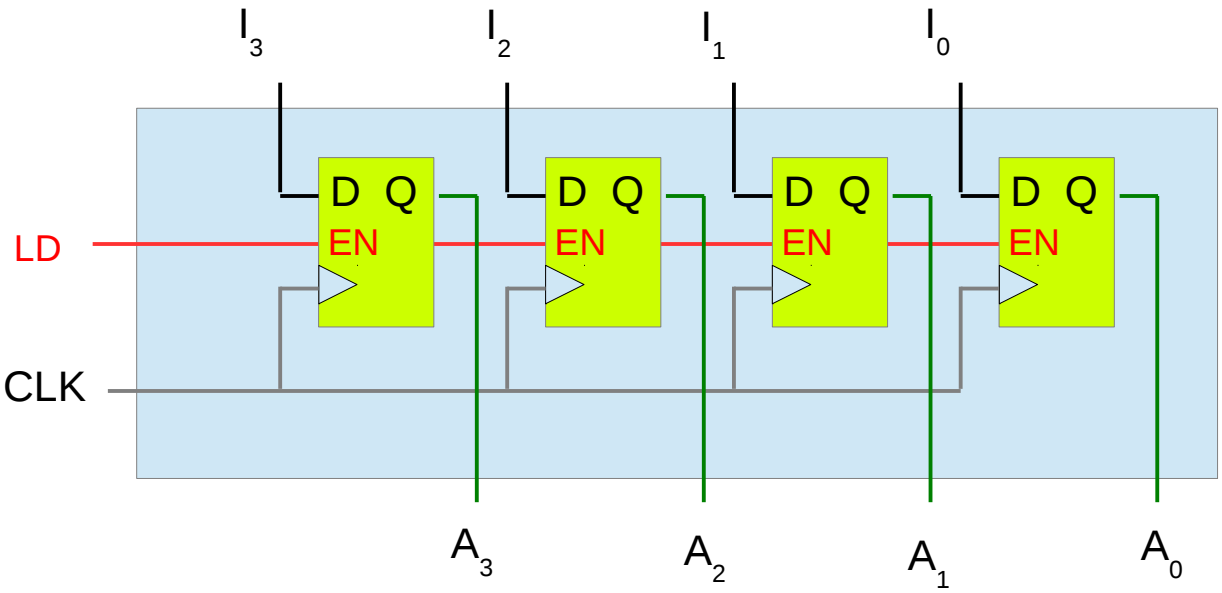
Toggling Input

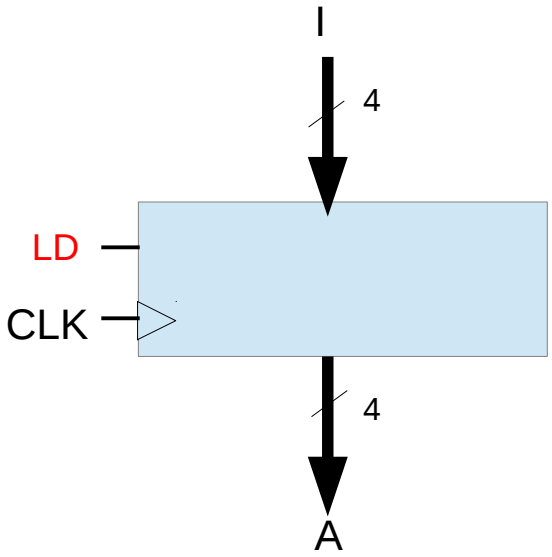


Register with Parallel Load

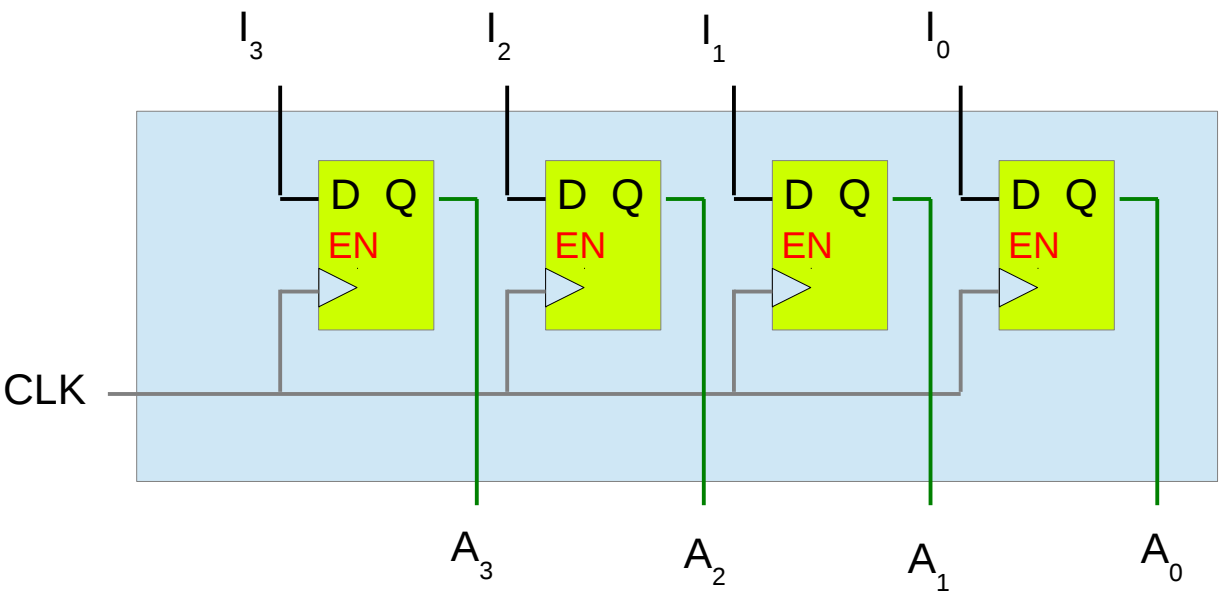


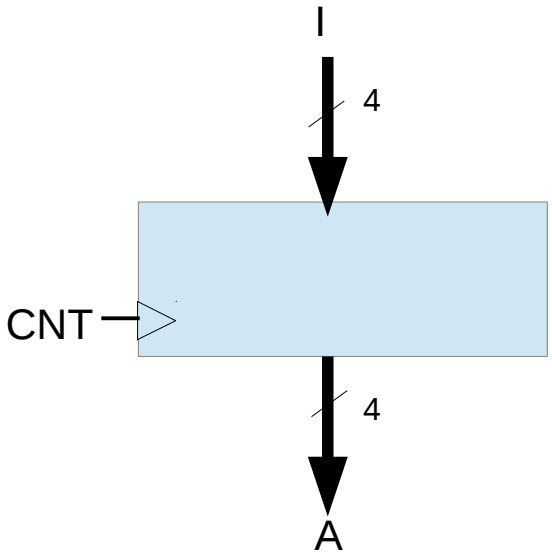




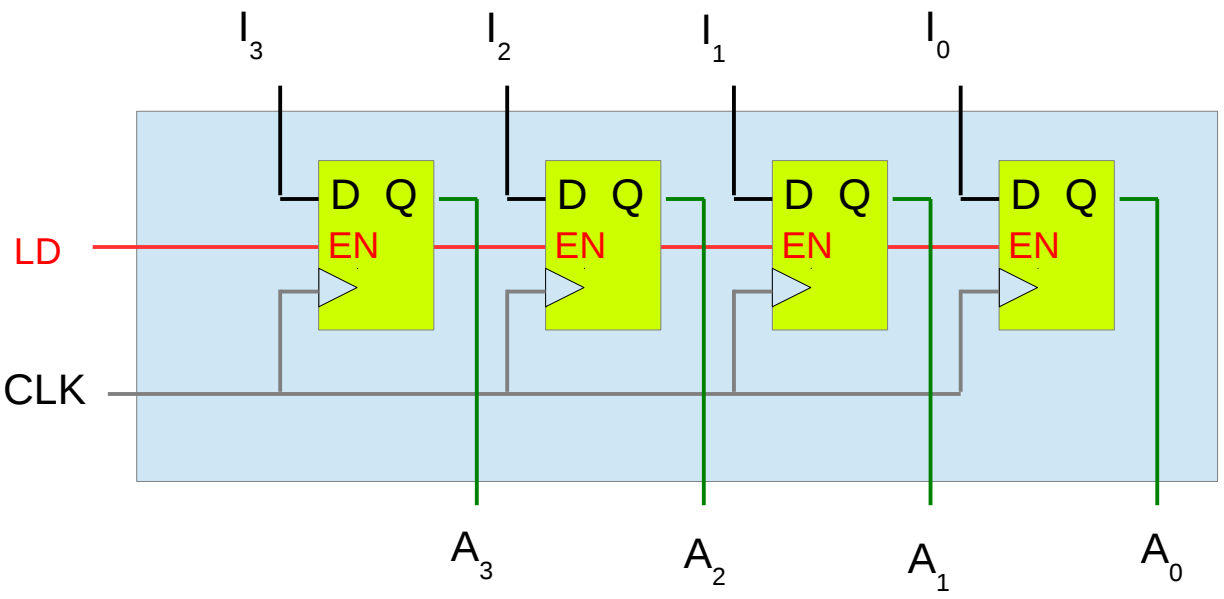


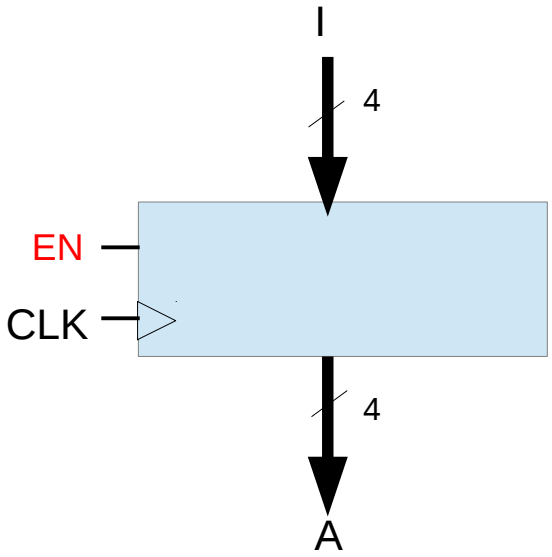
Ripple Counter





Synchronous Binary Counter





References

[1] http://en.wikipedia.org/
[2] M. M. Mano, C. R. Kime, “Logic and Computer Design Fundamentals”, 4th ed.
[3] D.M. Harris, S. L. Harris, “Digital Design and Computer Architecture”