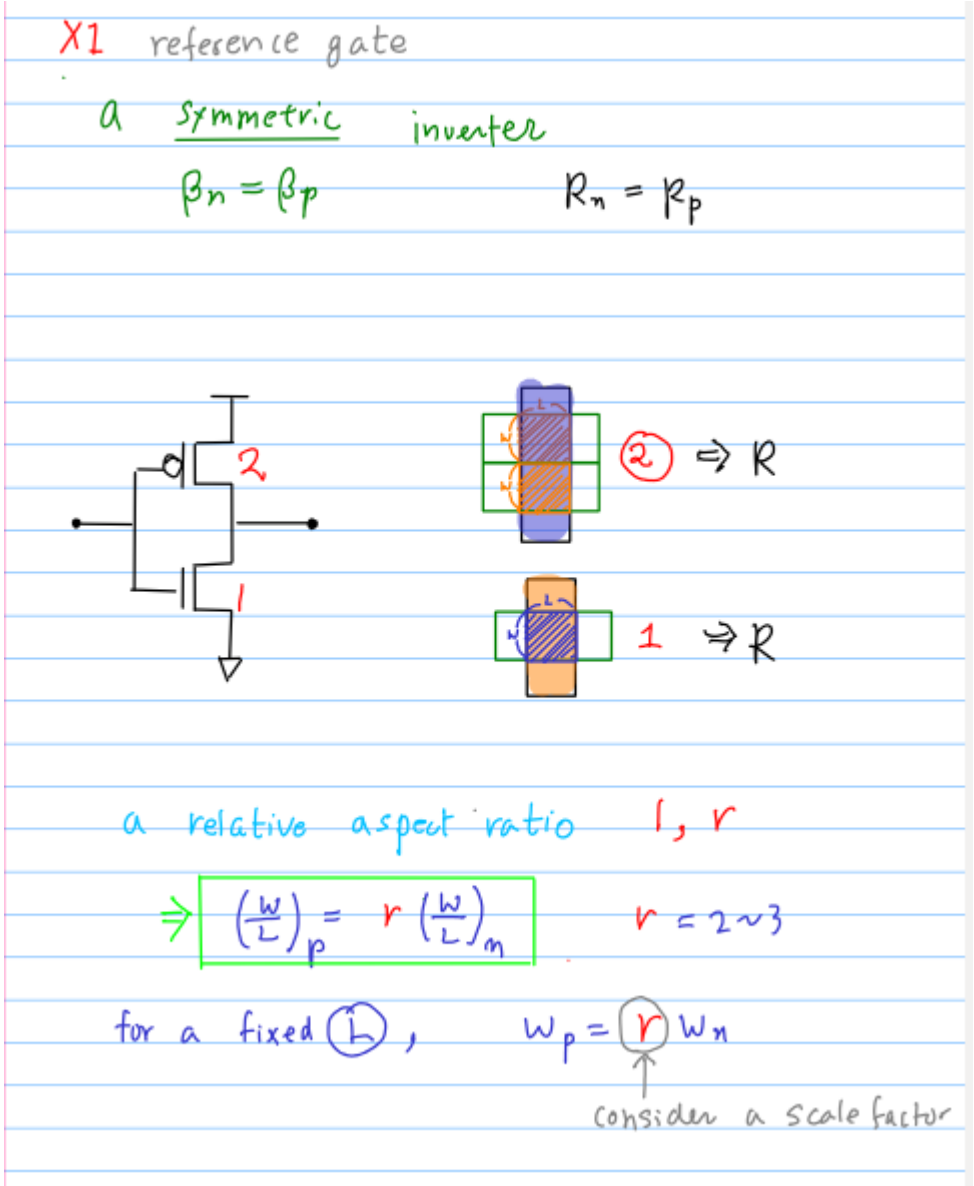
Gate Area

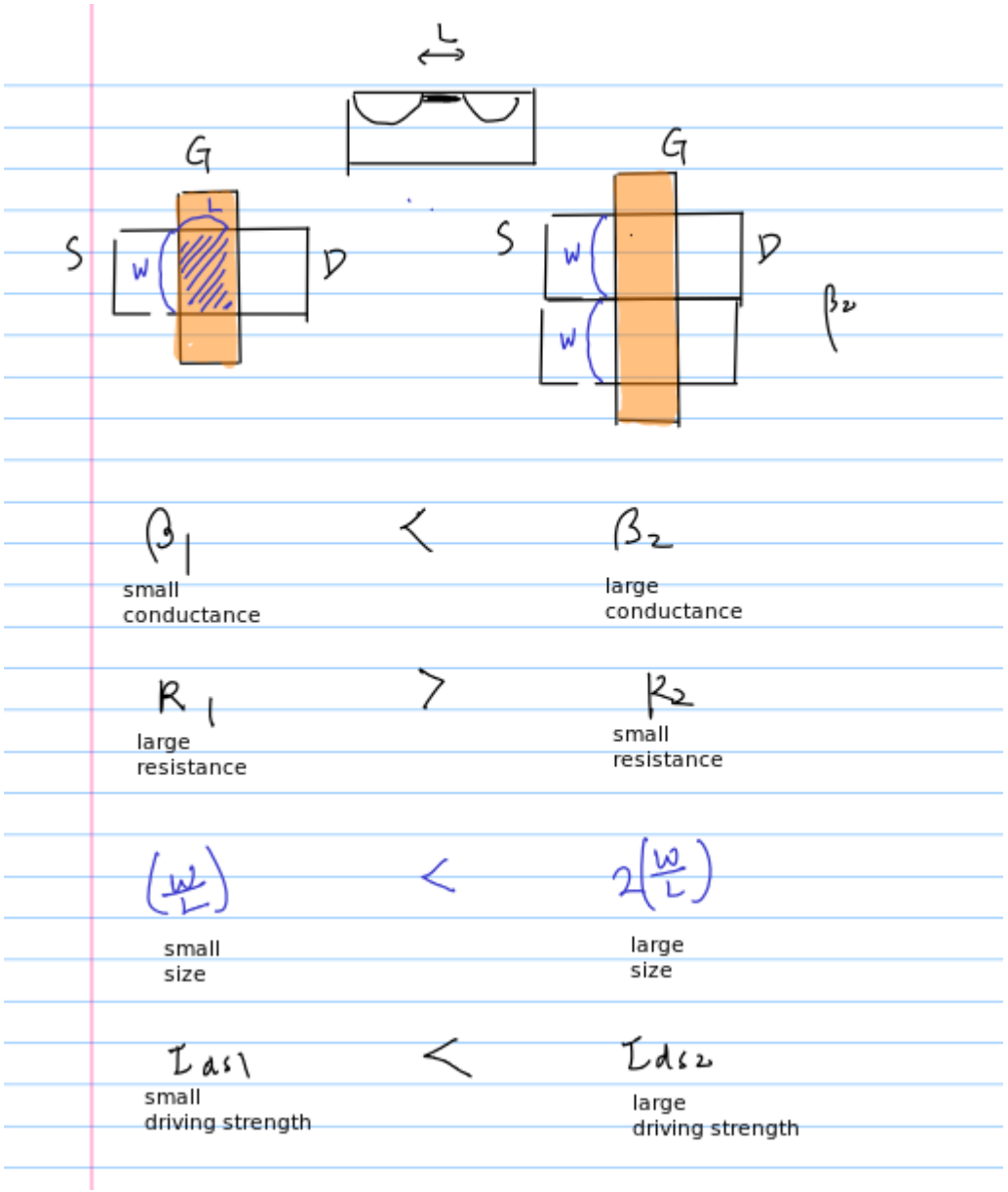
Please send corrections (or suggestions) to youngwlim@hotmail.com.

This document was produced by using OpenOffice and Octave.

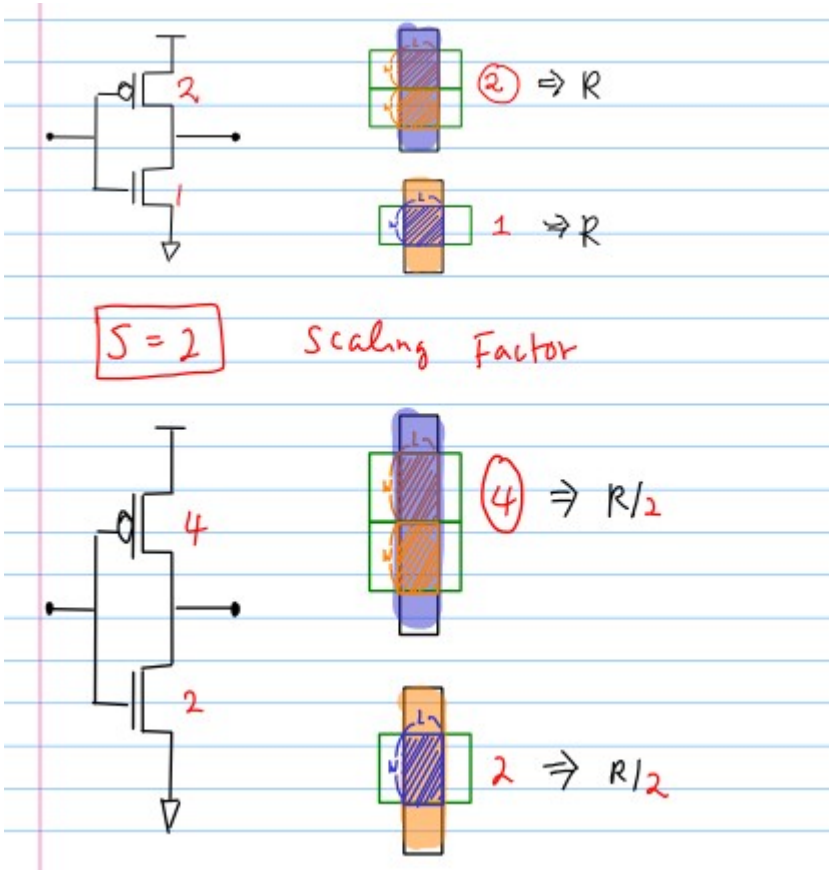
A Unit Inverter

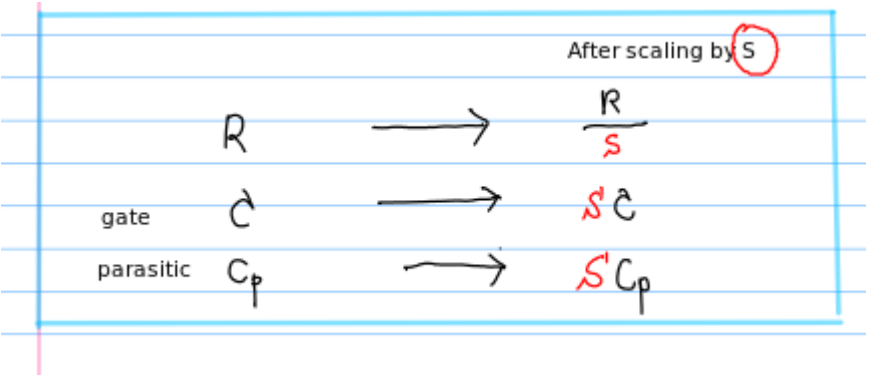


Aspect Ratio Related

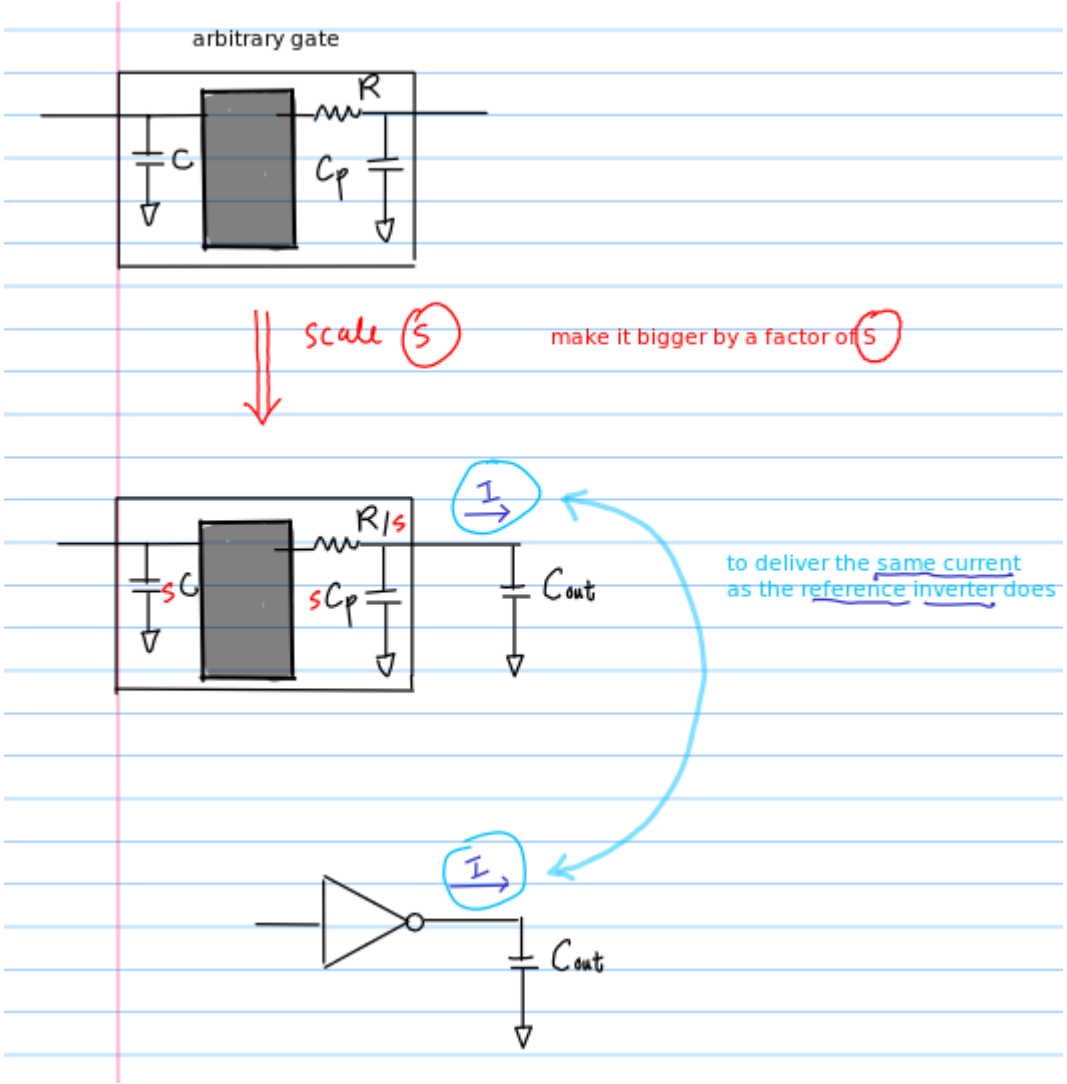


Scaling Factor

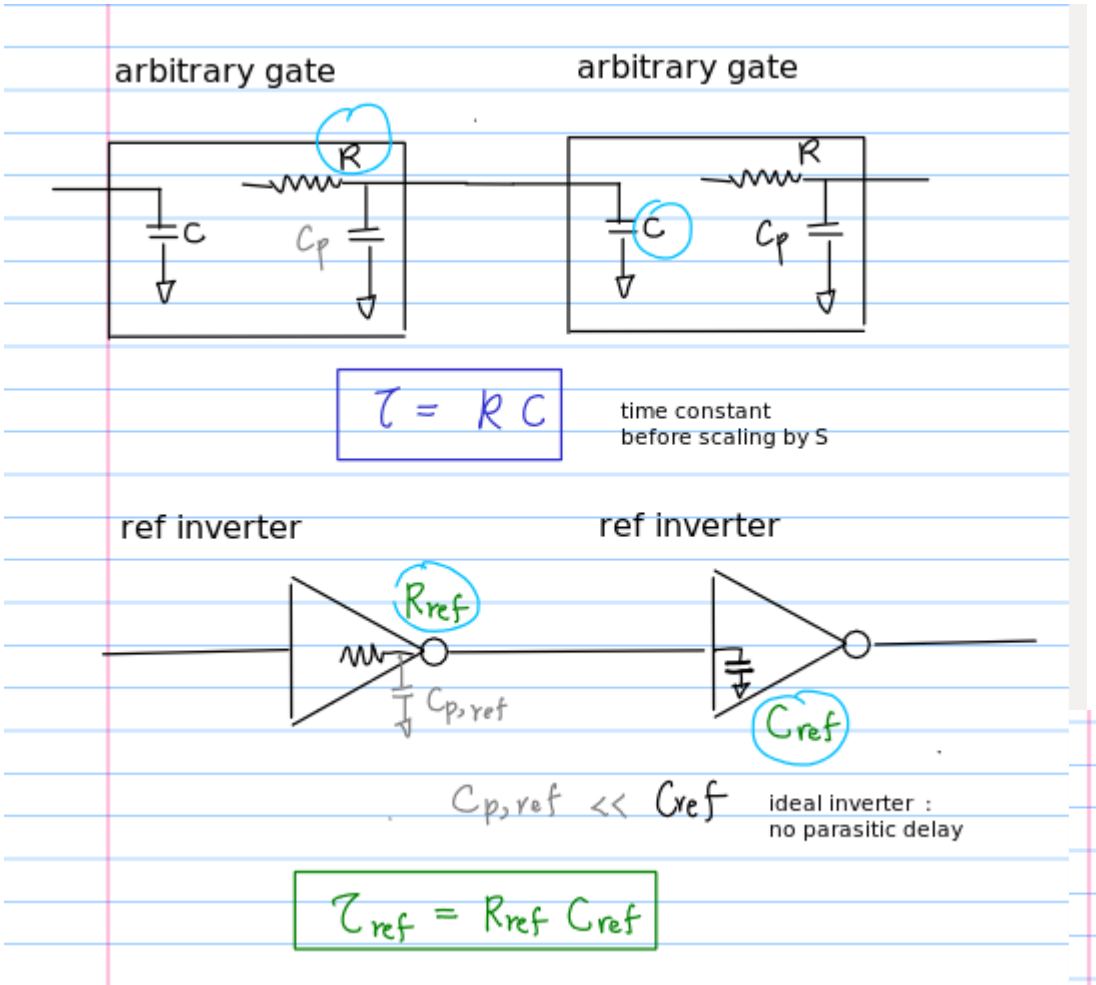




Scaling for the same output I



Time Constant



$$g \cdot h = \left(\frac{RC}{R_{ref} C_{ref}}\right)\left(\frac{C_{out}}{C_{in}}\right)$$

$$= \left(\frac{\tau}{\tau_{ref}}\right)\left(\frac{C_{out}}{C_{in}}\right)$$

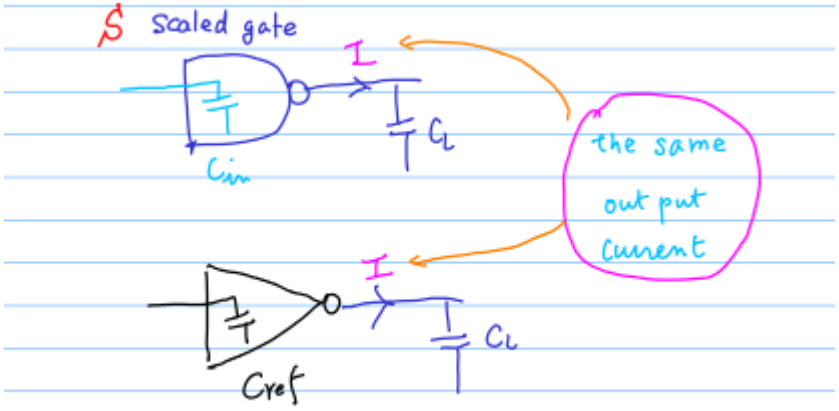
Logical Effort

Logical effort (g) of a gate

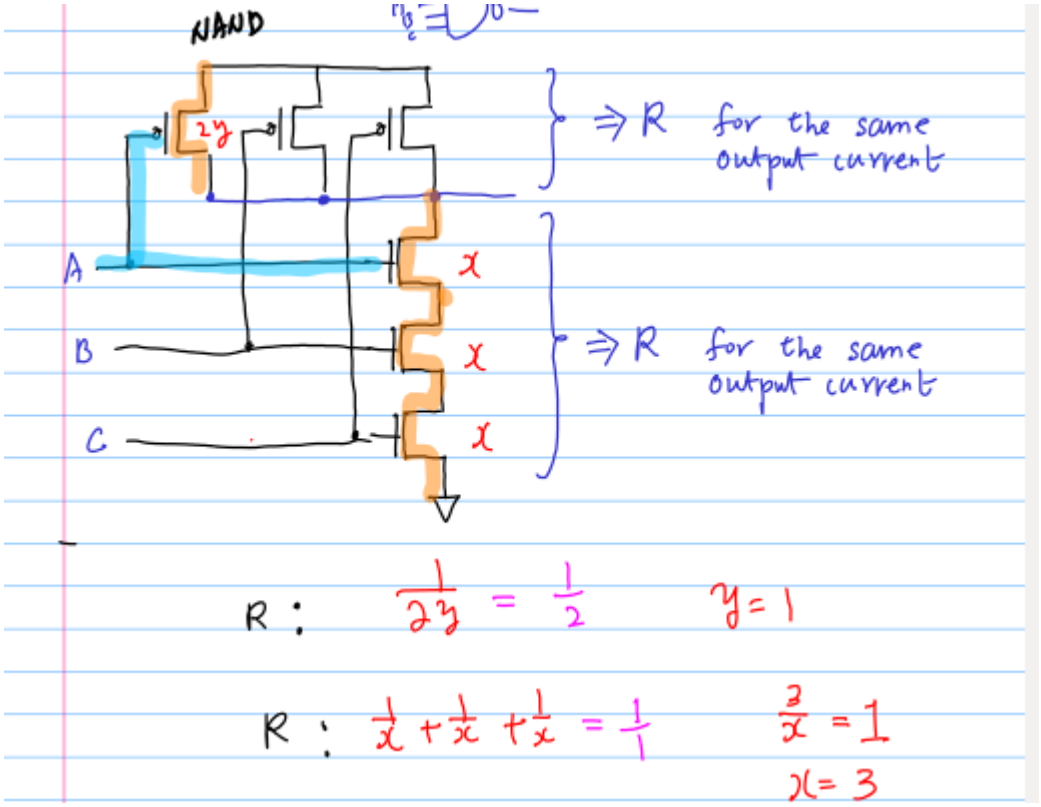
the ratio of
the input capacitance of the gate to
the input capacitance of an inverter
that can give the same output current

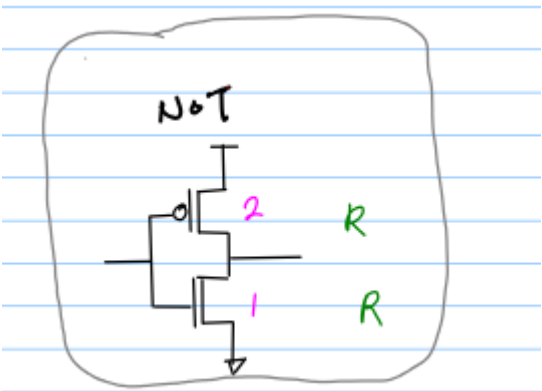
$$g = \frac{C_{in}}{C_{ref}}$$

C_{in} after scaling
in order to make its output current
the same as reference gate's output current

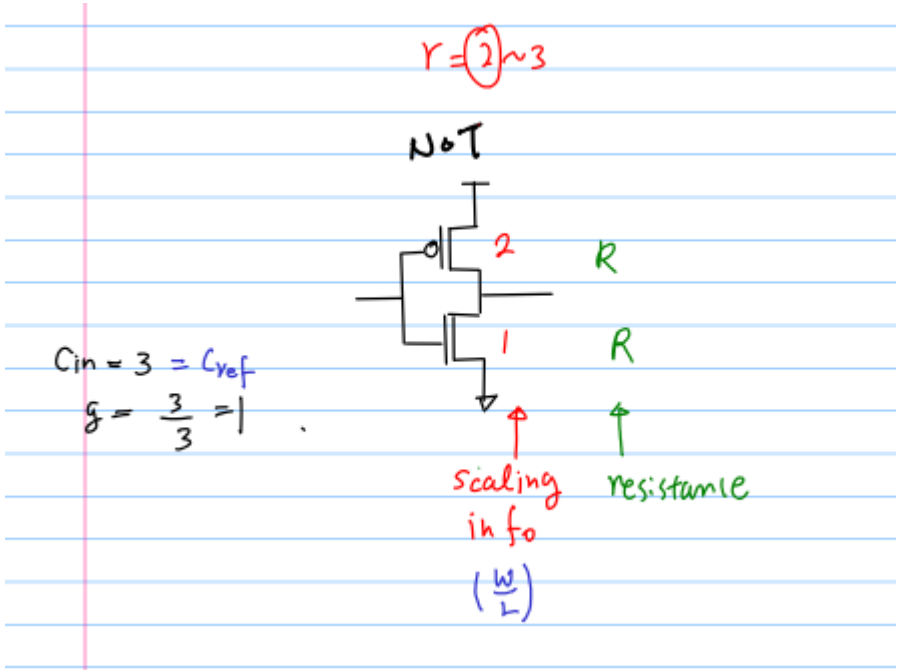


Example

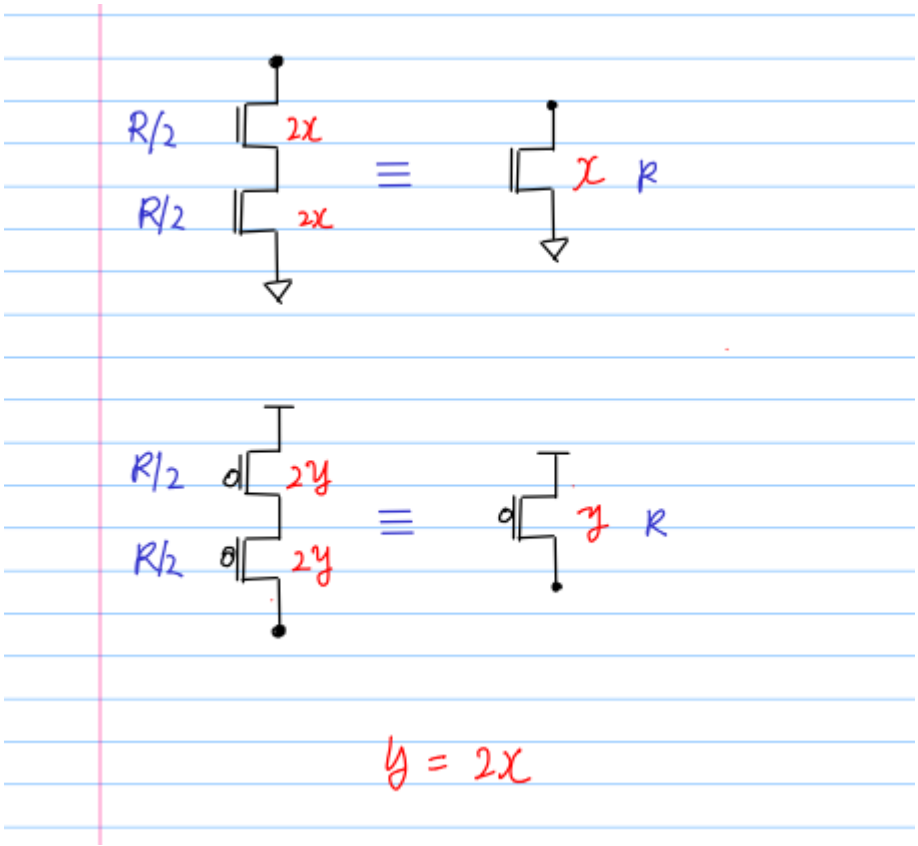

NAND
2y
A
B
C
x
x
x
⇒ R for the same output current
⇒ R for the same output current
R : 1/2y = 1/2 y = 1
R : 1/x + 1/x + 1/x = 1/1 3/x = 1
x = 3


NOT
2
R
1
R

Example



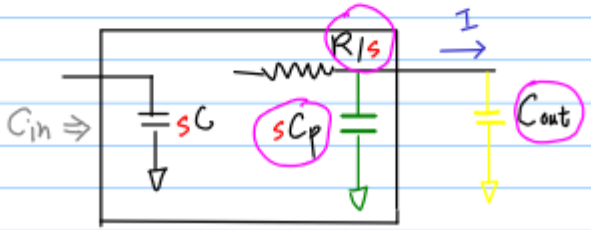
Summary



Parasitic Delay

parasitic delay (p)

- delay due to internal parasitic capacitance sC_p
- excluding external load cap C_{out}
- count only diffusion capacitance of the output

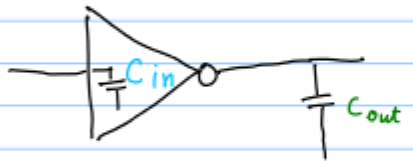


Electrical Effort

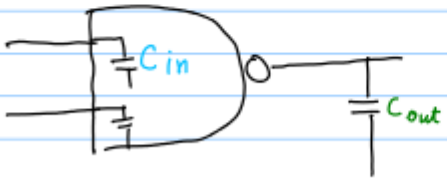
Electrical Effort : the capacitance ratio

$$h = \frac{C_{out}}{C_{in}}$$

the ratio of the drive strength to drive C_{out}
to the drive strength to drive its own capacitence C_{in}



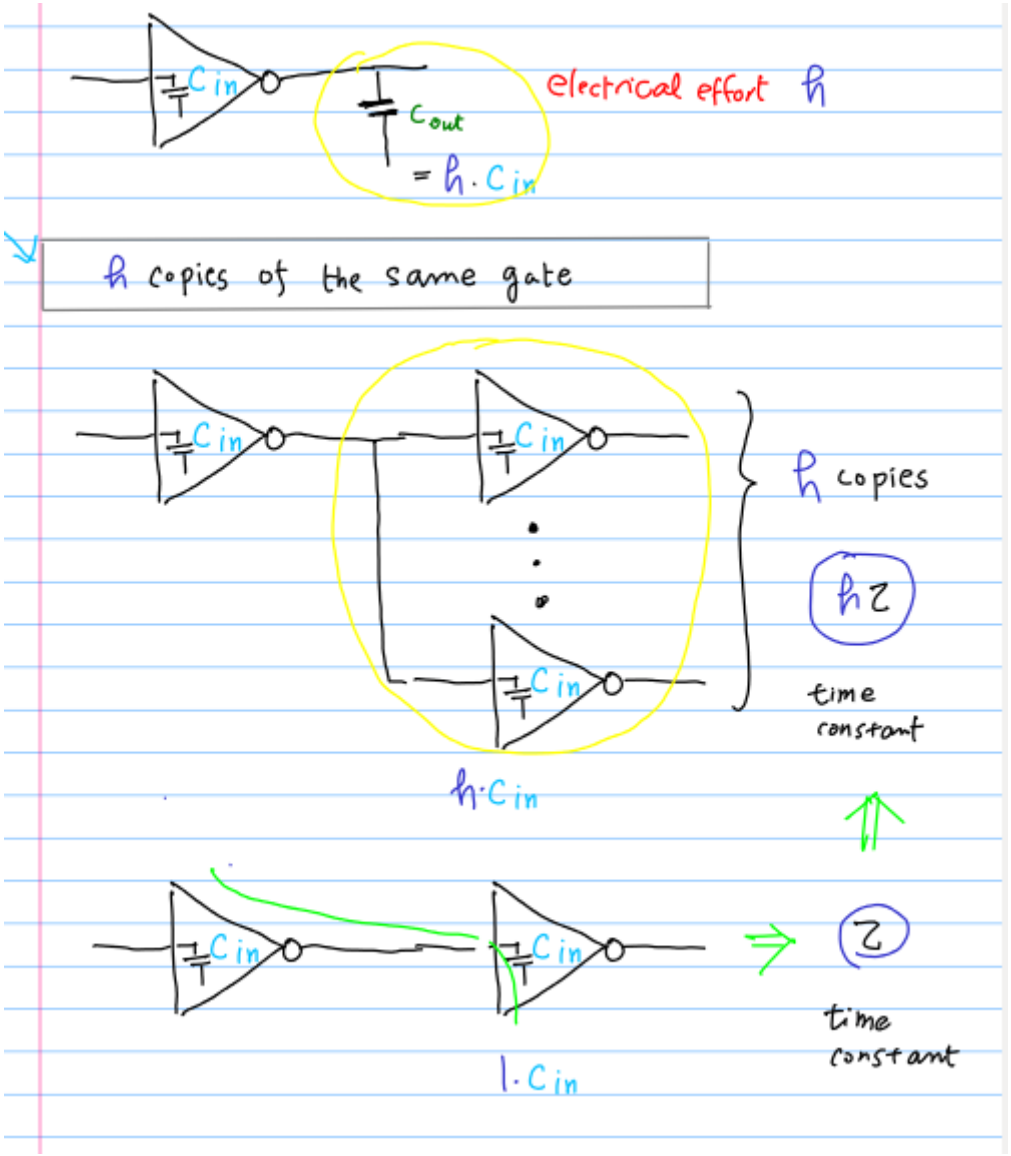
an inverter
is driving C_{out}



a NAND
is driving C_{out}

C_{out} is h times larger than C_{in}

Electrical Effort



References

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[5] J. P. Uyemura, “Introduction to VLSI Circuits and Systems”
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[10] https://en.wikiversity.org/wiki/The_necessities_in_Computer_Organization