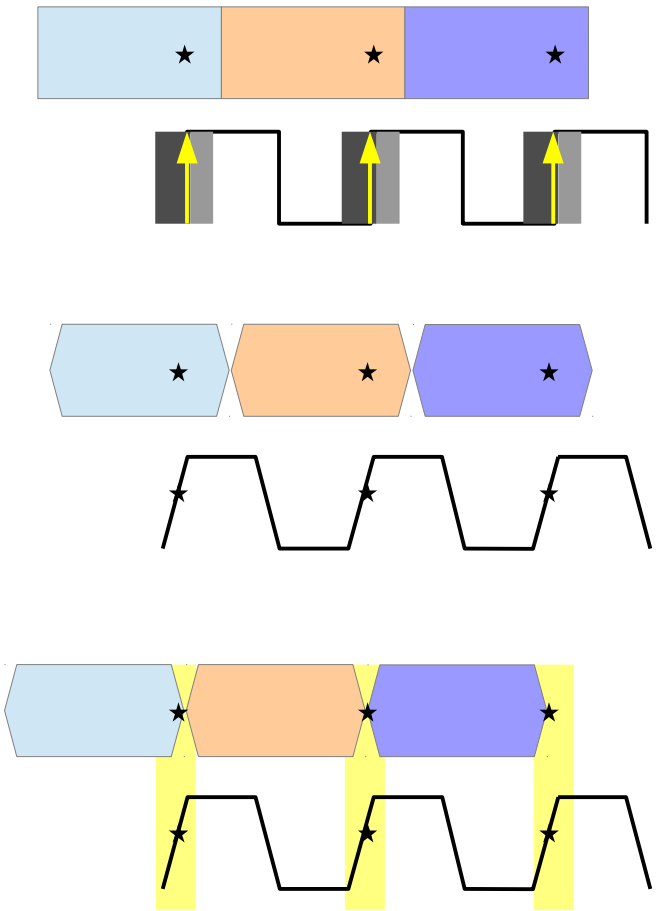
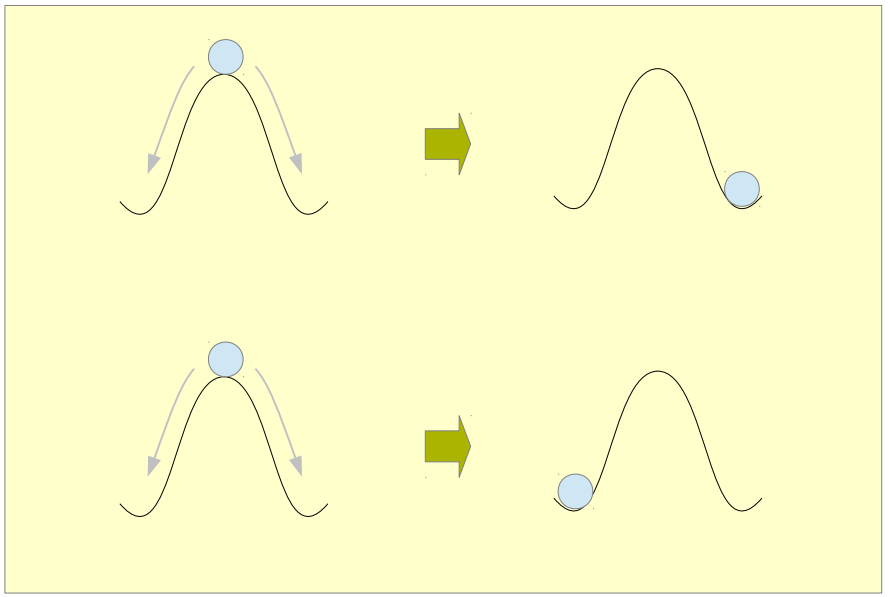
Gate Delay (3D)

Please send corrections (or suggestions) to youngwlim@hotmail.com.

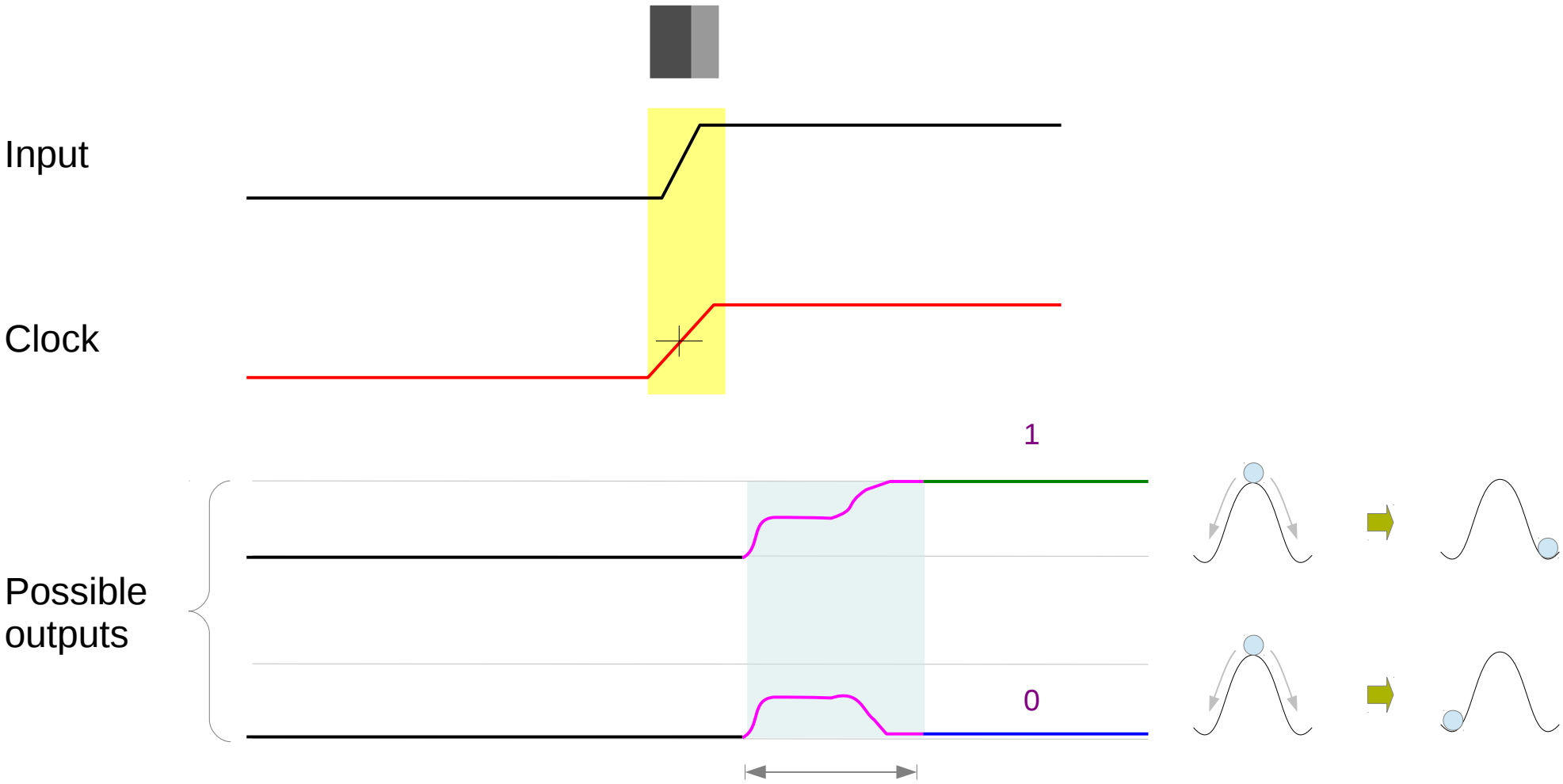
This document was produced by using OpenOffice and Octave.

Metastability

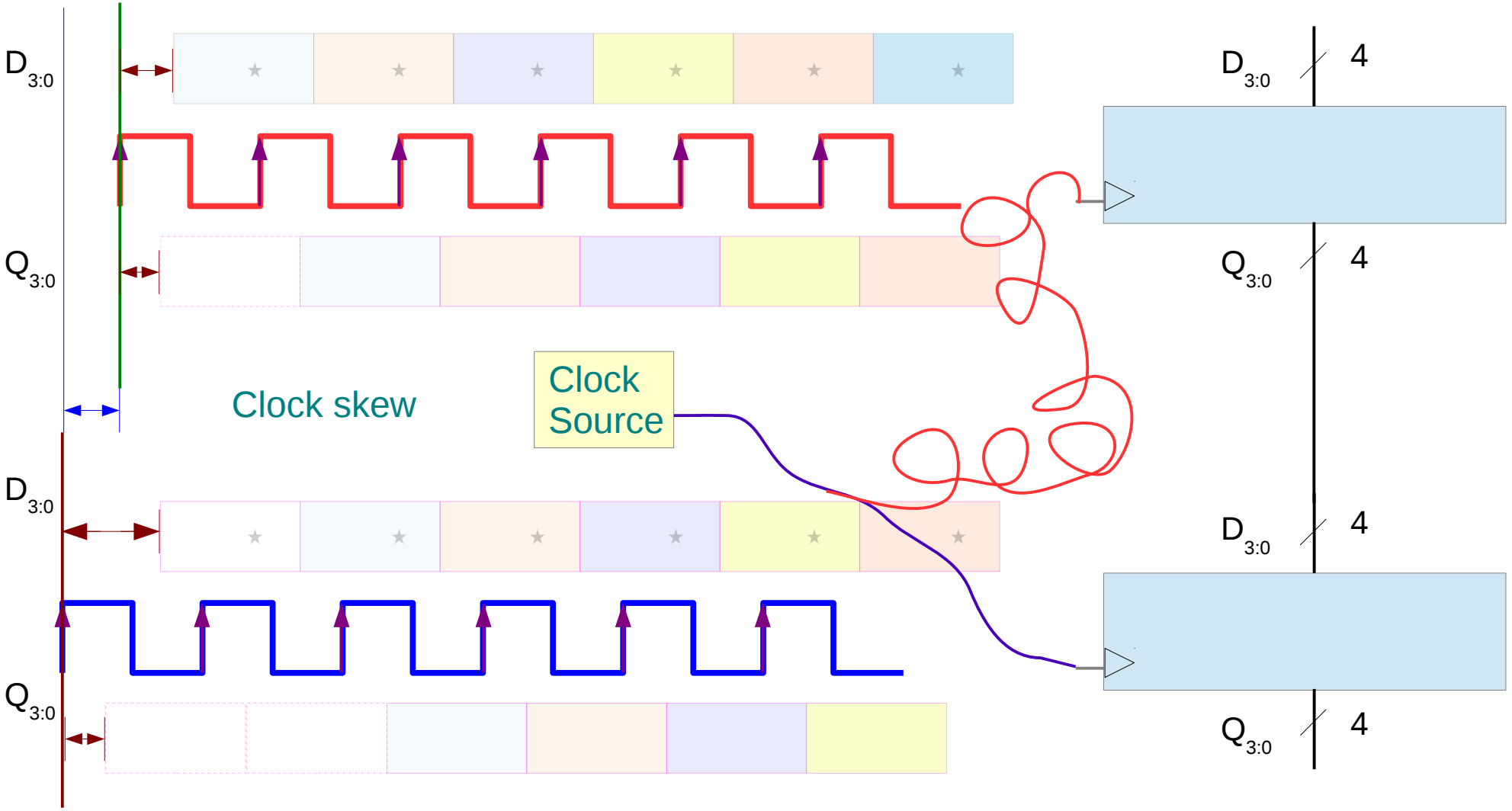




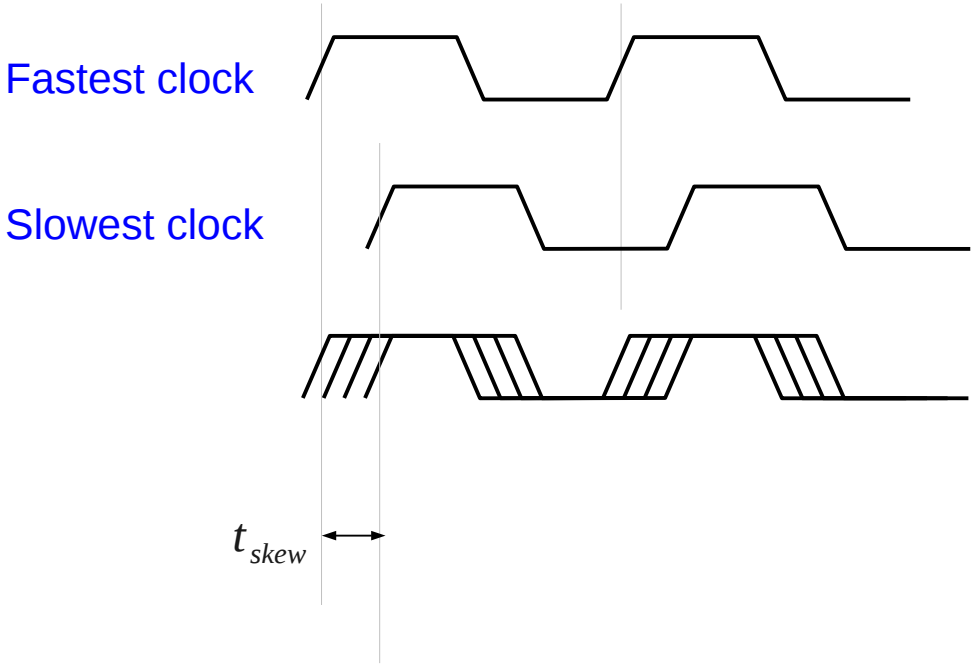
Possible Metastable Outputs

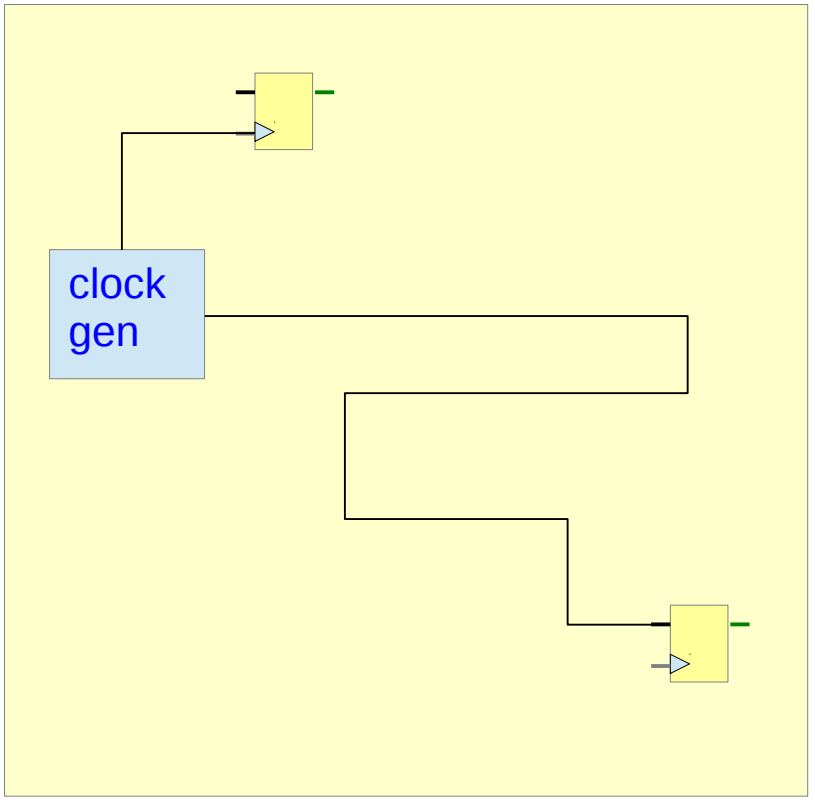


Clock Skew

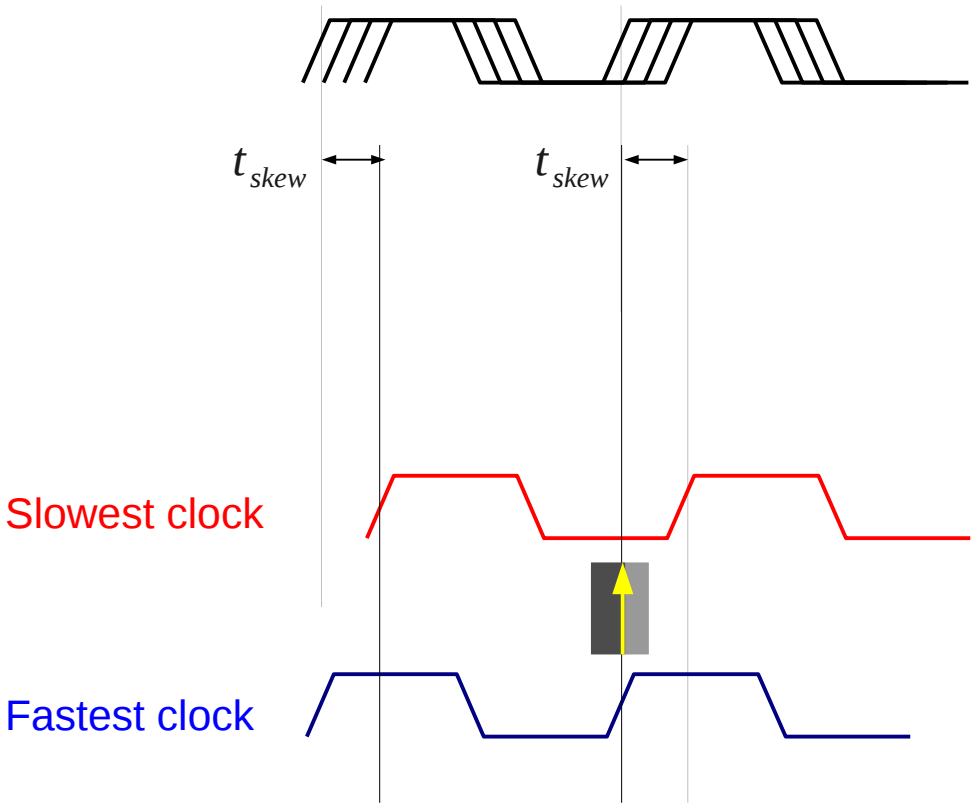


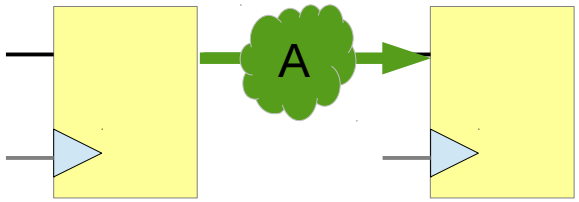
Clock Skew





Setup Time with Clock Skew

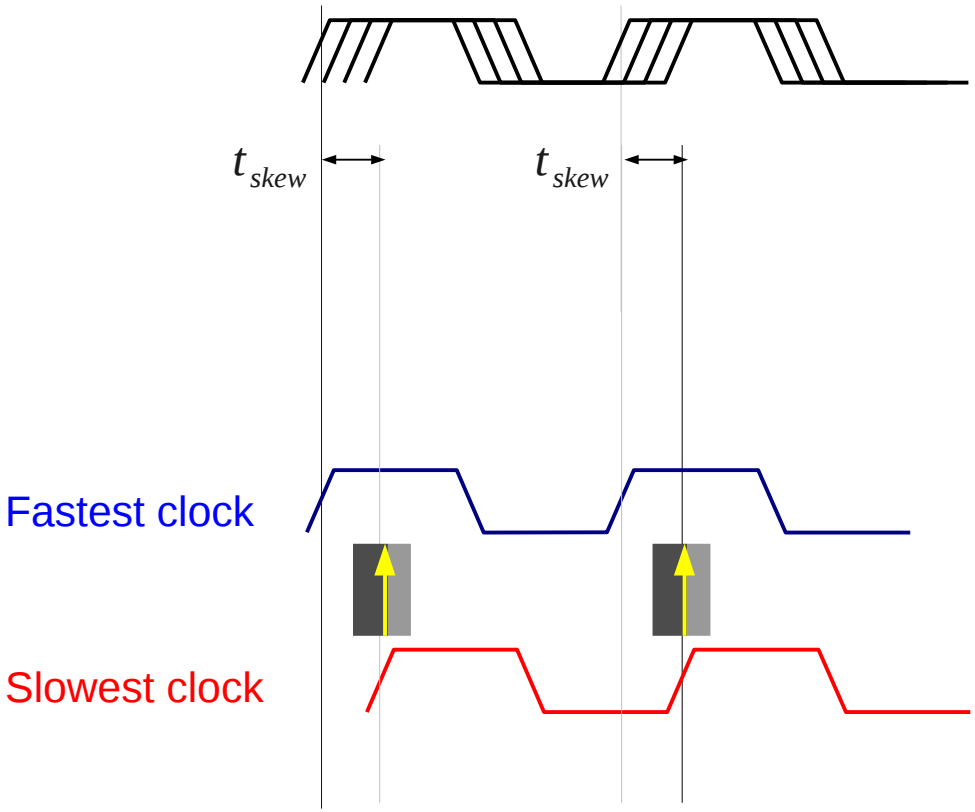


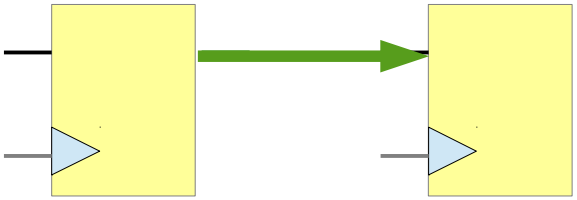


Slowest clock

Fastest clock

Hold Time with Clock Skew

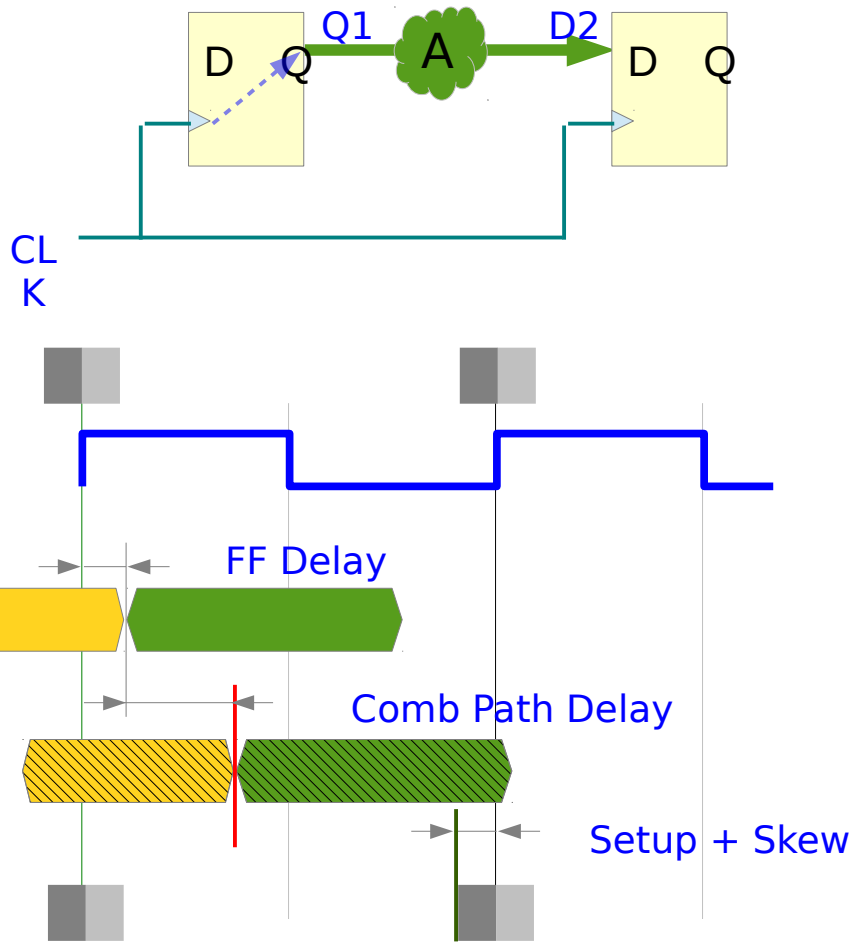




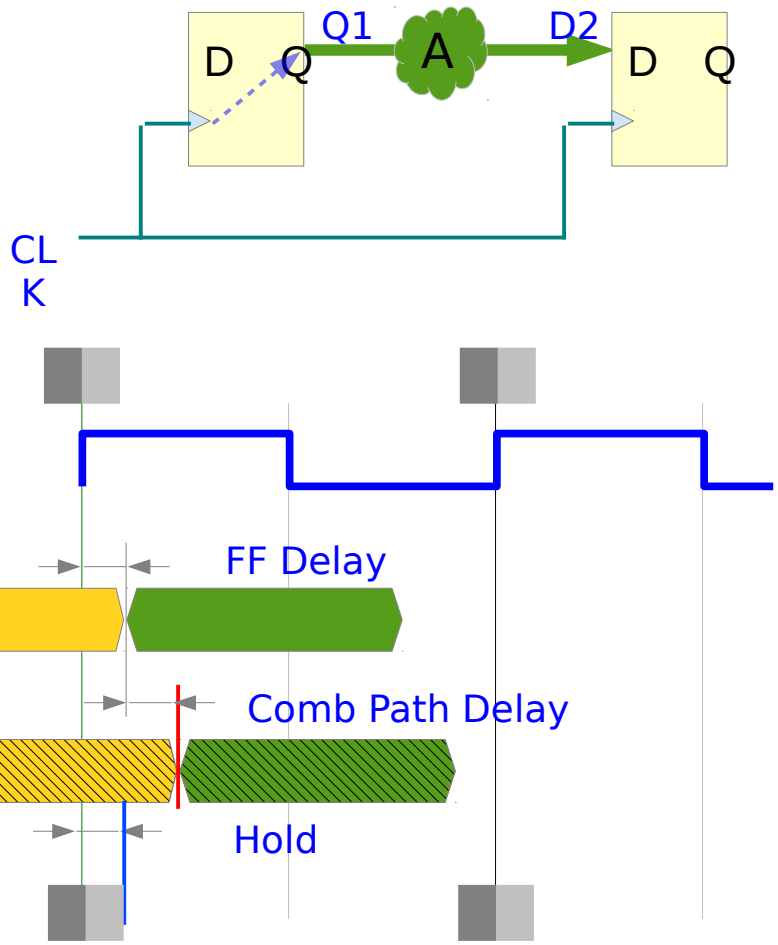
Fastest clock

Slowest clock

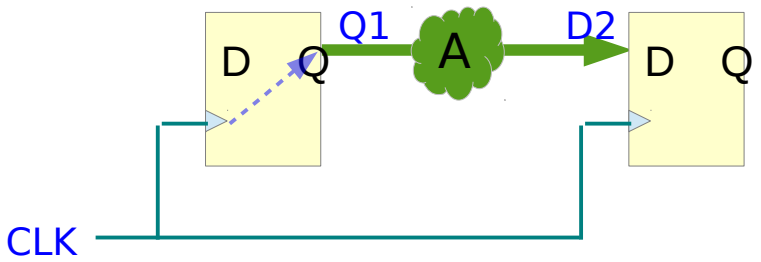
Setup Time



Hold Time



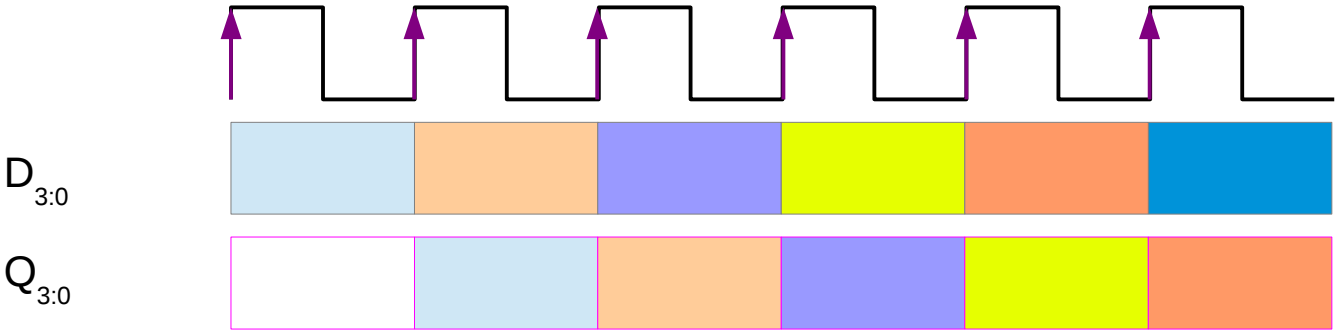
Hold Time

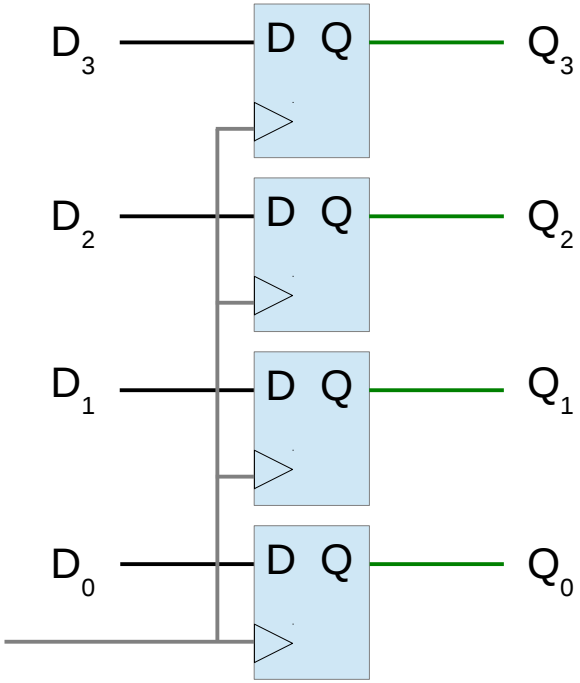


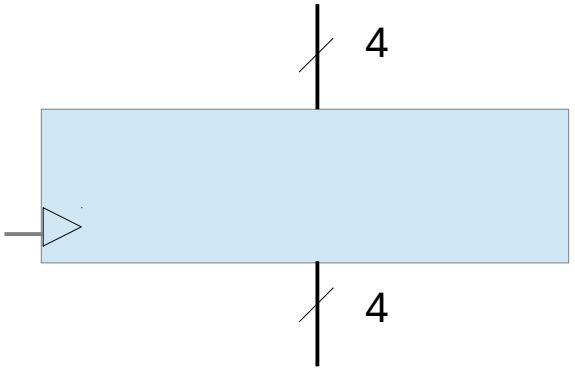
Gate Delay

Fan out
Path Delay
Max-Path
Min-Path
Clock
Setup & Hold Time
Metastability
Synchronizer

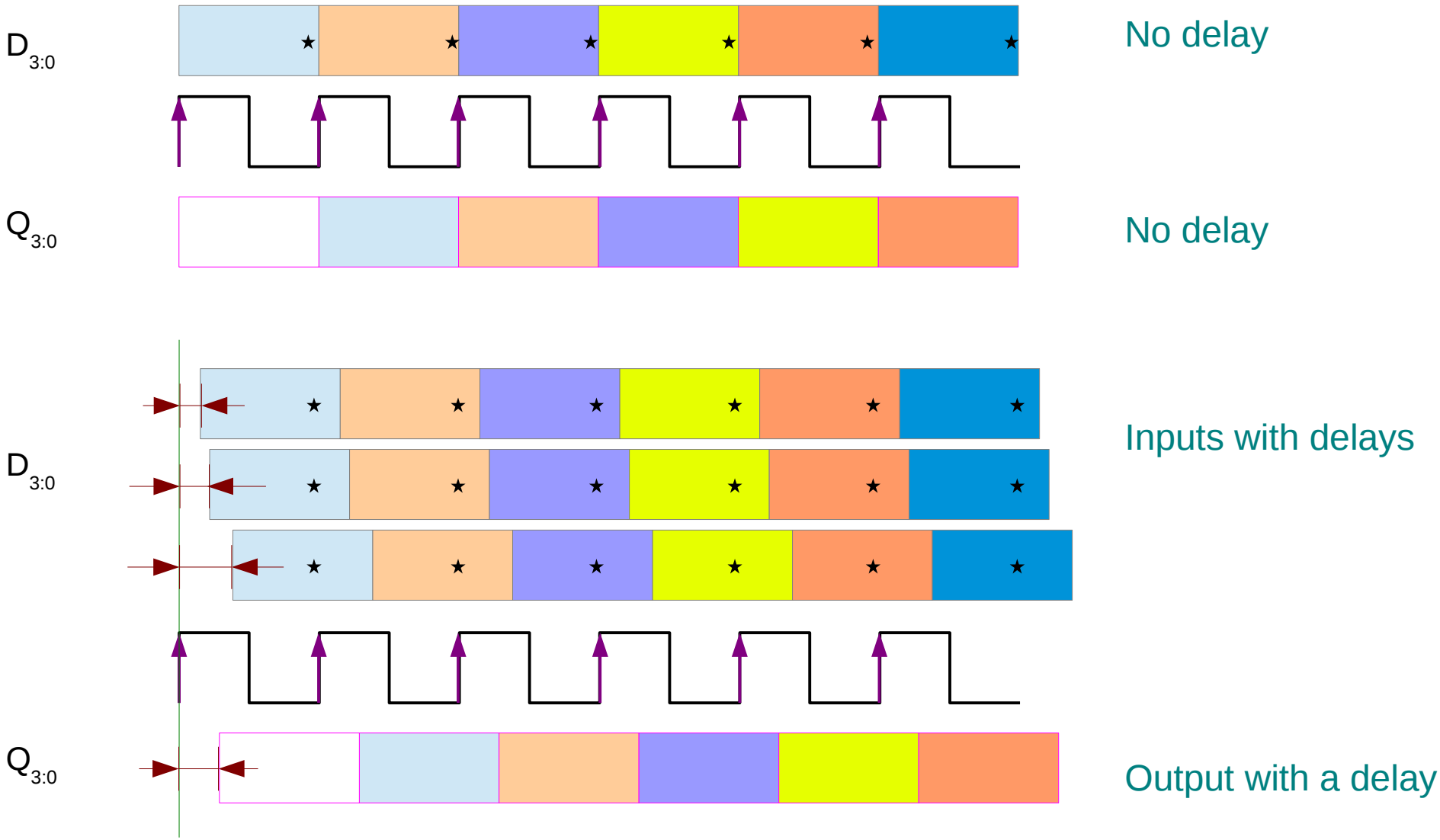
FF Timing (Ideal)



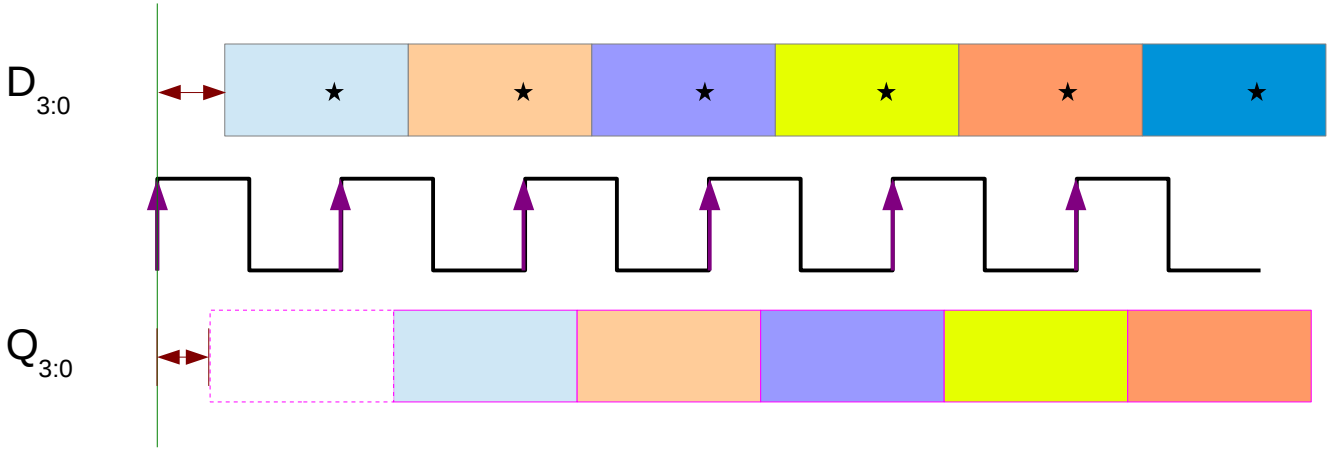


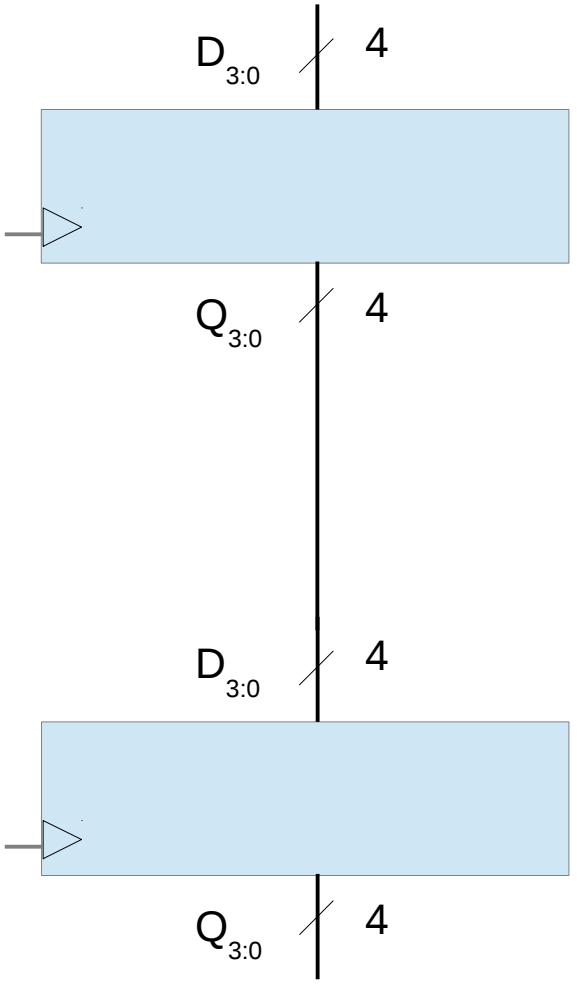


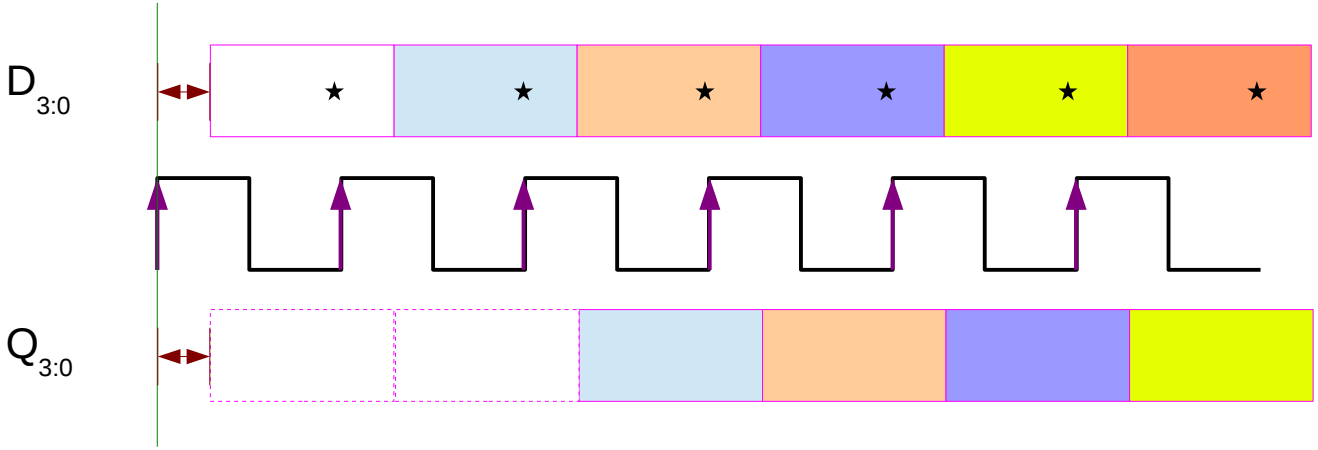
FF Timing (Delay)



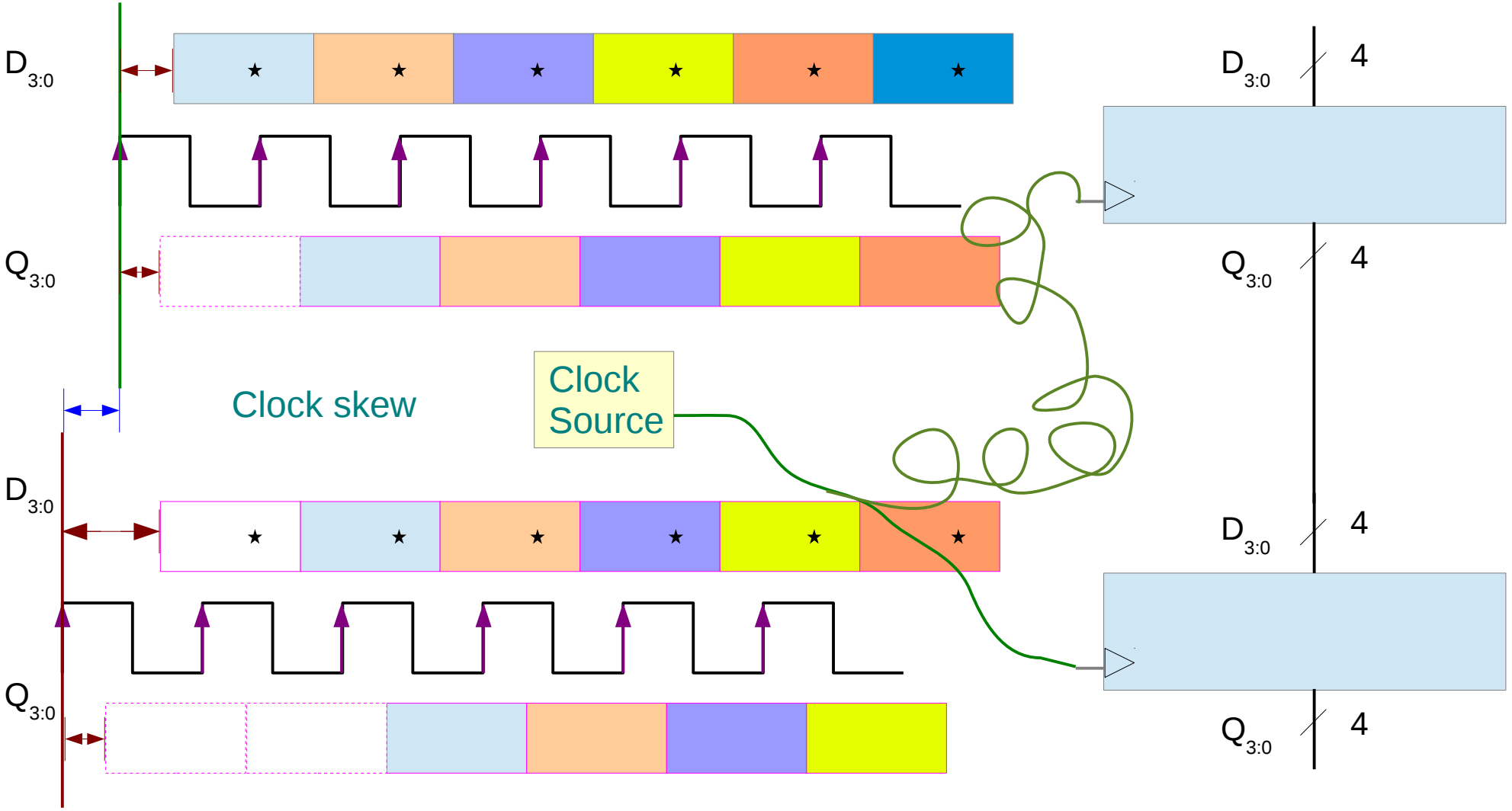
FF Timing (Delay)



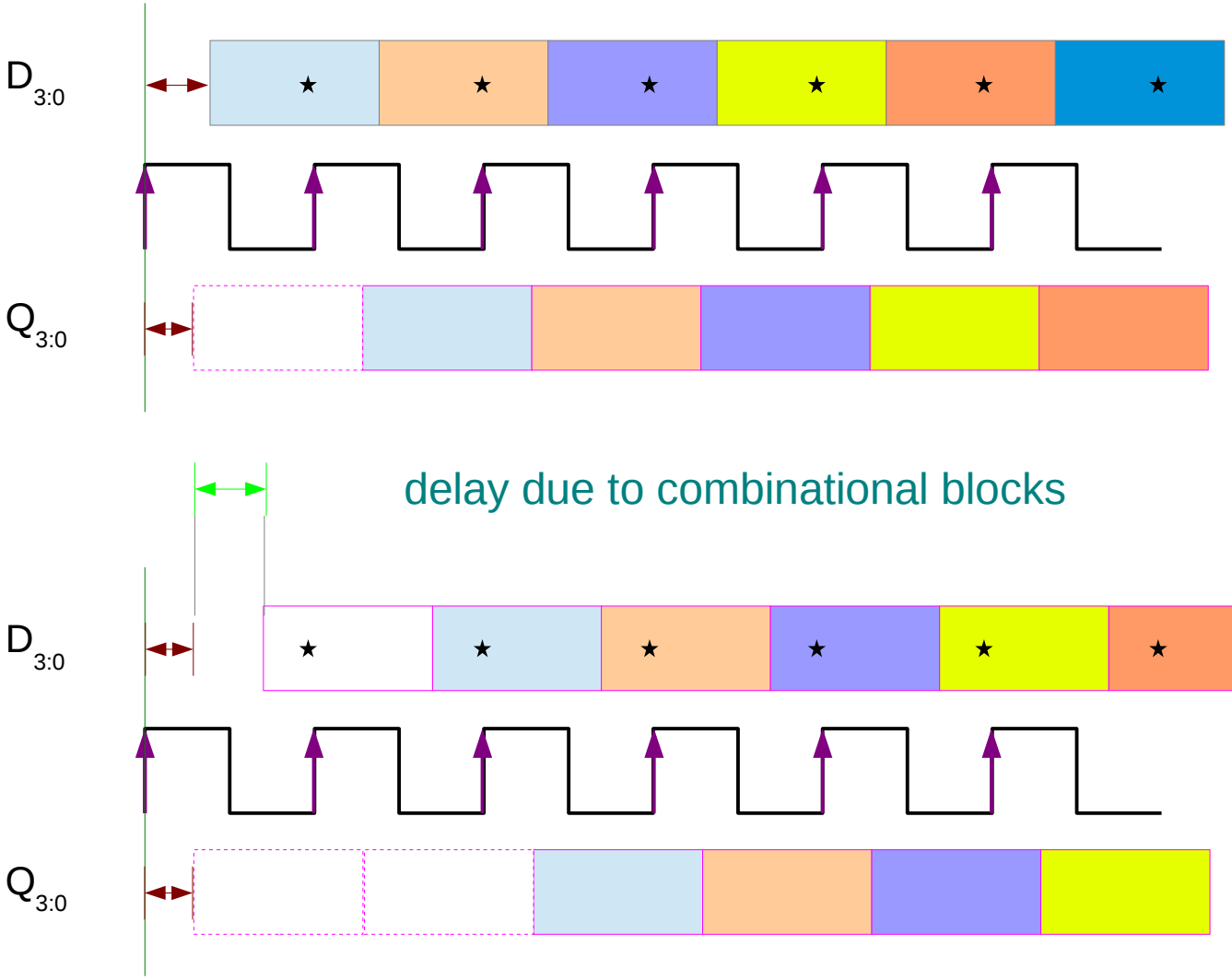


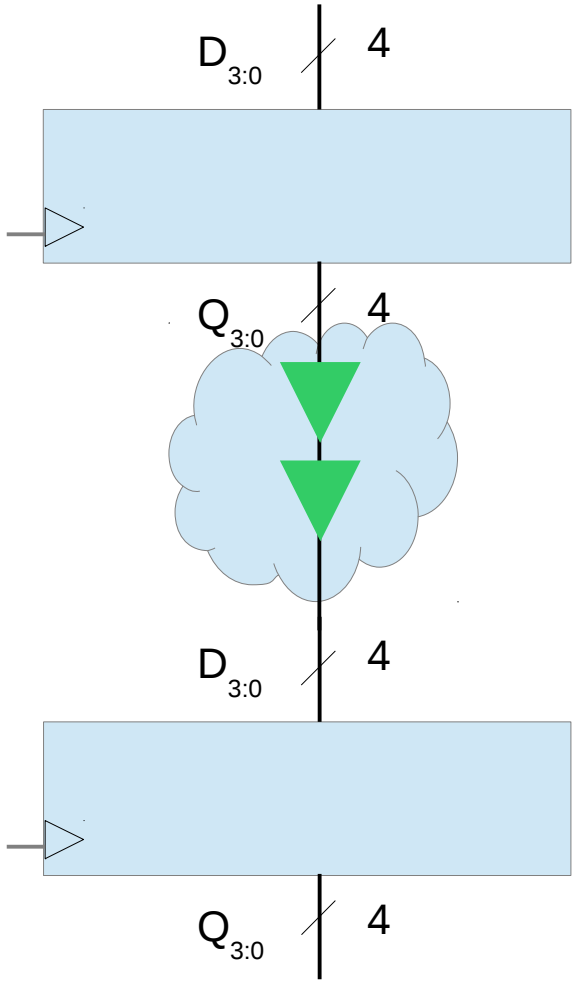


Clock Skew

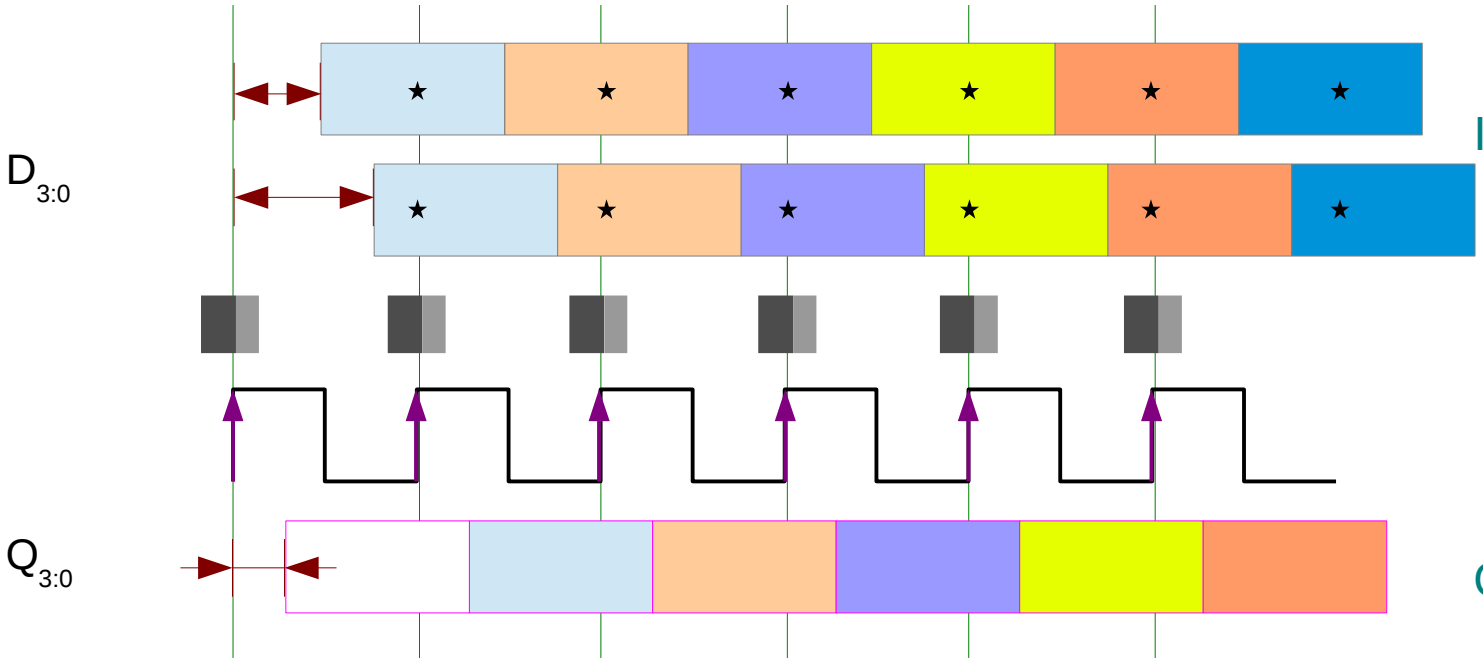


Path Delay


D3:0
Q3:0
delay due to combinational blocks
D3:0
Q3:0

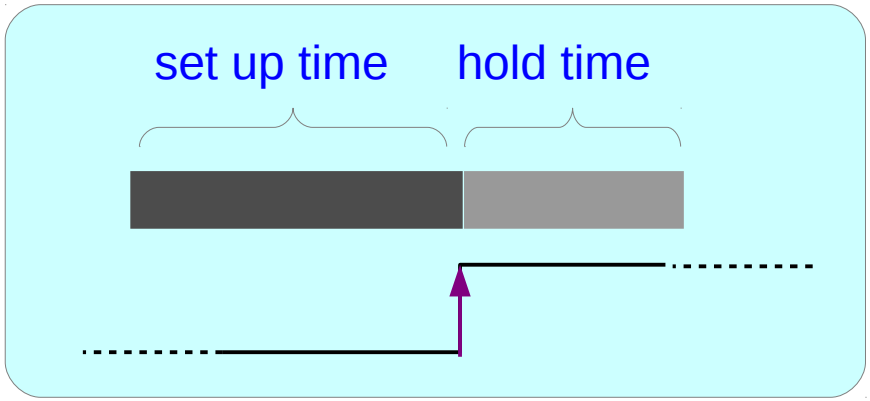

D3:0
4
Q3:0
4
D3:0
4
Q3:0
4

Setup & Hold Time (1)

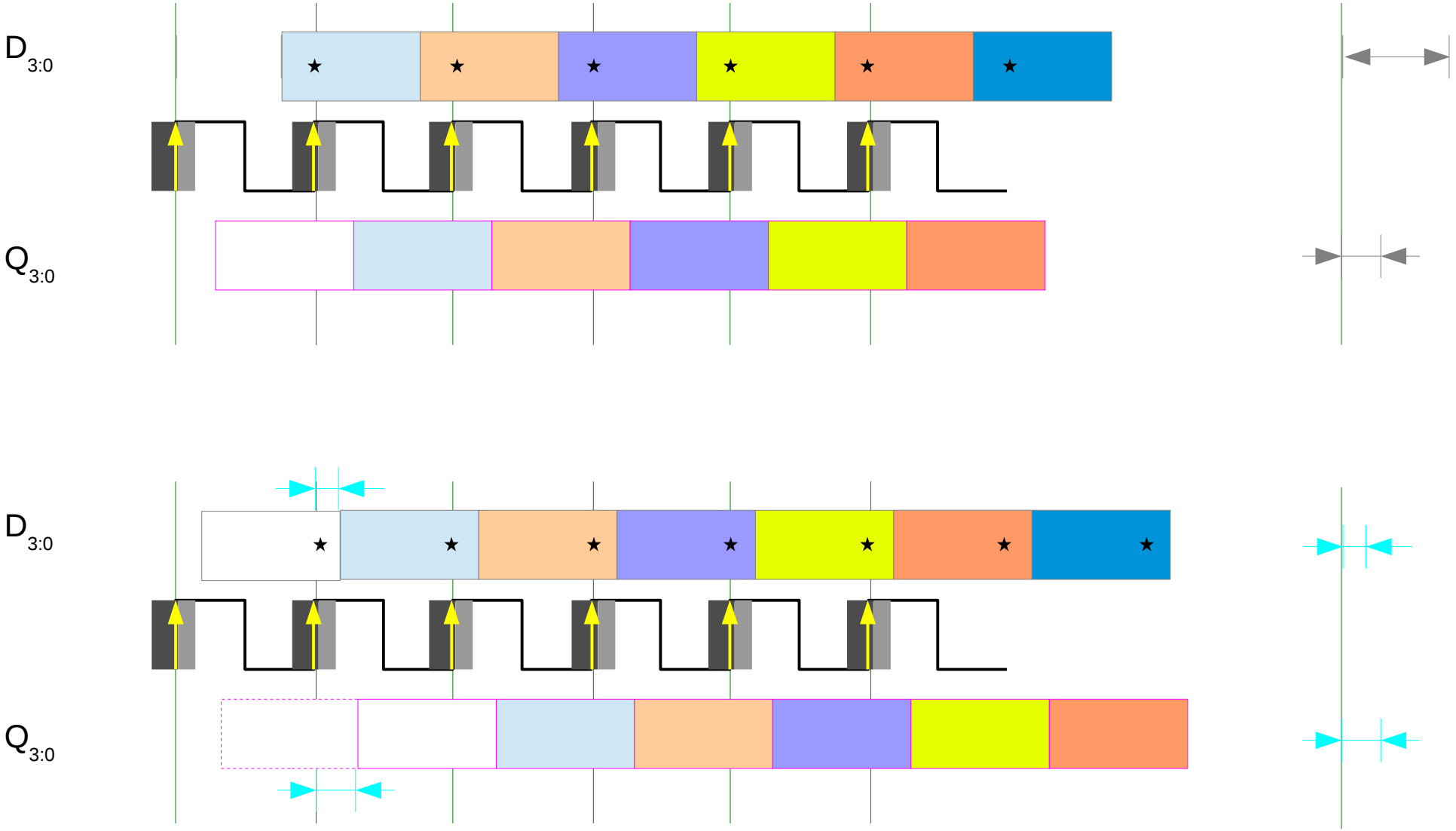


Inputs with delays

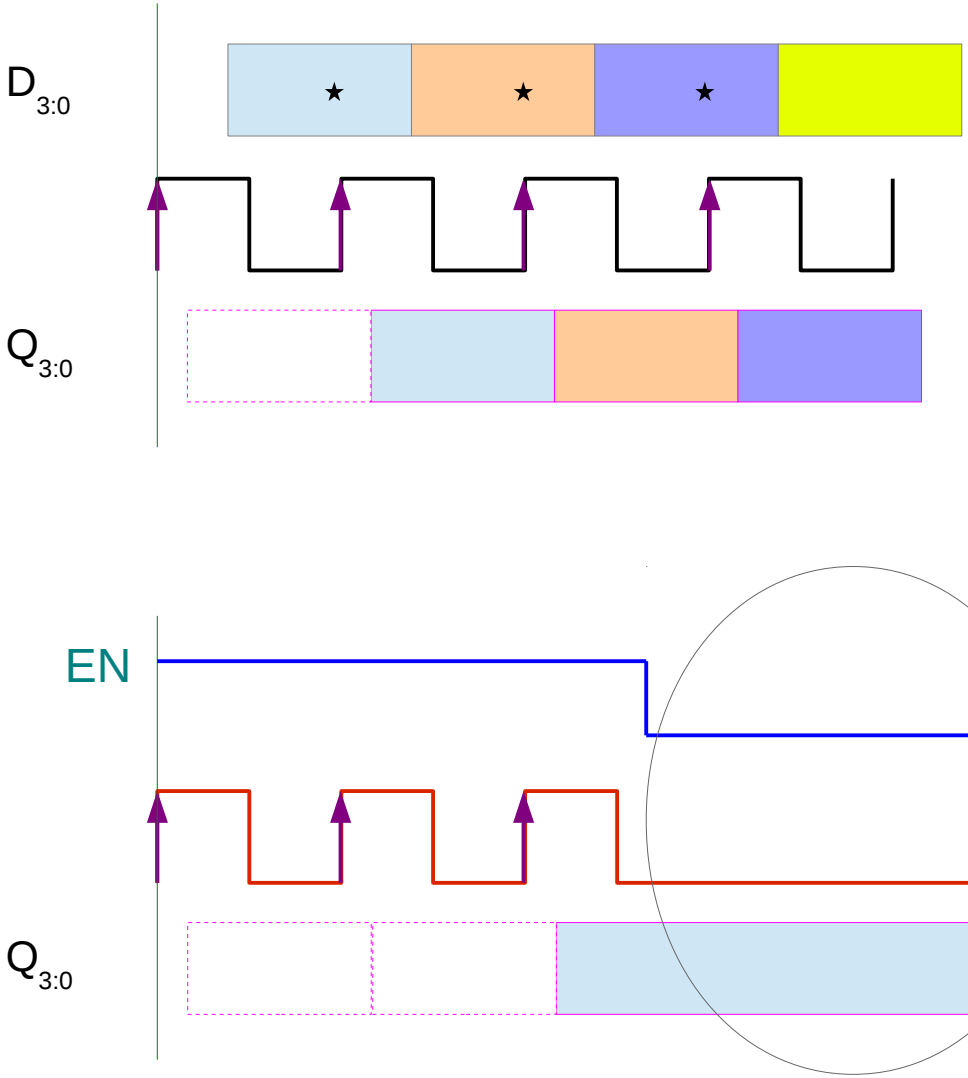
Output with a delay

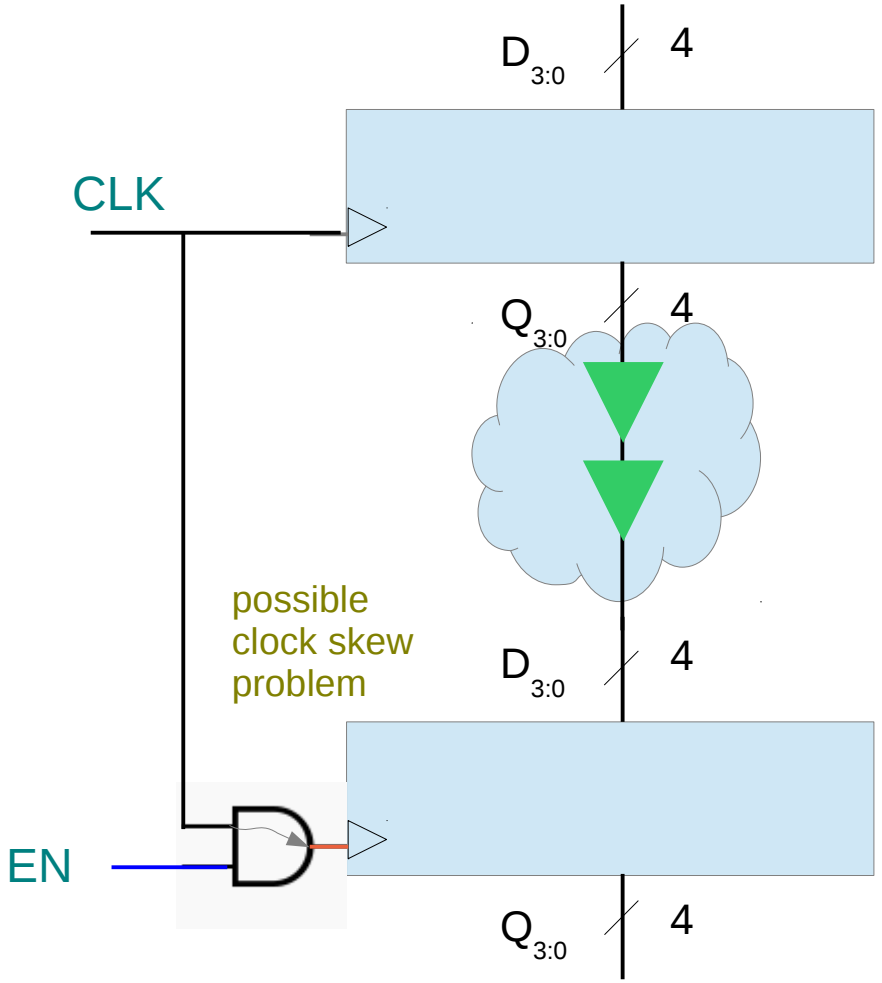


Setup & Hold Time (2)



Clock Gating





References

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[2] http://www.allaboutcircuits.com/
[3] W. Wolf, “Modern VLSI Design : Systems on Silicon
[4] N. Weste, D. Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”
[5] J. P. Uyemura, “Introduction to VLSI Circuits and Systems”
[6] https://en.wikiversity.org/wiki/The_necessities_in_SOC_Design
[7] https://en.wikiversity.org/wiki/The_necessities_in_Digital_Design
[8] https://en.wikiversity.org/wiki/The_necessities_in_Computer_Design
[9] https://en.wikiversity.org/wiki/The_necessities_in_Computer_Architecture
[10] https://en.wikiversity.org/wiki/The_necessities_in_Computer_Organization