Sequential Gates (3B)

Transistor Level Design
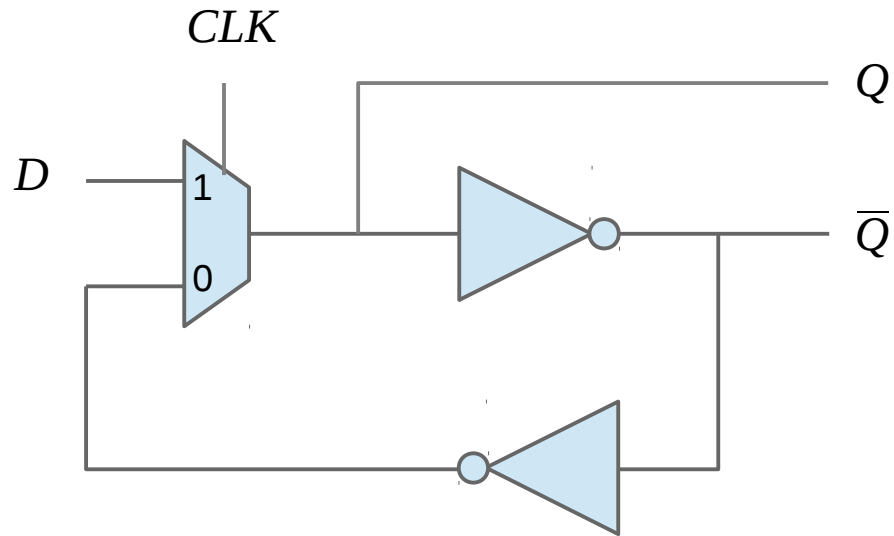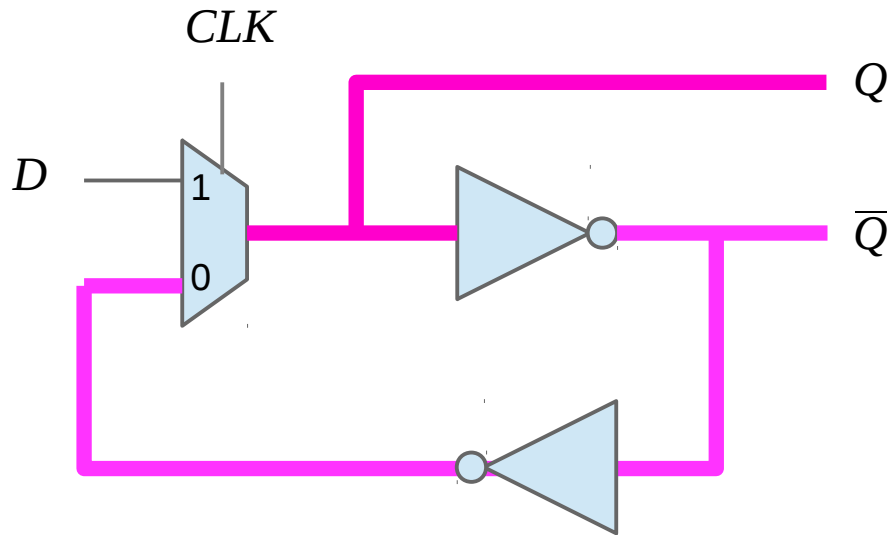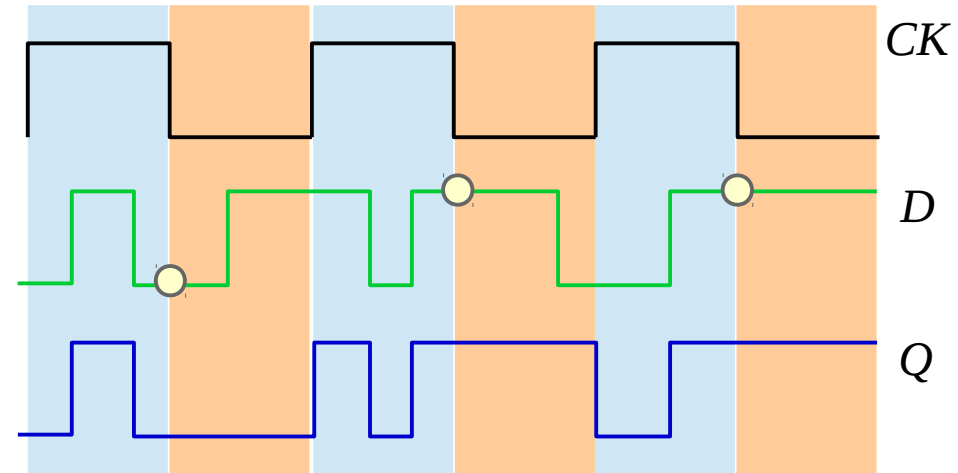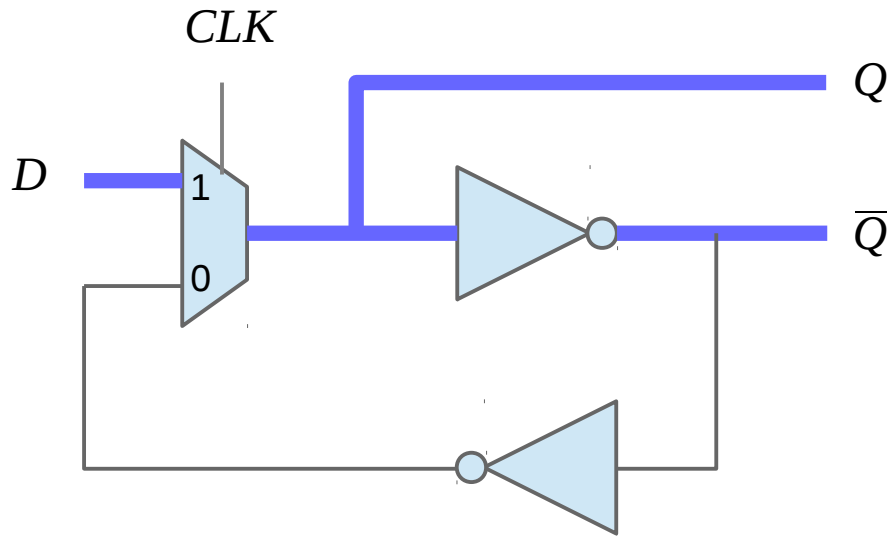
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Please send corrections (or suggestions) to youngwlim@hotmail.com.
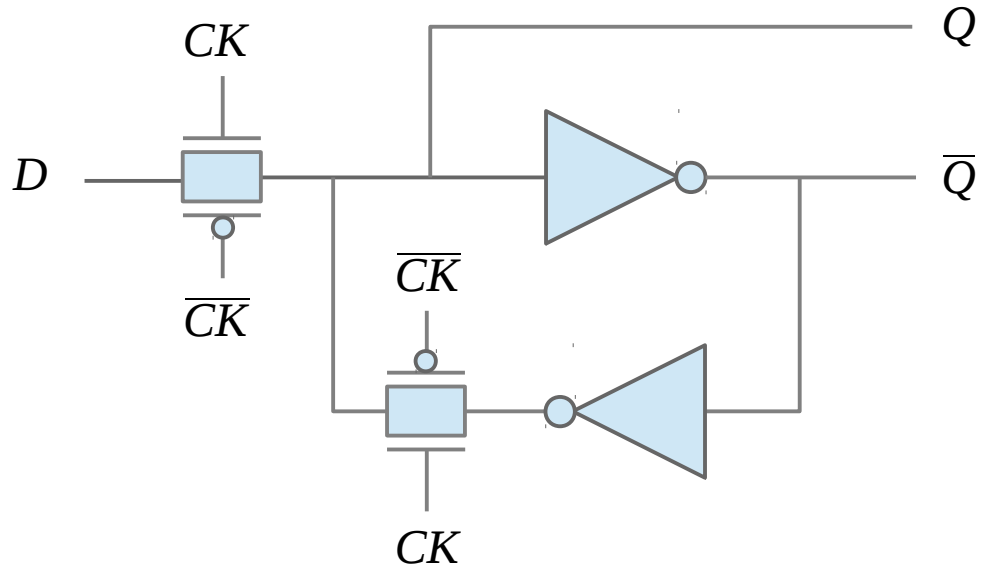
This document was produced by using OpenOffice and Octave.

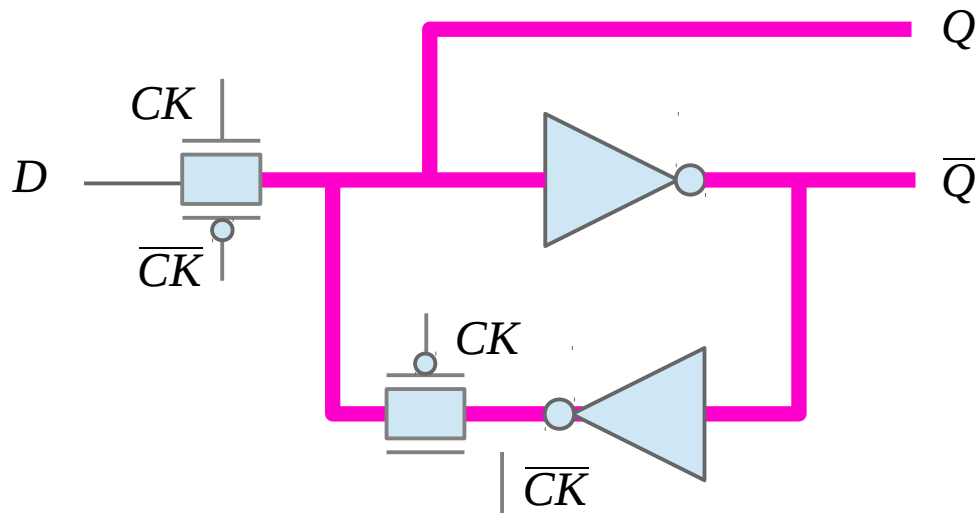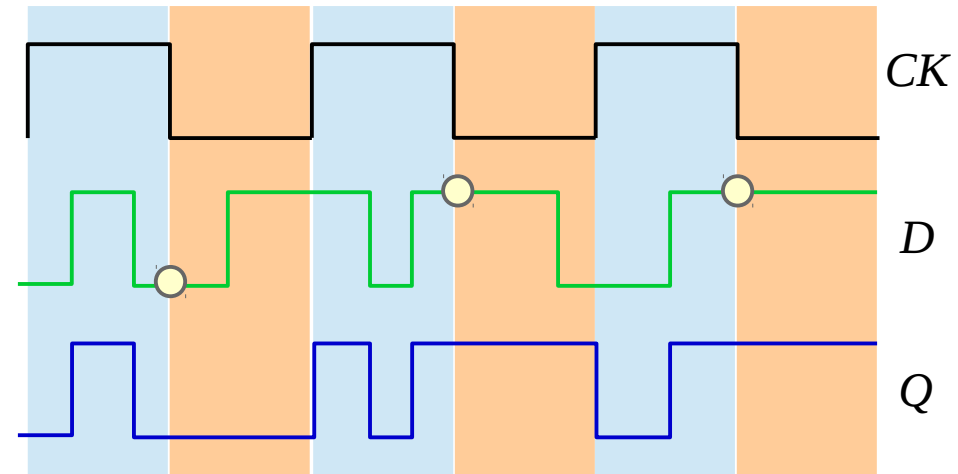# D Latch with Mux (1)

D Latch with Mux (2)

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D Latch with Pass Gate (1)

D Latch with Pass Gate (2)

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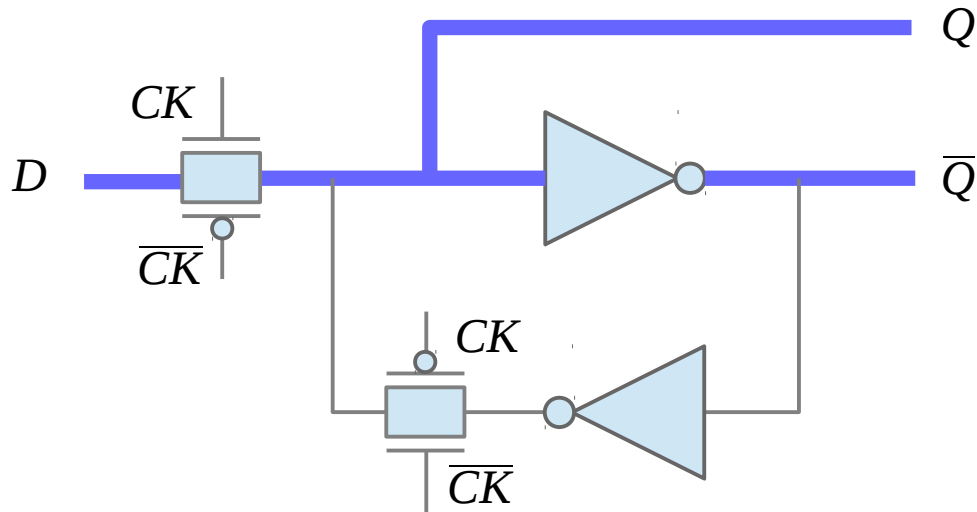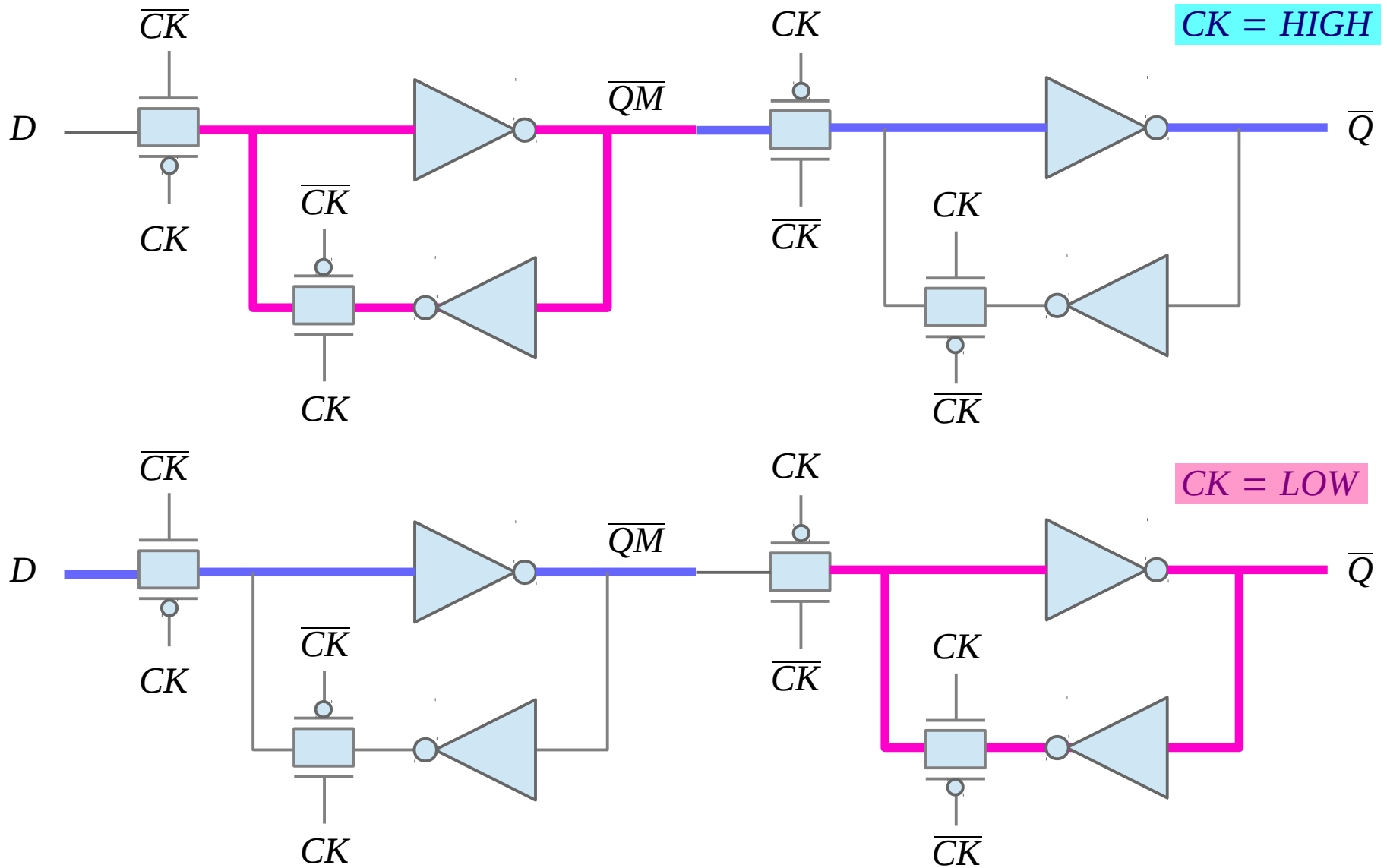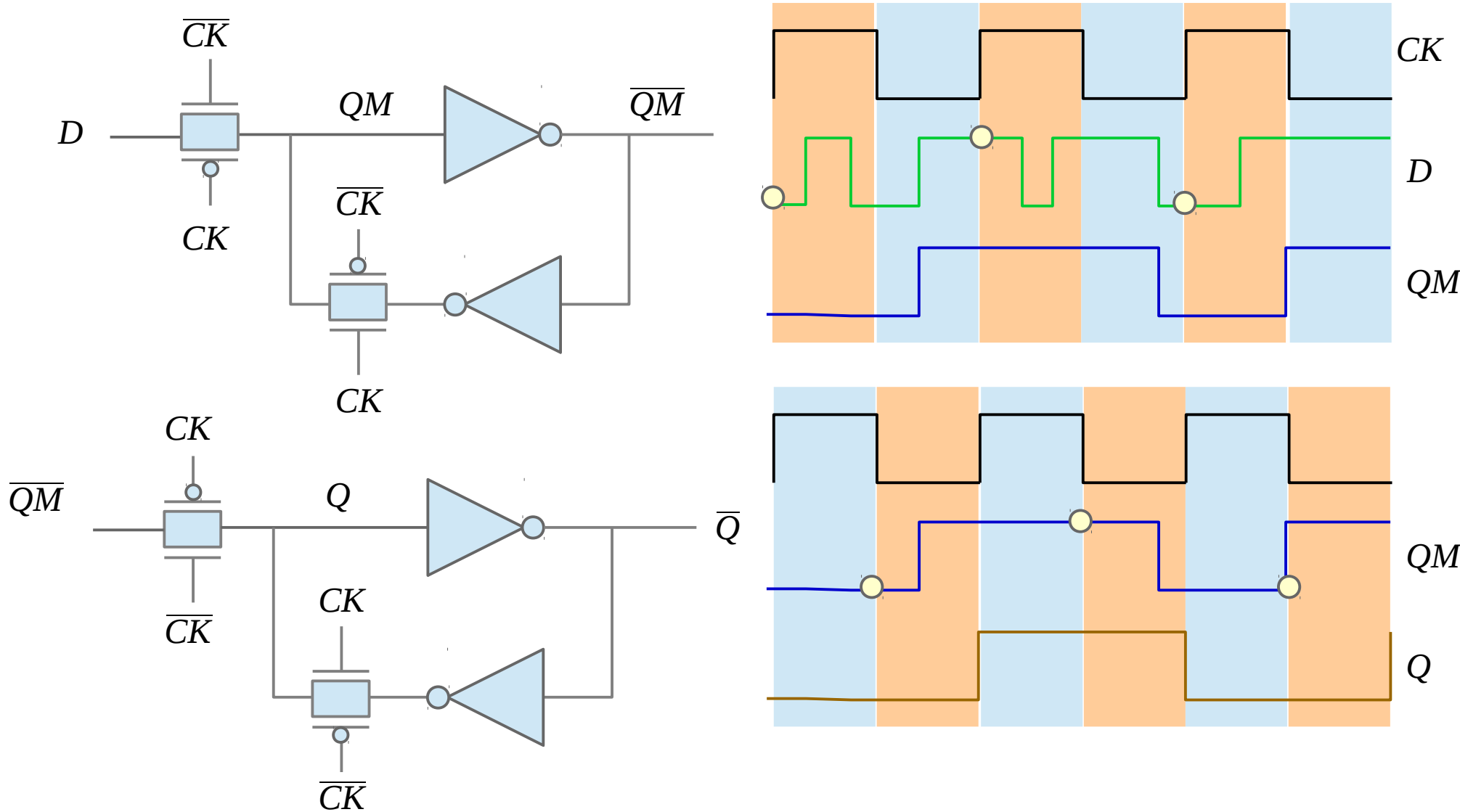
D Flip Flop with Pass Gate (1)
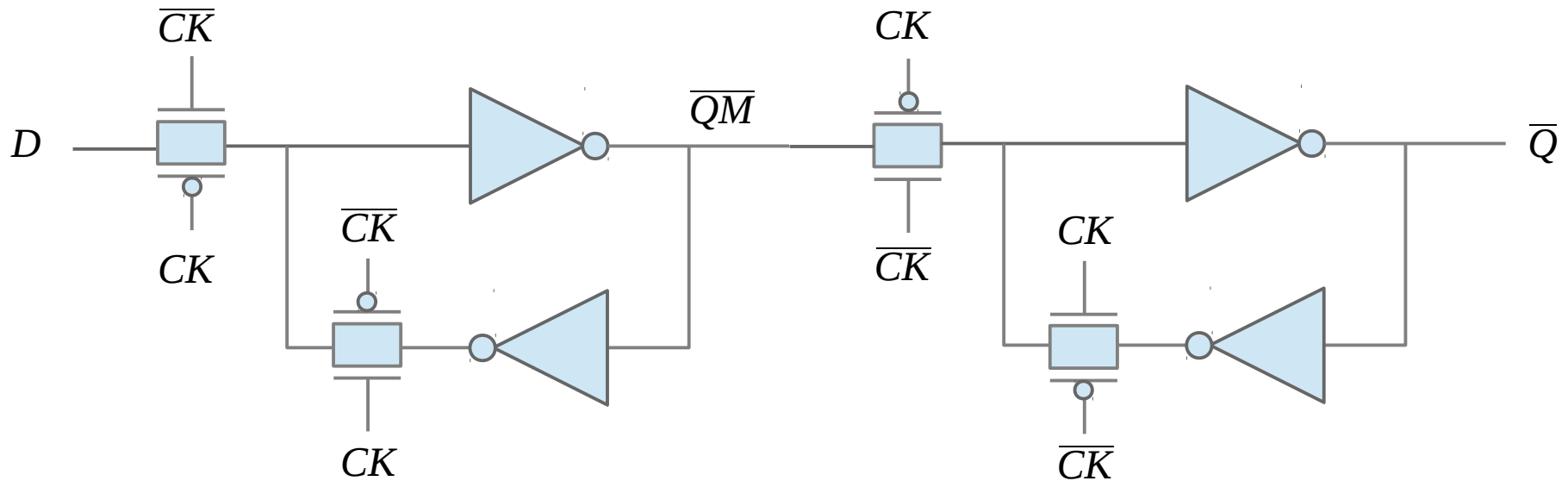
D Flip Flop with Pass Gate (1)

D Latch with Pass Gate (2)

9

Sequential Element Types

CMOS Latches
CMOS FlipFlops
Pulsed Latches
Latches and FlipFlops with a Reset
Latches and FlipFlops with an Enable

References

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[5] J. P. Uyemura, "Introduction to VLSI Circuits and Systems"
[6] https://en.wikiversity.org/wiki/The_necessities_in_SOC_Design
[7] https://en.wikiversity.org/wiki/The_necessities_in_Digital_Design
[8] https://en.wikiversity.org/wiki/The_necessities_in_Computer_Design
[9] https://en.wikiversity.org/wiki/The_necessities_in_Computer_Architecture
[10] https://en.wikiversity.org/wiki/The_necessities_in_Computer_Organization