Device Power (2H)

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Power

Static Power Dissipation

- Sub threshold condition when the transistors are off.
- Tunnelling current through gate oxide.
- Leakage current through reverse biased diodes.
- Contention current in ratioed circuit

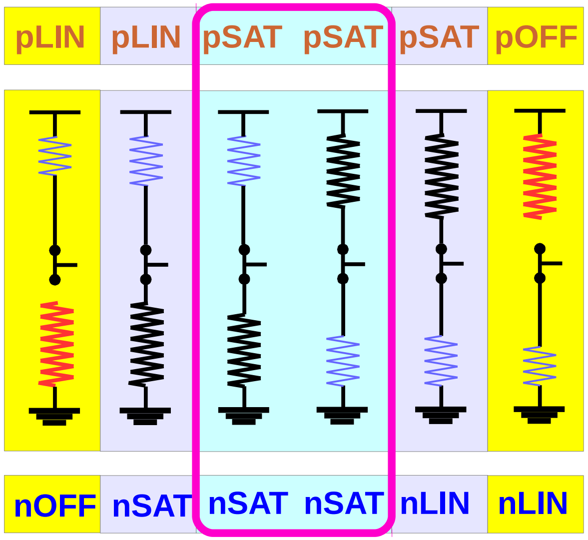
Dynamic Power Dissipation

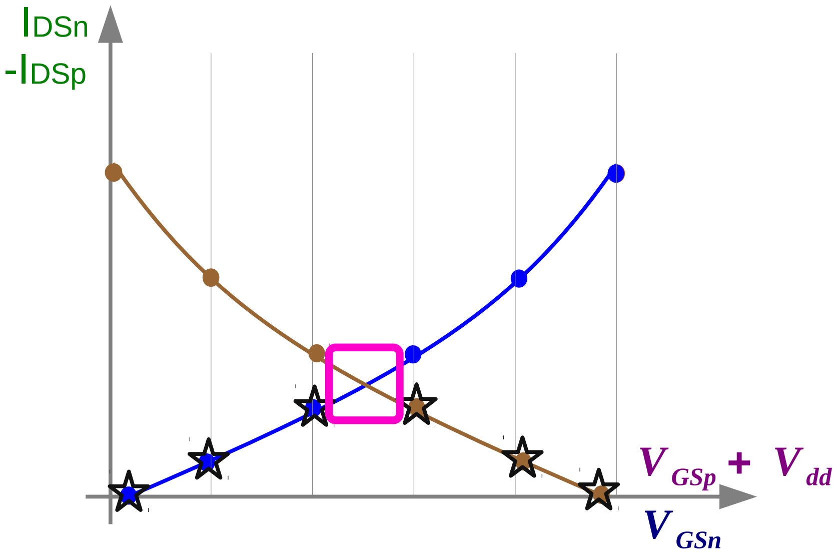
- Charging and discharging of load capacitances.
- Short circuit power dissipation

Short Circuit Power Dissipation

Since there is a finite rise/fall time for both pMOS and nMOS, during transition, for example, from off to on, both the transistors will be on for a small period of time in which current will find a path directly from VDD to ground, hence creating a short circuit current.

Short circuit power dissipation increases with rise and fall time of the transistors.

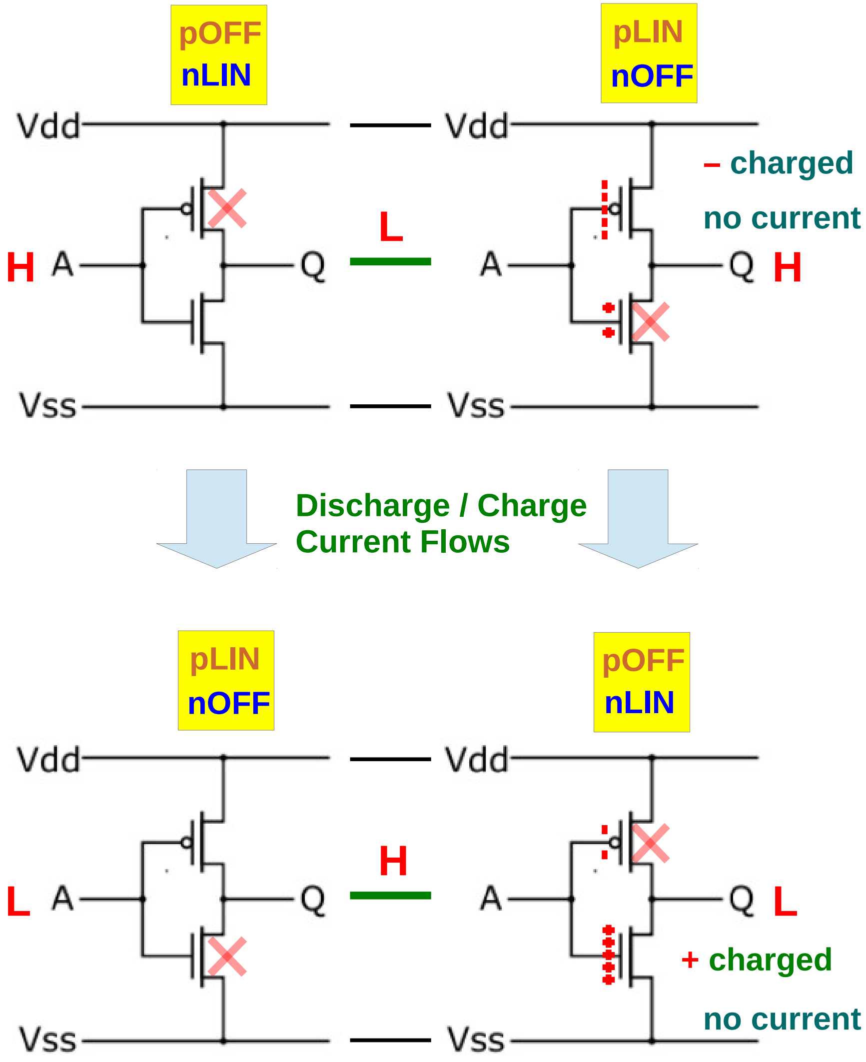




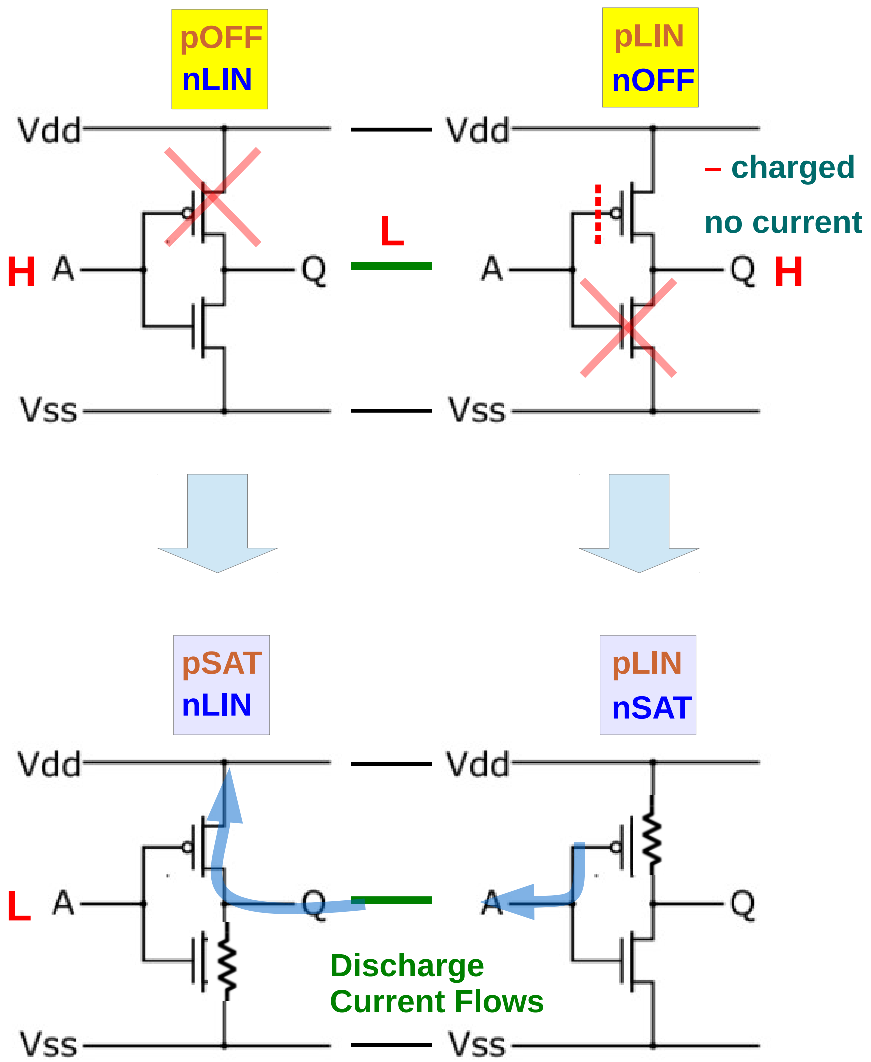
Charging and Discharging Load Capacitance (1)

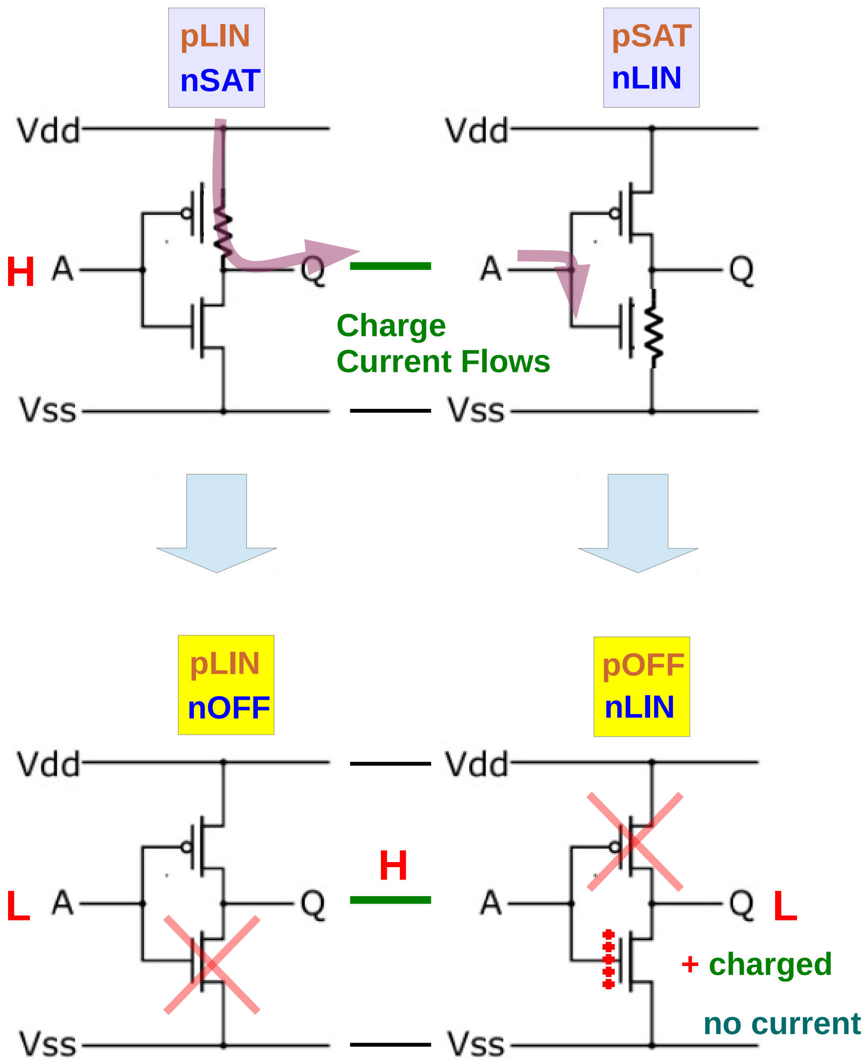
CMOS circuits dissipate power by charging the various load capacitances (mostly gate and wire capacitance, but also drain and some source capacitances) whenever they are switched.

In one complete cycle of CMOS logic, current flows from VDD to the load capacitance to **charge** it and then flows from the charged load capacitance to ground during **discharge**.

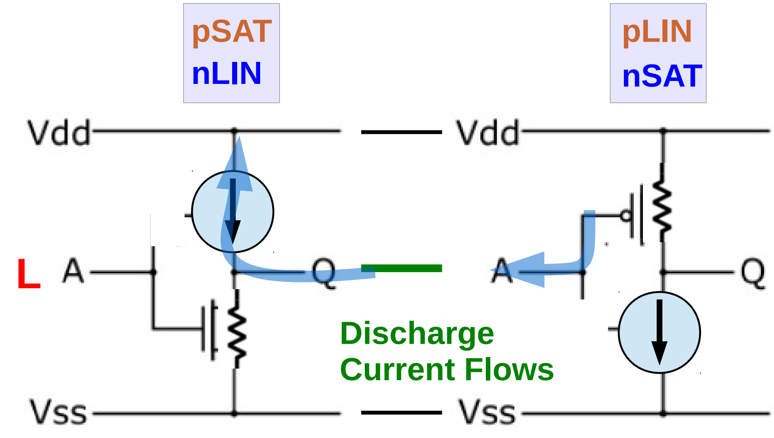


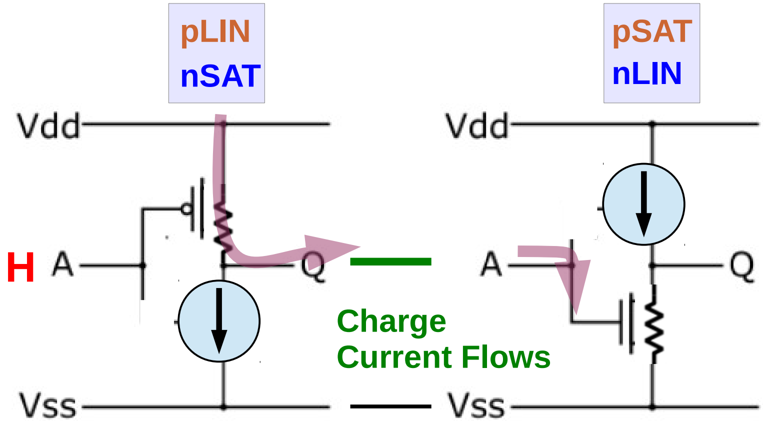
Charging and Discharging Load Capacitance (2)

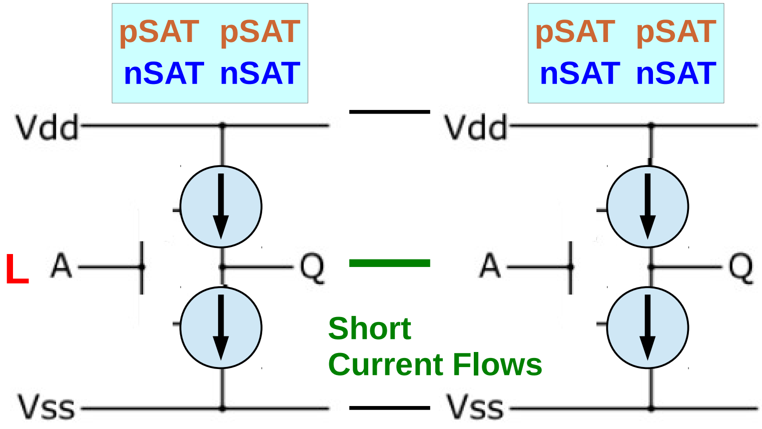




Charging and Discharging Load Capacitance (3)





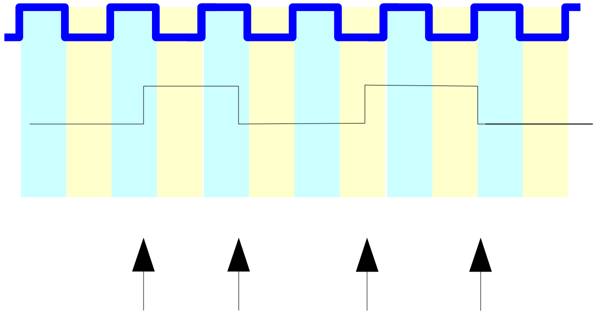


Charging and Discharging Load Capacitances (4)

Therefore in one complete charge/discharge cycle, a total of $Q=C_L V_{DD}$ is thus transferred from V_{DD} to ground.

Multiply by the switching frequency on the load capacitances to get the current used, and multiply by voltage again to get the characteristic switching power dissipated by a CMOS device: $P = C V^2 f$.

Since most gates do not operate/switch at every clock cycle, they are often accompanied by a factor α, called the activity factor. Now, the dynamic power dissipation may be re-written as $P = \alpha C V^2 f$.



Static Power

- Static Power Source
  - Subthreshold Leakage
  - Gate Leakage
  - Junction Leakage
  - Contention Current

  - Static Power Estimation

- Multiple Threshold Voltages and Oxide thickness
- Variable Threshold Voltages
- Input Vector Control

Dynamic Power

Minimize Capacitance
Minimize Short Circuit Current

References

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