Digital Logic Implementation (2C)

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ASIC

An application-specific integrated circuit

an integrated circuit (IC) customized for a particular use, rather than intended for general-purpose use.

Standard Cell

A **standard cell**
a group of transistor and interconnect structures
a boolean logic function (e.g., AND, OR, XOR, XNOR, inverters)
a storage function (flipflop or latch).

The simplest cells: the elemental NAND, NOR, and XOR boolean function
Complex cells: such as a 2-bit full-adder, or muxed D-input flipflop.

Logical view:

Schematic view:

Layout view:

Standard Cell Views

logical view:
The cell's boolean logic function
by a truth table or Boolean algebra equation (for combinational logic)
a state transition table (for sequential logic).

schematic view:
the initial design of a standard cell, developed at the transistor level
the netlist is a nodal description of transistors, of their connections to each other, and of their terminals (ports) to the external environment.
A schematic view may be generated with a number of CAD or EDA

layout view:
the physical representation of the standard cell for device fabrication
the closest to an actual "manufacturing blueprint" of the standard cell

Standard Cell Library

a collection of low-level electronic logic functions
such as AND, OR, INVERT, flip-flops, latches, and buffers.
fixed-height, variable-width full-custom cells.
enables them to be placed in rows,
easing the process of automated digital layout
optimized full-custom layouts to minimize delays and area.

two main components:

Library Database
- layout, schematic, symbol, abstract, and other logical or simulation views
- information for automated "Place and Route" tools.

Timing Abstract
- functional definitions, timing, power, and noise information for each cell.

Standard Cell Design

Logic synthesis transforms the RTL design into a large collection of standard cells. The resulting collection of standard cells, plus the needed electrical connections between them, is called a gate-level netlist

a placement tool places the standard cells onto a region
attempts to find an optimal placement subject to a variety of specified constraints

a routing tool takes the physical placement of the standard cells and uses the netlist to create the electrical connections between them.
The output is a file which can be used to create a set of photomasks enabling a semiconductor fabrication facility

Given the final layout, circuit extraction computes the parasitic resistances and capacitances. In the case of a digital circuit, this will then be further mapped into delay information, from which the circuit performance can be estimated, usually by static timing analysis. This, and other final tests such as design rule checking and power analysis (collectively called signoff) are intended to ensure that the device will function correctly over all extremes of the process, voltage and temperature. When this testing is complete the photomask information is released for chip fabrication.

Gate Array

the diffused layers, i.e. transistors and other active devices, are predefined.
wafers containing such devices are held in stock prior to metallization (unconnected)
the physical design process then defines the interconnections of the final device

- fixed height routing tracks
- two to as many as nine metal layers
- each metal layer running perpendicular to the one below it
- photolithographic masks are required only for the metal layers

production cycles are much shorter

- metallization is a comparatively quick process.

never gives 100% utilization.

- a larger array device

Sea of Gate

contains a continuous array of n and p transistors
polysilicon crossing the n & p diffusions

- – horizontal array of transistors
- – this row repeated vertically

routing channels are over the unused transistors
the core of SOG is surrounded by an array of I/O cells
master or base wafers processed upto polysilicon
metalization and contacts are to be performed

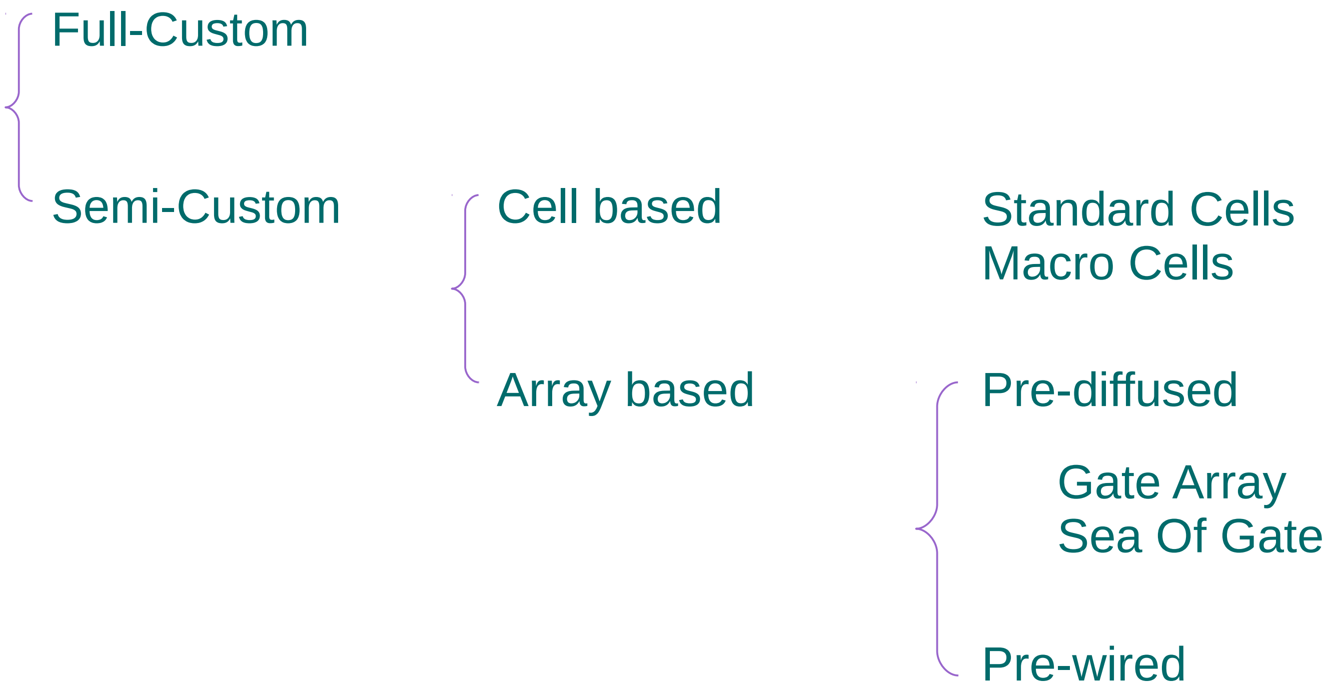
Full Custom Design

all the photolithographic layers of the device

+ reduced area
+ performance improvements
+ the ability to integrate analog components and other pre-designed components

- increased manufacturing and design time
- increased non-recurring engineering costs
- more complexity in the CAD system
- a much higher skill requirement

Digital Circuit Implementation Approaches



Full-Custom

Semi-Custom

Cell based

Standard Cells
Macro Cells

Array based

Pre-diffused

Gate Array
Sea Of Gate

Pre-wired

Programmable Logic Devices

PLA (Programmable Logic Array)
PAL (Programmable Array Logic)
GAL (Generic Logic Array)
CPLD (Complex Programmable Logic Device)
FPGA (Field Programmable Gate Array)

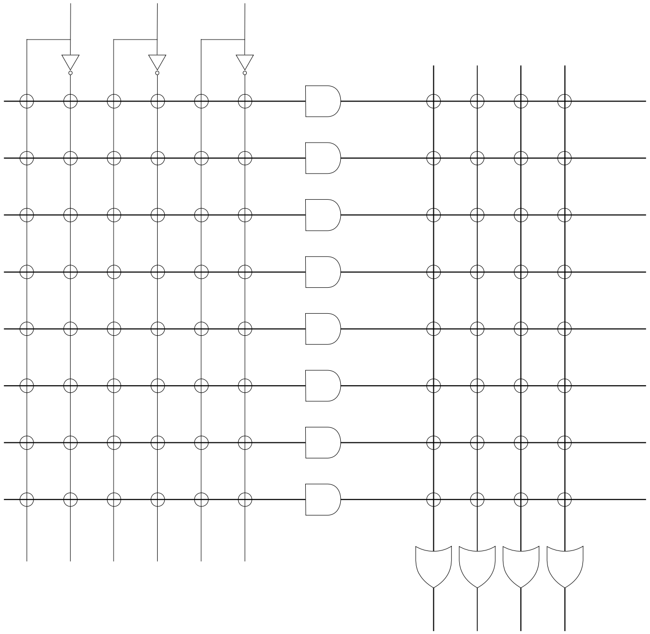
PLA (Programmable Logic Array)

a programmable logic device used to implement combinational logic circuits

has a set of programmable AND gate planes which link to a set of programmable OR gate planes which can then be conditionally complemented to produce an output

allows for a large number of logic functions to be synthesized in the sum of products (and sometimes product of sums) canonical forms.

Not field-programmable
mask-programmed like a mask ROM.

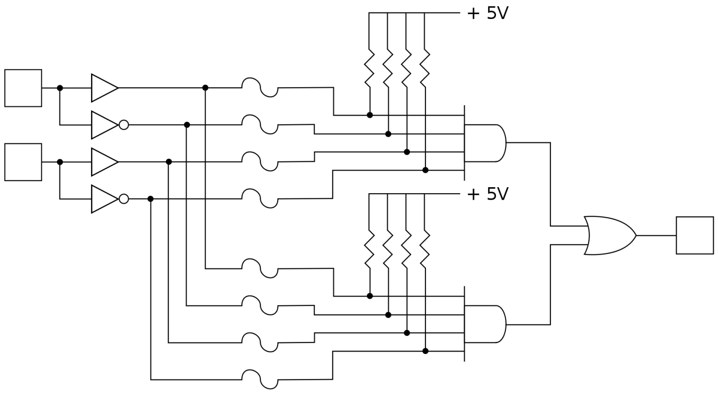


don't-care conditions
with a read-only memory, a don't care condition becomes an address input that will never occur
not all the bit patterns available in read-only memory are used (a waste of available component)

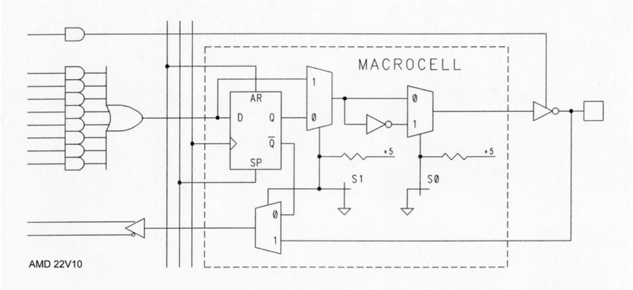
PAL (Programmable Array Logic)

consisted of a small PROM (programmable read-only memory) core
and additional output logic for desired logic functions with few components

field programmable using specialized machines
one-time programmable (cannot be updated)



Simplified programmable logic device



CPLD (Complex Programmable Logic Device)

a programmable logic device with complexity between that of PALs and FPGAs, and architectu
features of both.
the macrocell contains logic implementing disjunctive normal form expressions and more specialized logic operations.

on-chip non-volatile configuration memory. (no external configuration ROM)
(but the latest FPGA products also offer embedded configuration memory)

The method of programming is to solder the device to its printed circuit board, then feed it with
serial data stream from a personal computer. The CPLD contains a circuit that decodes the dat
stream and configures the CPLD to perform its specified logic function.

FPGA (Field Programmable Gate Array)

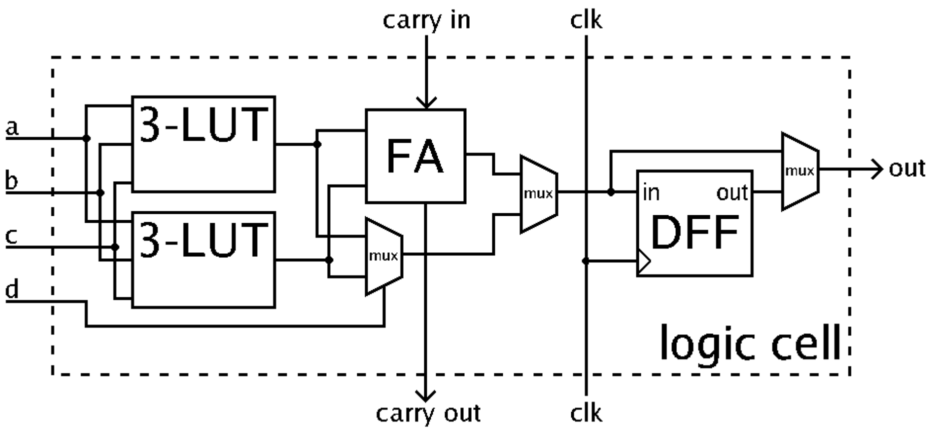
FPGAs use a grid of logic gates, and once stored,
the data doesn't change, like a gate array.
field-programmable - programmed by the customer, not the manufacturer.

FPGAs are usually programmed after being soldered down to the circuit board, in a manner similar to that of larger CPLDs.
In most larger FPGAs the configuration is volatile, and must be re-loaded into the device whenever power is applied or different functionality is required.
Configuration is typically stored in a configuration PROM or EEPROM.
EEPROM versions may be in-system programmable (typically via JTAG).

FPGAs are internally based on Look-up tables (LUTs)
CPLDs form the logic functions with sea-of-gates (e.g. sum of products)
CPLDs are meant for simpler designs
FPGAs are meant for more complex designs

FPGA – Logic Block

contain programmable logic components called "logic blocks"
a hierarchy of reconfigurable interconnects



Dielectric

References

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[3] M.L. Boas, “Mathematical Methods in the Physical Sciences”